

MATHEMATICAL SIMULATION PROGRAM OF DOPED SI OXIDATION IN NANO-DIMENSION SCALE

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Abstract

Micro and nano-electronic structures are the main components of all electronic devices today. Requirements of precision and reliability are applying for medicine electronics. Therefore micro and nano-semiconductor structures must be formed with high accuracy.

The fabrication of microelectronic structures vitally depends on the thermal oxidation for the formation of gate dielectrics, device isolation. Particularly, the precise control of silicon dioxide thickness as device geometries continues to scale to nano dimensions [1].

In semiconductor manufacturing process observed that thickness of SiO₂ layer getting uneven when oxidizing doped Si areas by various dopants. It was defined that boron, phosphorus, arsenic determinate SiO₂ formation in thermal oxidation technological process [2].

Dimension is very important parameter in nano-technologies therefore doping dependent oxidation makes additional problems when forming nano-structures.

By using mathematical simulation program ATHENA was performed mathematical simulation of Si thermal oxidation, and was evaluated the Si substrate doping dependent oxidation.

1. DOPING DEPENDENT OXIDATION

Experimental results explain that SiO₂ formation on highly-doped n-type and p-type substrates can be enhanced compared to SiO₂ formation on lightly-doped substrates. The dependence of silicon dioxide growth kinetics on doping concentration is manifested as part of the linear rate constant, where the physical significance of the high doping levels has been explained primarily as an electrical effect. This factor in the linear rate constant is given by:

$$\left(\frac{B}{A}\right)_{\text{doping}} = \left[1 + B_{K0} \cdot \exp\left(\frac{-B_{FE}}{k_b T}\right) \times \left(V^* \frac{V_i^*}{V_i^*} \right) \right] \quad (1)$$

where V* is the equilibrium vacancy concentration in silicon at the Si/SiO₂ interface. V_i* is the equilibrium vacancy concentration in intrinsic silicon. B_{K0} and B_{KE} relates to the doping dependence of the oxidation rate.

The equilibrium vacancy concentration, composed of vacancy defects in different charged states, depends on the Fermi level location and is given by:

$$V^* = V_i^* \left\{ \frac{1 + \left(\frac{n_i}{n}\right)\phi^+ + \left(\frac{n_i}{n}\right)^2 \phi^{++}}{1 + \phi^+ + \phi^{++} + \phi^- + \phi^=} + \frac{\left(\frac{n}{n_i}\right)\phi^- + \left(\frac{n}{n_i}\right)^2 \phi^=}{1 + \phi^+ + \phi^{++} + \phi^- + \phi^=} \right\} \quad (2)$$

where n is the electron concentration and n_i is the intrinsic carrier concentration, and φ⁺, φ⁺⁺, φ⁻, and φ⁼ are fractions of the vacancy concentration which are positively, double positively, negatively, and double negatively charged respectively.

Figure 1 shows a plot of at for common silicon dopants. Notice that for n-type dopants

(V^*/V_i^*) increases as the doping concentration increases, but V^*/V_i^* remains essentially constant for the p-type dopant. The increase in V^*/V_i^* for n-type dopants increases the linear rate constant. This ultimately leads to thicker oxides when oxidizing highly-doped n-type substrates due to a higher availability of unoccupied silicon lattice sites (vacancies) for oxidant molecules to be incorporated.

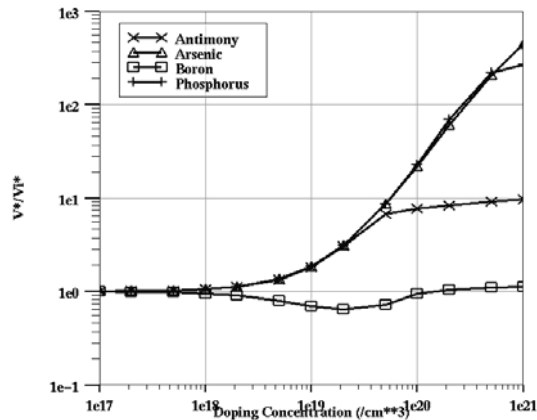


Figure 1. Simulated V/V_i ratio versus doping concentration

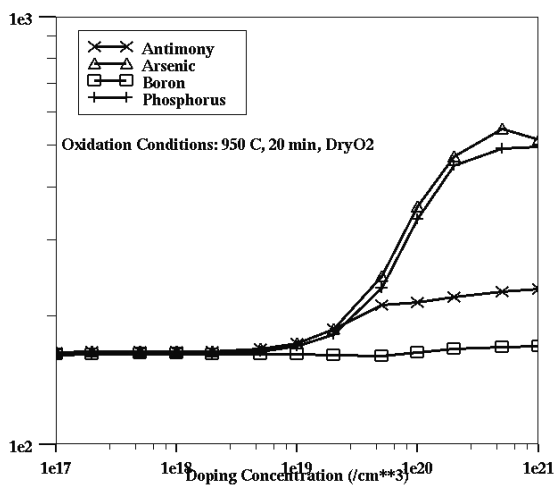


Figure 2. Simulated silicon dioxide thickness vs. doping concentration for common silicon dopants

The oxide thickness trend is shown in figure 2, where the SiO_2 thickness is plotted versus doping concentration for common silicon dopants [3].

2. OXIDATION OF EQUAL SI SUBSTRATE

By using mathematical simulation program ATHENA was performed mathematical simulation of oxidation technological process of undoped Si substrate and phosphorus doped Si substrate. Mathematical simulation results presented at 3 – 6 figures.

Ion implantation technology was used to dope Si by phosphorus. To analyze dopants influence to SiO_2 formation, it was doped one side of Si substrate by using Si_3N_4 mask. Ion implantation dose is $3 \cdot 10^{15} \text{ C/cm}^2$, energy – 10 keV. Ion implantation mathematical simulation results presented at figure 4. Mathematical simulation results (Fig. 4) demonstrate that phosphorus dopants concentrate at right corner of Si substrate.

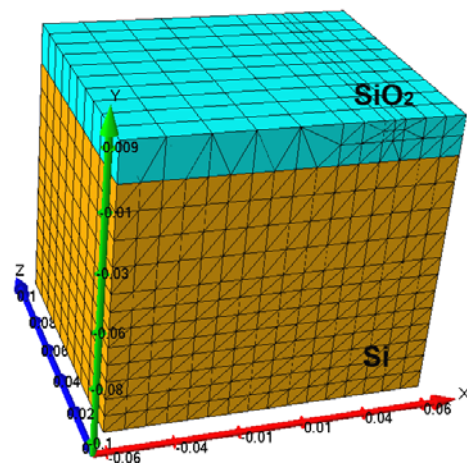


Figure 3. Undoped Si oxidation: oxidation time – 1min., temperature – 1000 °C, ambient – wet O_2

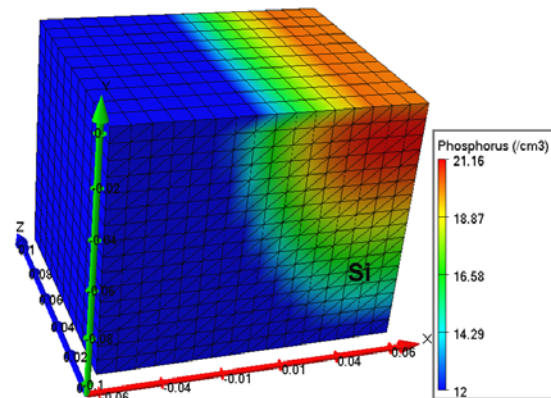


Figure 4. Phosphorus implantation in to Si substrate: ion implantation dose – $3 \cdot 10^{15} \text{ C/cm}^2$, energy – 10 keV

Next step – Si surface oxidation in wet O_2 ambient. Oxidation reaction time is 1 min., temperature – 1000 °C. Mathematical simulation results presented at figure 5.

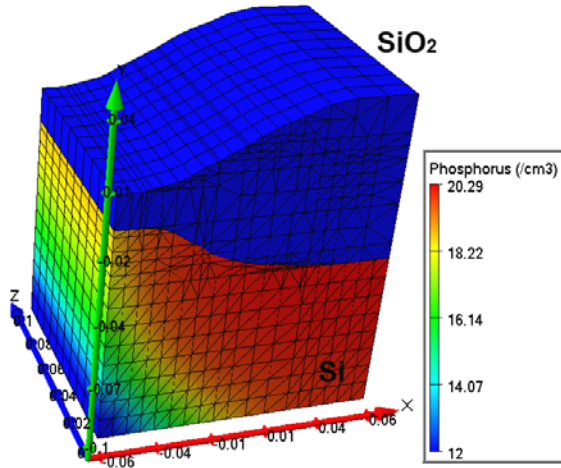


Figure 5. Phosphorus doped Si oxidation: oxidation time – 1min., temperature - 1000 °C, ambient – wet O_2

Figure 6 demonstrate comparison of mathematical simulation results of phosphorus doped and undoped silicon oxidation.

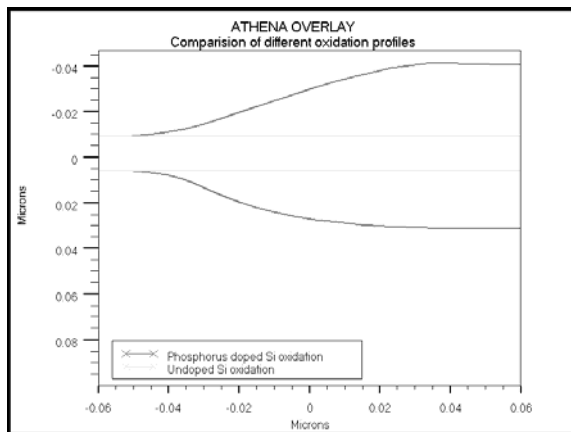


Figure 6. Undoped and phosphorus doped Si oxidation results comparison

During oxidation growing SiO_2 expand up and deep in to Si substrate. This effect is very important in integral elements forming technological process.

Mathematical simulation results demonstrate (Fig. 3-6), that dopant in Si substrate influent to

SiO_2 growing form and to SiO_2 layer thickness – very important parameter. After phosphorus doped Si oxidation process formed SiO_2 thickness is ~ 60nm bigger than oxidizing undoped Si.

3. OXIDATION OF SI SUBSTRATE WITH Si_3N_4 MASK

Local oxidation of silicon (LOCOS) is using to isolate one integral element from another. By using Si_3N_4 mask LOCOS oxide is forming in the certain areas of Si substrate. In the course of Si oxidation oxygen molecules penetrate under the masking Si_3N_4 layer, therefore surface becomes uneven. Irregularities are rather high, up to 0.3-0.6 μm . Irregularities themselves do not increase metallization defects, however, they lift Si_3N_4 causing cracks in it as well as impede the photolithography deposition process [5].

Inequalities of the surface getting very important in nano dimension scale because thickness of deposited layers is very small and in this case arising number of defects in the deposited layer (Fig. 7)

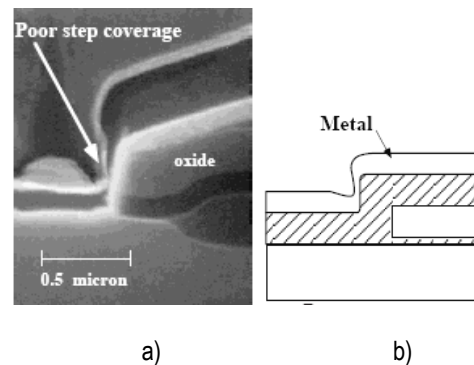


Figure 7. Metal deposition defect [5]

Simulation of oxidation technological process of Si substrate with Si_3N_4 mask it was performed by using mathematical simulation program ATHENA. In first of all it was performed undoped Si oxidation (Fig. 8) and then phosphorus doped Si oxidation (Fig. 10) to investigate the Si dopants influence to oxidation.

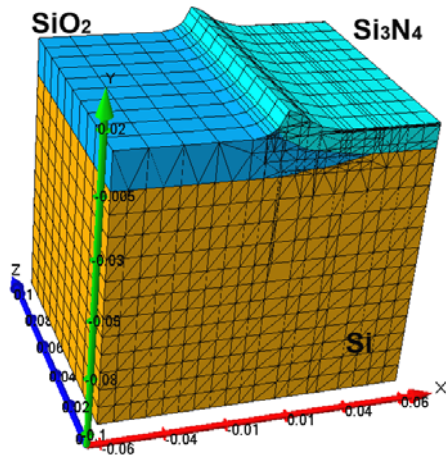


Figure 8. Boron doped Si substrate oxidation with Si_3N_4 mask: oxidation time – 1min., temperature - 1000 °C, ambient – wet O_2

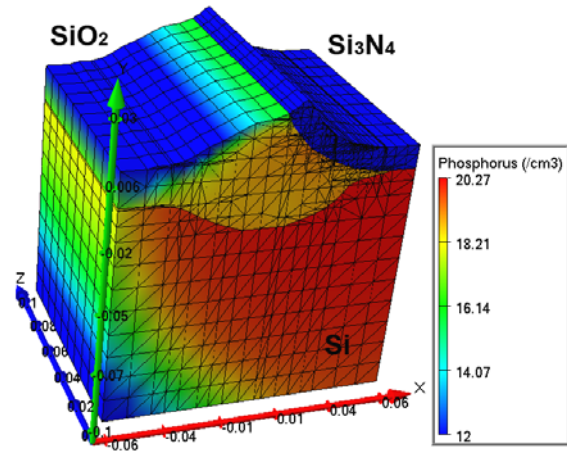


Figure 10. Phosphorus doped Si oxidation with Si_3N_4 mask: oxidation time – 1min., temperature - 1000 °C, ambient – wet O_2

Ion implantation technology was used to dope Si by phosphorus (Fig. 9). Ion implantation dose is $3 \cdot 10^{15} \text{ C/cm}^2$, energy – 10 keV. The less ion implantation energy is using to form nano-structures.

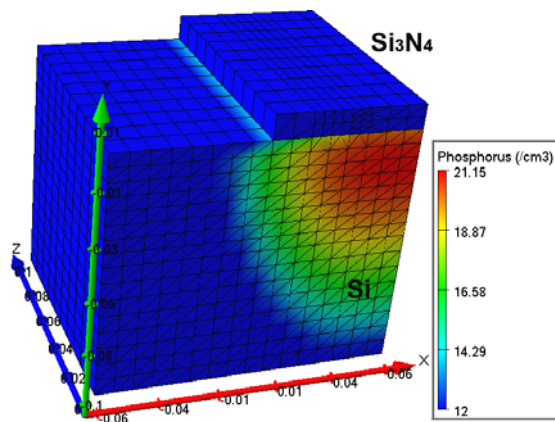


Figure 9. Phosphorus implantation in to Si substrate: ion implantation dose – $3 \cdot 10^{15} \text{ C/cm}^2$, energy – 10 keV

Impurities diffuse from high-doped regions to adjacent layers then performing oxidation. Mathematical simulation results in figures 9 and 10 demonstrate that phosphorus diffuse in to adjacent areas of Si substrate. This effect is very important when need to form p-n junctions in the particular depth [6].

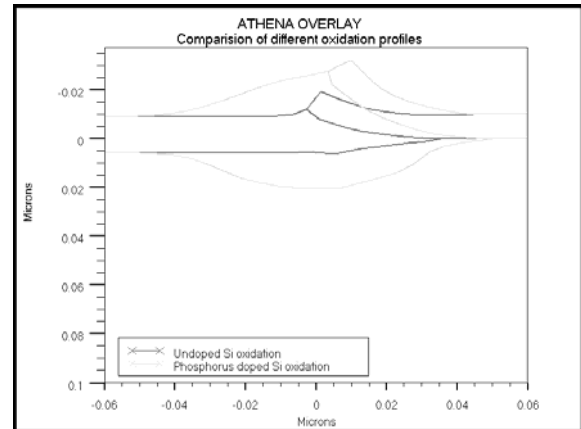


Figure 11. Undoped and phosphorus doped Si with Si_3N_4 mask oxidation results comparison

Mathematical simulation results of doped and undoped Si with Si_3N_4 layer oxidation (Fig. 11) demonstrate that dopants in the Si substrate accelerate SiO_2 forming process and also accelerate SiO_2 drift under the Si_3N_4 mask. Therefore growing SiO_2 form is changing markedly, surface becomes uneven. Irregularities of surface can reach ~ 40nm.

To prevent thermal diffusion of impurities it is purposeful in first of all to use thermal oxidation and then Si doping. In first of all Si substrate was oxidized in wet O_2 ambient 1 min at 1000 °C temperature. After that it was performed phosphorus doping by using ion implantation. Mathematical simulation results presented at figure 12.

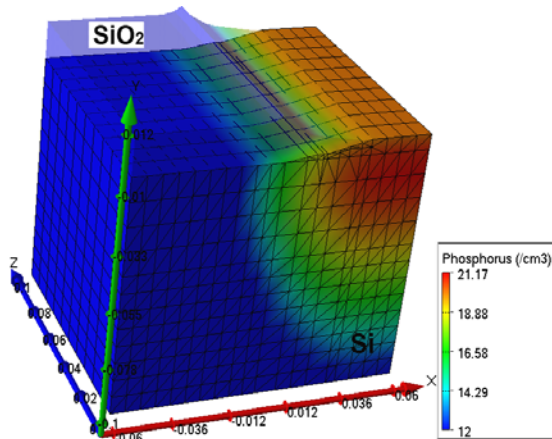


Figure 12. Phosphorus doped regions forming in to oxidized Si substrate: ion implantation dose – $3 \cdot 10^{15}$ C/cm², energy – 10 keV

Comparison of simulation results in figures 8, 9, 10 and 14 demonstrate that more acceptable results obtaining then in first of all are using thermal oxidation and doping process after that. It is avoiding thermal diffusion of impurities and dopants influence to SiO₂ forming process. The surface of formed structure is smoother, therefore number of defects in deposited layer decreasing.

4. CONCLUSIONS

Inequalities of the surface are very important in nano dimension scale because thickness of deposited layers is very small and in this case arising number of defects in the deposited layer.

Dopant in Si substrate influent to SiO₂ growing form and to SiO₂ layer thickness – very important parameter. Dopants in the Si accelerate SiO₂ forming. After phosphorus doped Si oxidation process formed SiO₂ thickness is ~ 60nm bigger than oxidizing undoped Si. Surface of the structure becomes uneven and irregularities of surface can reach ~ 40nm.

To prevent dopants influence to SiO₂ growing and thermal diffusion of dopants it is purposeful in first of all to use thermal oxidation and then Si doping. The surface of formed structure obtaining smoother, therefore number of defects in deposited layer decreasing.

References

- [1] Marcinkevičius A. J. Integral elements design. Vilnius Gediminas Technical University. - Vilnius: Technique, 2004.
- [2] Stephen A. Campbell. The Sciences and Engineering of Microelectronic Fabrication. New York: Oxford University Press; 2001. p. 83 - 86.
- [3] ATHENA user manual. Official Website of SILVACO International. Internet. <http://www.silvaco.com> [02/02/2008]
- [4] Eidukas D, Anilionis R, Kersys T. Simulation of LOCOS Technology // Proceedings of the 18-th International Conference on Production Research; 2005 July 29 – August 2; Fisciano [SA], Italy. Salerno: University of Salerno; 2005. p. 163.
- [5] Physics and Modelling of VLSI Fabrication Courses. Internet. <http://dunham.ee.washington.edu> [02/02/2007]
- [6] Keršys T., Andriukaitis D., Anilionis R. VMOS, UMOS Technology Simulation // 28-th International Conference Information Technology Interfaces (ITI 2006). - University of Zagreb, University Computing Centre, Cavtat / Dubrovnik, Croatia. – 06 19 – 06 22 2006.