INVESTIGATION OF ETCHING PROCESS AND DIFFERENT CRYSTALLOGRAPHIC PLANE ORIENTATION DEPENDENCE MATHEMATICAL SIMULATION IN NANO SCALE STRUCTURES

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Abstract

Problems of etching process, related with MOS transistors separation in SOS technology was researched. Integral circuit and their elements must be released with high precision. After a photo mask has been created a layer under the resist is etching. Wet Etching provide a higher degree of selectivity than dry etching techniques. In isotropic etching materials are removed uniformly from all directions. A vertical profile can be easily made using anisotropic etching and it solves the problem of lateral etching. Using dry etching it is much easier to start and stop than simple immersion wet etching and less lateral encroachment is achieved. The main avantage of ion milling is directionality. That's why less lateral encroachment during region formation could be achieved using ion milling according to wet and dry etching process simulation results. Also relationship between etching process and crystallographic planes orientation are analyzed, because etch rate is different using different crystallographic planes orientations.

1. INTRODUCTION

Integral circuit (IC) and their elements must be released with high precision. The IC made modern day information processing and communications systems possible. It's basic functional element is the transistor, most commonly a silicon metal oxide semiconductor field-effect transistor (MOSFET). In MOS/CMOS structures regions between the active elements must be isolated [1]. That's why etching process is important to IC formation. Choosing correct type of etch is possible to avoid disasters like: lateral encroachments, undesirable dislocations, bird's beak (in thermal oxidation).

Etching process described by etch rate – dimension of thickness per unit. A large etch rate is like advantage in technological process. Too high an etch rate is treat like lack, because it is difficult to control etching process. Etch process rate can reach hundreds nanometers per minute by common way [2, 3, 4].

Every technological process holds on MOS transistors or IC less or more. Every technological process related with past one (for example: diffusion depends on wafer (crystal lattice) quality, which depends on technological process temperature) [5].

2. VERY-LARGE-SCALE INTEGRATION

Early ICs of the late 1950s consisted of about 10 components on a chip 3 mm square. Very large-scale integration (VLSI) vastly increased circuit density, giving rise to the microprocessor. The first commercially successful IC chip (Intel, 1974) had 4,800 transistors; Intel's Pentium (1993) had 3.2 million, and more than a billion are now achievable [3]. VLSI is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip [6]. The microprocessor is a VLSI device.

In micro/nanofabrication, in addition to thin film etching, very often the substrate also needs to be removed in order to create various mechanical micro-/nanostructures. Two important figures of merit for any etching process are selectivity and directionality. Selectivity is the degree to which the etchant can differentiate between the masking layer and the layer to be etched. Directionality has to do with the etch

profile under the mask. In an isotropic etch, the etchant attacks the material in all directions at the same rate, creating a semicircular profile under the mask. In an anisotropic etch, the dissolution rate depends on specific directions, and one can obtain straight sidewalls or other non-circular profiles. Also it is possible divide the various etching techniques into wet and dry categories.

3. ETCHING TECHNIQUES

3.1. Wet Etching

Wet etchants are by and large isotropic and show superior selectivity to the masking layer compared to various dry techniques. In addition, due to the lateral undercut, the minimum feature achievable with wet etchants is limited. Silicon dioxide is commonly etched in a dilute. Photoresist and silicon nitride are the two most common masking materials for the wet oxide etch. Nitride wet etch is not very common, due to the masking difficulty and unrepeatable etch rates.

Anisotropic and isotropic wet etching of crystalline and non-crystalline substrates are important topics in micro/nanofabrication.

For short etch times, silicon dioxide can be used as the masking material. However, one needs to use silicon nitride if a longer etch time is desired.

3.2. Dry Etching

Most dry etching techniques are plasma-based. They have several advantages compared with wet etching. These include smaller undercut (allowing smaller lines to be patterned) and higher anisotropicity (allowing high-aspect-ratio vertical structures). However, the selectivity of dry etching techniques is lower than the wet etchants, and one must take into account the finite etch rate of the masking materials.

The three basic dry etching techniques, namely, high-pressure plasma etching, reactive ion etching (RIE), and ion milling utilize different mechanisms to obtain directionality.

4. MOS TECHNOLOGICAL PROCESS

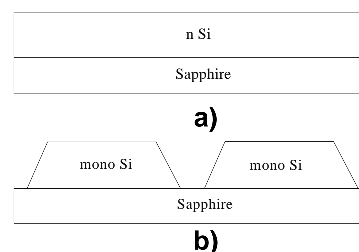
To improve MOS structure parameters parasitic capacities: gate-source, gate-drain has to be returned to minimum. In order to reduce parasitic capacities we must avoid lateral diffusion, the size of gate electrode must be the same during all technological processes in order to avoid source-drain channel shortening. The area of element formation must be the same during all technological processes. Separation of MOS elements can be produced using local oxidation [7] and silicon on sapphire technologies.

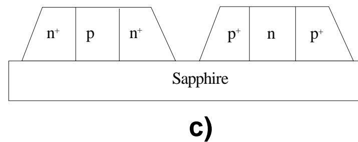
Thermical grown silicon oxide separates semiconductor elements. It is necessary to get hole with less lateral etched side wall. The lateral oxidation can be formed during local oxidation. Therefore length of the source-drain channel decreases, because source and drain regions can be moved under the gate. A large attention must be paid to this process.

Silicon on Sapphire (SOS) technology have recently attracted more and more interest in the development of next-generation high-performance VLSI circuits and systems. The absence of latch-up, the reduced parasitic capacitance, the transparency of the substrate, the isolation and multi-threshold devices are just a few of the advantages of this technology.

Silicon on sapphire is an integrated circuit manufacturing technology. It is a hetero-epitaxial process that consists of a thin layer of silicon grown on a sapphire (Al_2O_3) wafer and this epitaxial layer etching (Fig. 2).

Created silicon regions are isolated by wafer from bottom and from the side by air space. It is necessary to avoid lateral encroachment during region formation, because "active" length of region can be reduced, where transistors are formed.





c)

Φιγυρε 2. ΣΟΣ τεχνολογψ: α επιταξιαλ οφ σι λιχον; β σεπαρατεδ ρεγιονσ οφ σιλιχον χρεατ ιον; χ φορματιον οφ ΝΜΟΠ ανδ ΠΜΟΠ τρανσ ιστορσ

MOS transistor characterized by the output characteristic ($I_D(U_{DS})$). It is connected by common-source scheme. The inversion layer charge density varies in the channel between the source and the drain from 0 to L, channel voltage varies from 0 to U_{DS}:

$$\int_0^L I_D dy = -\mu C_{ox} B \int_0^{V_{SI}} (U_{GS} - U_S - U_C - U_T) dU_C, \quad (1)$$

$$I_D = -\mu C_{ox} \frac{B}{L}((U_{GS} - U_T)U_{DS} - \frac{U_{DS}^2}{2}),$$

$$when \; U_{DS} < U_{GS} - U_T, \quad (2)$$

where μ – the mobility, cm²/V; C_{ox} – capacitance per unit area, μF; B – gate width , nm; L – gate length , nm; U_{GS} – gate-source voltage, V; U_S – drain-source voltage, V; U_C – inversion channel voltage, V; U_T – threshold voltage, V. Output current direct proportional channel length (2). In this we got, that decreases channel length increases escarpment of transistor output characteristics, threshold voltage and drain current.

5. PROCESS SIMULATION

Etch process is simulated with ATHENA. ATHENA is a simulator that provides general capabilities for numerical, physically – based, two – dimensional simulation of semiconductor processing.

The ELITE module of ATHENA allows the use of sophisticated models for etch process. This process is modeled by defining a machine and invoking the machine to perform etch [8].

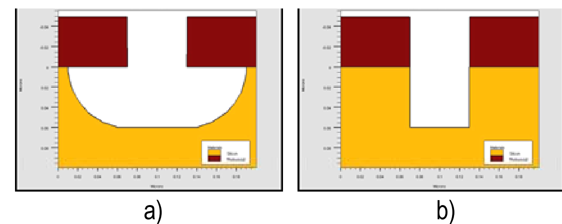
For all models except Monte Carlo Etching, ELITE uses a string algorithm to describe topographical changes that occur during etching process.

As micro/nanofabrication technology becomes more complex, modeling each step of the manufacturing process is increasingly important for predicting the performance of the technology.

Etching is a step that is universal in micro/nanofabrication. It may take place as the dissolution of a photoresist by an organic solvent, the etching of an oxide by an alkali, or the plasma etching of an electron resist. Whatever its physical details, the etching process can in many cases be modeled as a surface etching phenomenon. Etching simulation starts from an initial profile that moves through a medium in which the speed of etching propagation can be a function of position and other variables that determine the final profile.

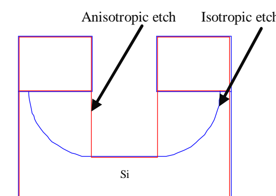
Main task of etching process simulation is avoid lateral encroachment during region formation.

Wet Etching can provide a higher degree of selectivity than dry etching techniques. In isotropic etching (Fig. 3a) materials are removed uniformly from all directions and it is independent of the plane of orientation of the silicon (crystal lattice). Anisotropic etching presents presents the opposite behavior of isotropic etching. Anisotropic etchants remove materials based on the crystal plane and do not etch uniformly in all directions (Fig. 3b)



a) b)

Φιγυρε 3. Ωετ ετχηινγ τψπεσ: α ισοτροπιχ ετχ η; β ανισοτροπιχ ετχη



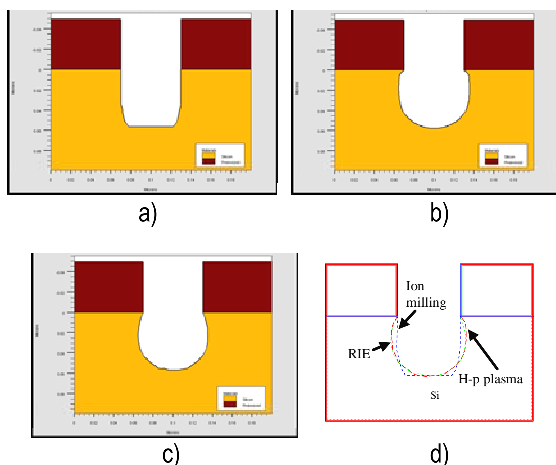
Φιγυρε 4. Χομπαρισον ωετ ετχηινγ τψπεσ: βλυε λινε ισοτροπιχ; ρεδ λινε ανισοτροπιχ

Anisotropic etching solves the problem of lateral control. The laterally masked geometry of

the planar surface can be etched and a vertical profile can be easily made. Although it solves the problem of lateral etching, the process is not problem-free. The process is slow even in the fast etching direction of the plane (100) and consumes more time.

Despite its simplicity in controlling the etching, wet etching is not flexible and reliable process. A dry etching process is an alternative choise (Fig. 5)

Dry Etching has several significant advantages compared with wet etching: it is much easier to start and stop than simple immersion wet etching; less undercutting; better process control. Ion milling (Fig. 5) has two significant advantages compared to high–pressure plasmas: directionality and applicability. With RIE can be achieved much higher selectivity compared with with ion milling.



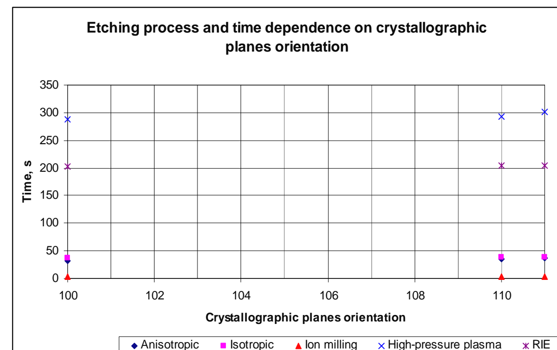
Φιγυρε 5. Δρψ ετχηινγ τψπεσ: α □ ιον μιλλινγ ετχη, β □ ηιγη–πρεσσυρε πλασμα ετχη, χ □ PIE ετχη; δ □ χομπαρισον δρψ ετχηινγ τψπεσ: βλυε λινε □ ιον μιλλινγ; ρεδ λινε □ πλασμα, γρεεν λινε □ PIE

Etching process is simulated in silicon depending on crystallographic planes orientation. Only (100), (110) and (111) crystallographic planes orientation are recognized in process simulator – ATHENA. Every etching process simulated 10 times and average time values is given in Table 1 and Fig. 6.

According to wet and dry etching process simulation results less lateral encroachment during region formation could be achieved using dry etching technology – ion milling. It has better directionality and time of etching process is less (~3s). The highest etching rate is reached in substance with crystallographic planes orientation (100). The lowest etching rate is reached in substance with crystallographic planes orientation (111), because there are 8 planes in substances with crystallographic planes orientation (111), which suspend etching process.

Ταβλε 1. Ετχηινγ προχεσσ ανδ τιμε δεπενδενχε ον χρψσταλλογραπηιχ πλανεσ οριεντατιον

	Crystallographic planes orientation			Etching type
	<100>	<110>	<111>	
Time, s	31,62	35,4	37,26	Anisotropic
	36,82	38,12	39,16	Isotropic
	2,81	2,97	3,56	Ion milling
	287,35	293,7	301,7	H-p plasma
	202,37	203,8	204,78	RIE



Φιγυρε 6. Ετχηινγ προχεσσ ανδ τιμε δεπενδενχε ον χρψσταλλογραπηιχ πλανεσ οριεντατιον

6. CONCLUSION

Unavoidable problems associated with wet etching process are: difficulties in etching at convex corners; difficult in preparing the mask with high precision; etch rate is very sensitive, it difficult to control both lateral and vertical geometries of the structure.

Using dry etching: it is possible to get less undercutting; better process control, directionality (Ion milling).

Less lateral encroachment could be achieved using dry etching technology – ion milling during region formation in MOS/CMOS technology.

The highest etching rate is reached in substance with crystallographic planes orientation (100). The lowest etching rate is reached in substance with crystallographic planes orientation (111).

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