THE INVESTIGATION OF FILTERS FOR REAL-TIME DATA ACQUISITION

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Abstract

Application of the real time digital filters in ultrasonic data acquisition system has been investigated. The work compares the digital filters (both programmable logic (CPLD/FPGA) both real time processing carried in PC) effectiveness when applied on ultrasonic signals. The investigation is cover filter, rounding noise and amplitude estimation performance. The acquisition system has been developed, including Xilinx Spartan 3E FPGA, high speed 10bit ADC and USB2 high speed interface. FIR filters have been developed and investigated experimentally.

Experimental results are documented and presented in tables and figures. Description and grounding of experimental techniques are presented.

1. INTRODUCTION

Development of ultrasonic inspection is raising demands for signal filtering since fields of application require higher dynamic range of the reception channel. Along with conventional, analog filter circuits, digital filtering is being extensively used. High gain values used, use of switched mode power supplies gives rise for electromagnetic interference (EMI). Ultrasound equipment should contain filters for EMI reduction [1].

Application of real time digital and/or analog filters in ultrasonic data acquisition system allows to have required processing immediately, during data acquisition process. The work will compare the digital (both programmable logic (CPLD/FPGA) both real time processing carried in PC) [2]. The investigation will cover filter rounding noise and AC response performance.

2. EXPERIMENTAL SYSTEM

The acquisition system has been developed for experimental purposes, including Xilinx Spartan 3E FPGA, high speed 10bit analog-to-digit converter (ADC) and USB2 high speed interface (Figure 1).

The core of the system is Spartan 3E Starter Board [3], obtained from Digilent, Inc. The Board is a self-contained development platform for designs targeting the Spartan 3E FPGA from Xilinx. It features a 500K gate Spartan 3E XC3S500E FPGA with a 32 bit RISC processor and DDR interfaces. A Xilinx Platform Flash for storing FPGA configurations, JTAG interface, 32MB Micron DDR SDRAM, 16MB Numonyx StrataFlash, 2MB ST Microelectronics Serial Flash, necessary Power Supplies regulators. For FPGA development in VHDL [4], Xilinx ISE web pack was used. Simulation was run on Aldec software Active HDL. Filter design and some simulations were run on MATLAB.

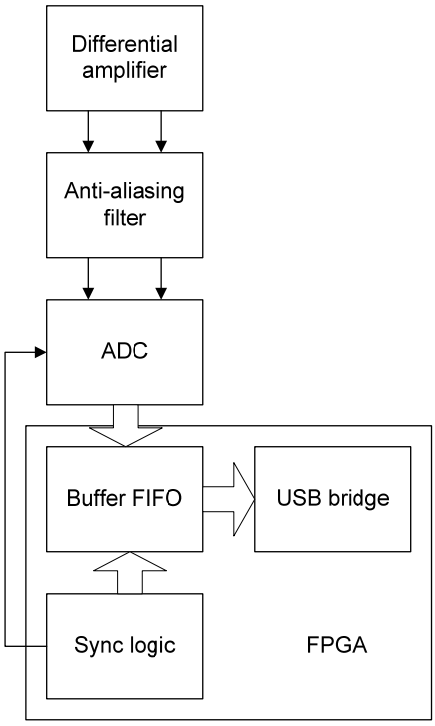

Fig. 1. Simplified system structure

The 100-pin Hirose FX2 connector is used for daughter board connection (Figure 2).

Daughter board contains coaxial connectors for analog signals supply, asymmetric to differential

converter and differential amplifier, anti-aliasing filter, high speed 10 bit ADC and USB2 high speed interface. Refer Figure 3 for daughter board circuit diagram.

Fig. 2. FPGA board with daughter board attached

3. DIGITAL NOISE INVESTIGATION

Sampled continuous wave (CW) amplitude extraction error standard deviation was used as noise evaluation. Sine wave correlation (SWC) [5] technique was used to extract the signal amplitude from acquired data set.

It was suggested to use common reference frequency source for excitation generator and sampling. Then frequency instability errors can be disregarded. In such case non-iterative fitting is used [5]:

$$U_c = \frac{\sum_{m=1}^{M}\left[\cos\left(2\pi f t_m\right)\cdot y_m\right]}{\sum_{m=1}^{M}\left[\cos\left(2\pi f t_m\right)\right]^2}, \quad (1)$$

$$U_s = \frac{\sum_{m=1}^{M}\left[\sin\left(2\pi f t_m\right)\cdot y_m\right]}{\sum_{m=1}^{M}\left[\sin\left(2\pi f t_m\right)\right]^2}, \quad (2)$$

$$U_{DC} = \frac{\sum_{m=1}^{M} y_m}{M}. \quad (3)$$

Then the magnitude and phase:

$$U = \sqrt{U_c^2 + U_s^2}\ , \varphi = \arctan\left(\frac{U_s}{U_c}\right). \quad (4)$$

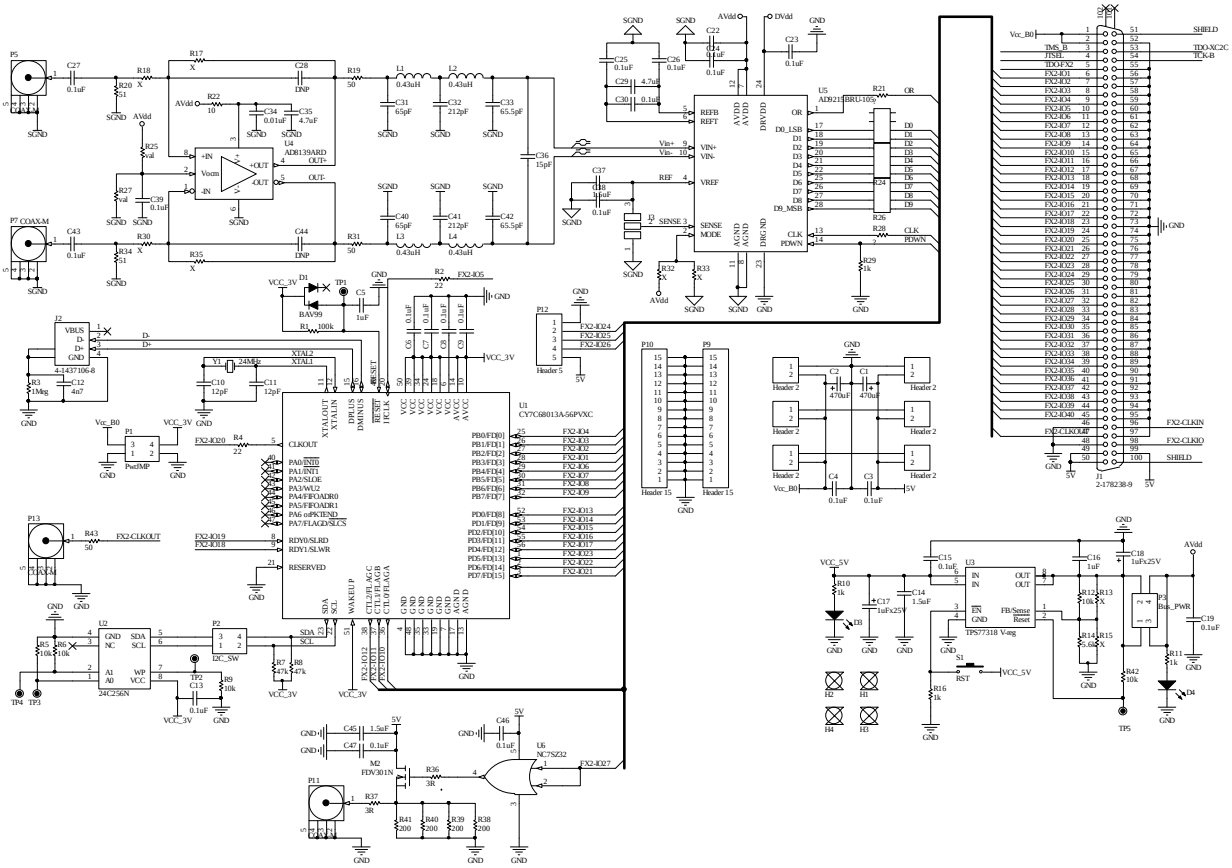

Fig. 3. Daughter board circuit diagramm

The SWC technique has been implemented for measured signal amplitude and phase estimation in data acquisition module. Experiments were repeated 1000 times and amplitude obtained in every cycle was accumulated and then standard deviation calculated.

Following system operation modes wre investigated:

1. 1 MHz CW signal acquired using 100 MHz sampling frequency and 10 bit ADC. Analog signal was passed through anti-aliasing filter. Signal stored in 8k memory.

2. Same 1 MHz CW signal acquired using at 100 Ms/s sampling frequency and 10 bit ADC with preceding anti-aliasing filter. But then was decimated to 10 Ms/s and stored in 8k memory. Anti-aliasing filter is used during decimation and stored as 10 bit.

3. Same 1 MHz CW signal acquired using at 10 Ms/s sampling frequency, 10 bit ADC with preceding anti-aliasing filter and stored in 8k.

Experiments were carried out in MATLAB. System input noise density was varied. Results where quantisation err was not taken into account are presented in Figure 4.

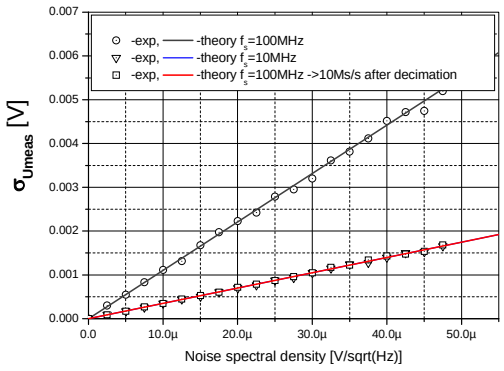

Fig. 4. Measured voltage standard deviation vs. electronics noise spectral density

It can be concluded that only filter bandwidth is influencing errors obtained. Therefore, keeping record length 8k gives same filter bandwidth for 10 Ms/s case and wider bandwidth for 100 Ms/s case.

Then quantisation was applied to evaluate the quantisation noise influence. In order to keep the quantisation noise as much random, carrier frequency was varied and kept as a fractional number of sampling frequency. Also, small amount (10 nV/sqrt(Hz)) of electronics noise was injected to simulate the real case. Results are presented in Figure 5.

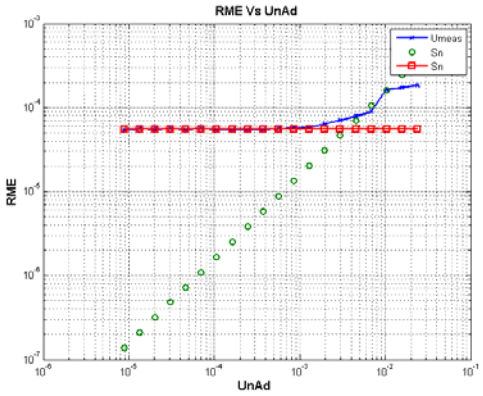

Fig. 5. Measured voltage standard deviation vs. quantisation noise standard deviation

ADc resolution was varied from 4 to 16bits and resulting quantisation noise standard deviation evaluated as:

$$U_{ADCnRMS} = \frac{U_{FS}}{2^K \sqrt{12}}, \qquad (5)$$

where K is ADC bits number, U_{FS} is the ADC full-scale range.

It can be concluded that ADC quantisation noise should match the electronics noise: otherwise noise statistics is distorted (see the upper part of the curve on Figure 5); also, there no need for further increase of ADC resolution since electronic noise starts to dominate (see the lower part of the curve on Figure 5 – there is no improvement in noise performance).

4. DIGITAL FILTERS INVESTIGATION

Digital filters were implemented in FPGA and testing signals acquired using acquisition system developed. Filter AC response was measured passing chirp signal through the filter. Using the spectra of signal supplied to filter and at the filter output filter AC response was obtained:

$$T_{filt}(j\omega) = \frac{S_{out}(j\omega)}{S_{in}(j\omega)}. \qquad (6)$$

Refer Figure 6 for signal magnitude spectrum used for testing.

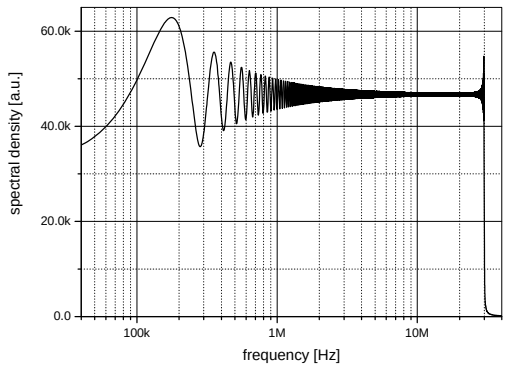

Fig. 6. Test signal spectrum

AC response for 39 taps FIR equiripple filter is in Figure 7.

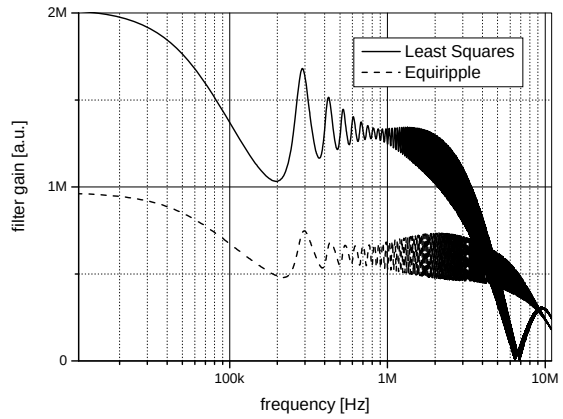

Fig. 7. FIR filters AC response

Filter cutoff frequency was 4.4MHz and stopband frequency was 9MHz with stopband attenuation 64dB (demanded by 10bit decimation from 100Ms/s to 10Ms/s) and it had 42 taps.

Another filter (Figure 7) had same cut-off frequency and stopband frequencies and attenuation but it was designed as least squares filter.

5. CONCLUSIONS

Application of digital filters in real time non-destructive testing ultrasonic systems is favoured nowadays. But possible artefacts are the penalty for digital processing advantages. Design of the filters require both high designer qualification both efforts in fighting such issues as saturation, abrupt degradation of the signal.

References

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