DESIGN AND SIGNAL PROCESSING OF A ECG RECORDER

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Abstract

The paper presents an analysis on data input/output methods, standards for radio-communication in body sensor networks.

Long time digital data recordings in ambulatory devices have become possible today with the presence of high capacity flash memories.

In the second part a use-case scenario for remote monitoring of ECG and pulse rate is presented. To demonstrate the use of intelligent Bluetooth ECG is employed in described scenario.

1. Introduction

The modern technology offer far greater opportunities they can be easily programmed either online by connecting the device to a PC using Bluetooth technology or offline by inserting a pre-configures flash card. Wireless communication eliminates data transmission cable and allows to display real time ECG, in this way the appropriate electrode placement can be checked anytime even during the ECG session. The measurements are stored on a conventional SD/MMC flash card to avoid data loss. The ECG storage quality (diagnostic, holter, rhythm) and the size of the memory card can be choose in order to meet the user's needs and achieve the best results.

2. Main text

In this context, data logging has a critical importance to make the patient's health history available to the health care provider. In implementing such patient treatment and monitoring equipments, researchers can design power-full medical devices with embedded processors that are easier to use, accessible and affordable. Implementation begins with the physiological interface to collect the signals from the human body. Using required front-end solution for essential signal conditioning, processor can perform further digital signal processing, measurements, recordings and analysis to monitor patient condition. As well as short-term measurements long-term measurements can be recorded in massive data storage and they can be transferred to a computer workstation for advanced analysis. Over the last two decades, researches have studied on developing some portable physiological data logging systems consisting of various analog signal conditioning and digital data processing solutions with different data recording capacities. These systems have been used generally in Electrocardiography (ECG) studies to detect infrequent cardiac arrhythmias or transitory cardiac function abnormalities. Several system designs have been described in this context. Some of them achieved the performance of commercial Holter recorders, systems that are named after an ECG recorder developed by N.J.Holter (1961), regarding the portability and nonvolatile data storage capacity. As a result of the developments in solid-state technology, researchers presently can implement such systems in a small and light structure with huge capacity of data storage. For instance, they can record the samples of physiologic signals in a flash memory card, Multi Media Memory Card (MMC) or Secure Digital Memory (SD) card. They can easily transfer the recorded data to a computer workstation for advanced signal analysis.

In this chapter we described such a microcontroller-based recorder design. It can be used as a reference model to build portable data logging systems. The design is powered by a NiMH battery. It integrates a microcontroller and its interfaces including a front-end unit for bio-signal conditioning. It provides recording capacity up to 1GB and sampling rate up to 1 kHz. Thus, it can be used for logging the data related to the various bio-signals. It includes off-the shelf components and can be easily built with inexpensive components including an embedded microcontroller, PIC 18FXXX, from Microchip family. In this case, we used it to get the 500 Hz rated samples of ECG signal and evaluate them for R-wave peak detection in QRS complexes, by using an on-line procedure. The system measure the interbeat times between the consequtive peaks, and records them into a file in the MMC/SD card recording media.

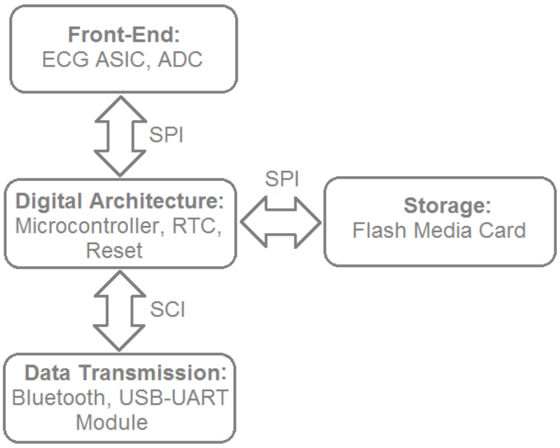

Figure 2-1. ECG Recorder Telemedicine System Block Diagram

The main function of this system is to acquire, store and transmit the ECG signals and provide mobility to the patient in two operation modes. First, in on-line transmission mobility is subject to a limited space, determined by the Bluetooth device class. Second, off-line acquisition is available through Holter operation mode. Therefore, this technology primarily designed for long-term usage in both modes [3].

Front-End: This block is for signal conditioning and digital conversion.

The function of this OEM Application Specific Circuit (ASIC), is to condition ECG signals from the electrodes. It also has the following characteristics: built-in pacer pulse detector, filtered lead-off for each electrode, programmable input offset for each channel, selectable reference electrode, on-chip RF filtering on all inputs and built-in self-test capability. This ASIC is configured through serial peripheral interface (SPI).

ADC: Digital conversion of the ECG differential channels is achieved through Analog Devices' analog to digital converter AD7716BS [1], with 4 independent and simultaneous delta-sigma sampling channels with 22 bits resolution. This ADC has 3 configurable sampling frequencies: 250, 500 and 1000 Hz. Samples from each channel, including channel and device address, are storied in 32-bit registers for later transmission. This device signals each end of conversion trough a pin connected to the microcontroller [11].

Digital Architecture: This stage is constituted by three main components: microcontroller, a real-time clock (RTC) circuit and a reset circuit. A microcontroller is used for setting the configuration of peripheral devices, processing and storing digital data acquired by the front-end, and establishing communication with local stations or APs through Bluetooth or USB. When the flash memory card is used, most of the processing time of µC is employed to update the FAT16 information in RAM and to communicate with the card. Therefore, the memory card and the front-end are connected to the µC through two different serial interface to ensure independence of the acquisition and storage process. Also, the end conversion pin of the ADC was connected to a high priority external interrupt to ensure that every set of samples was received with as little delay as possible. This set of samples is buffered awaiting its storage in the card. The 22-bit samples provided by the ADC can be stored and/or transmitted in both a 22-bit or 16-bit format, that is, data can be preprocessed in the µC to reduce storage and data rate requirements [1].

RTC: serial real-time clock used is a low-power clock/calendar with I2C bus interface for data transfer. The clock/calendar provides seconds, minutes, hours, day, data, and year information for recording identification purposes. Reset is used as a supervision circuit providing circuit initialization and timing supervision for the µC, to generate a power-on reset and power supply monitoring [4].

Storage: In this stage, collected data is stored in a flash memory card using FAT16 file format. Therefore, the memory card can be removed from this block for data retrieval in any computer-based platform. Each acquisition produces a new file with a simple protocol structure including sampling rate and lead configuration. Communication between the memory card and the µC is established through SPI bus. In the prototype, three different memory cards were tested since they share a common communication protocol: Multimedia Memory Card (MMC), Secure Digital Card (SD) and TransFlash [2].

Data Transmission: Two independent serial communication protocols are proposed: USB and Bluetooth. The four line SCI communication (RX, TX, RTS, CTS) go through a quad channel digital isolator.

Two AA batteries provide power to the model. A 95% efficiency step-up switching converter is used to generate 3.3V for system component. Exhaustive battery life-time measurement has not been carried out for all the operations modes. For a design estimate we considered the worst case for minimum battery life-time.

This condition occurs in two cases: Holter mode, witch includes the SD and real-time transmission, witch includes the Bluetooth module. In both cases, two 2500mAh AA batteries were assumed as power supply for the system.

In Holter mode, calculations were made using maximum current during memory writing and maximum and minimum writing times according to manufacturer's specification for both MMC and SD cards. A preliminary estimate suggests that battery lifetime should be at least 25 hours for MMC and 20 hours for SD cards.

3. Illustrations

Secure Digital Cards (SD) / Multimedia Memory Card (MMC), are used to hold information in many common electronic devices. SD/MMC cards can operate three different communication modes: one bit SD mode, four-bit SD mode, and SPI mode. SPI is a more basic protocol and it is widely supported by many microcontrollers.

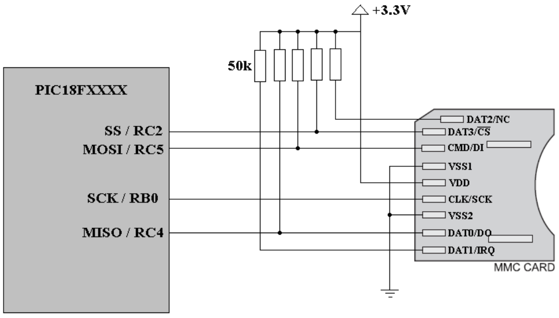

Figure3-1. Wiring Diagram for an SD Card

An SD card has 9 pins. Only 7 of these pins are used to communicate with an SD card in SPI mode. SD require between 2 and 3.6 VDC. In this case, I use power supply to provide 3.3 VDC to both the PIC and to the SD card. 50k pull-up resistors are essential, even for the pins that are not being used for SPI communications. Note that pull-up resistor should not be used on the clock line [5].

From Table 3-1, it is apparent that many SD Card pins are dual-purpose [6]. SPI is distinct from the 1-bit and 4-bit protocols in that the protocol operates over a generic and well-known bus interface, Serial Peripheral Interface (SPI) [7]. SPI is a synchronous serial protocol that is extremely popular for interfacing peripheral devices with microcontrollers. Most modern microcontrollers support SPI natively high data rates. The SPI communications mode supports only a subset of the full SD Card protocol.

Pin	Name	Function (SPI Mode)
1	DAT3/CS	Chip Select/Slave Select (SS)
2	CMD/DI	Master Out Slave In (MOSI)
3	VSS1	Ground
4	VDD	Supply Voltage
5	CLK	Clock (SCK)
6	VSS2	Ground
7	DAT0/DO	Master In Slave Out (MISO)
8	DAT1/TRQ	Unused or IRQ
9	DAT2/NC	Unused

Table 3-1. SD Card Pin Assignments

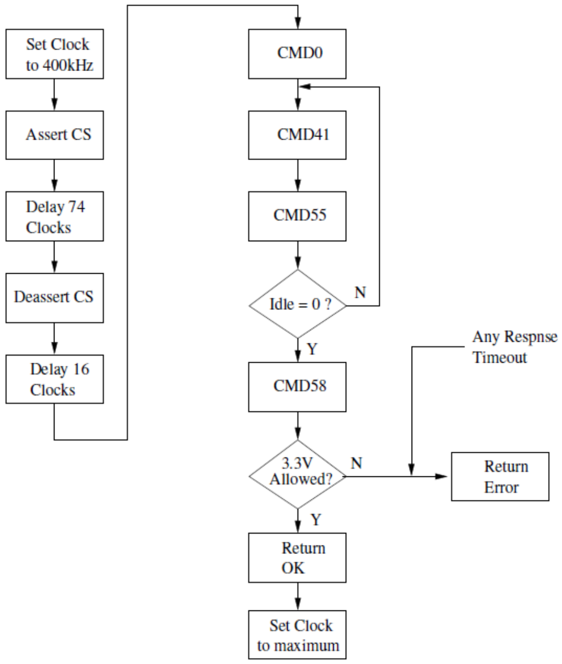

Figure 3-2. SD Card Initialization Sequence

The initialization sequence is characterized in the flowchart Figure 3-2 [8].

SD cards require a specific initialization sequence. Parts of the initialization sequence are historical, and other parts are required for backward and forward compatibility. MMC and SD are not substantially different, the primary difference from a software point of view is in the initialization sequence. Card initialization starts by setting the SPI clock to 400kHz.This is required for compatibility across a wide range of MMC and SD Cards [9]. Next, at least 74 clocks must be issued by the master before any attempt is made to communicate with the card. This allows the card to initialize any internal state registers before card initialization proceeds. Next, the card is reset by issuing the command CMD0 while holding the SS pin low [10]. This both resets the card and instructs it to enter SPI mode. Note that while the CRC, in general, is ignored in SPI mode, the very first command must be followed by a valid CRC, since the card is not yet in SPI mode. The CRC byte for a CMD0 command with a zero argument is constant 0x95. Next, the card is continuously polled with the commands CMD55 and ACMD41 until the idle bit becomes clear, indicating that the card is fully initialized and ready to respond to general commands. Next, the command CMD58 is used to determine if the card supports the processor's operating voltage. CMD58 returns a bitfield containing the allowed operating voltage ranges, typically between 2.7V and 3.6V. It is assumed that the MSP430 is using a voltage supply of 3.3V. Finally, the SPI clock is set to the maximum rate allowed.

4. Conclusion

SD Cards offer a cost-effective way to store large amounts of data in a removable memory storage device. The simplicity of the SD Card protocol and the flexibility in interfacing with these devices makes them ideal for use with small microcontrollers. Combined with the low-cost, low power and its advanced featured like onboard DMA and SPI, a fast and low-overhead complete data logging solution can be implemented quickly and inexpensively. Additional application-level support for a file system such as FAT16 can extend the usefulness of this solution even further.

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