DEMODULATOR FOR SATELLITE TV SIGNALS

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Abstract

In this paper the demodulator of satellite television signals formed by standard DVB-S2 is considered. A detailed block diagram and description of the blocks are given. A mathematical description of the algorithms used for carrier phase recovery is given. A parametric analysis of these units is done.

1. INTRODUCTION

One of the main problems in digital satellite TV receivers is the carrier phase recovery. The reason for this is the fact that the DVB-S2 receiver should operate at very low CNRs and consumer-type DVB-S2 receivers typically use low cost oscillators, which introduce a large initial carrier frequency offset. An additional problem occurs when operating in Adaptive Coding and Modulation (ACM) mode in which modulation can change at any package.

In the satellite TV receiver, the radio signal with intermediate frequency obtained after the second frequency conversion is digitized and transmitted in the form of samples with the symbol rate. It is important to take samples at the right moment, because otherwise the influence of inter-symbol interference increases. For this purpose the position of the maximum peak is necessary to be accurately determined. This is achieved by usage of the symbol timing recovery circuits.

It is known that the maximum noise immunity is provided by coherent demodulation, in which the carrier frequency and carrier phase are required to be known. Therefore it is necessary to perform accurate recovery of the carrier frequency and carrier phase and for this purpose the carrier frequency and phase recovery circuits are used.

In systems in which seeks simplicity of the scheme implementation and sustainability usually non-coherent or kvazi-coherent demodulation are used. Since in this type of demodulation the decision is based on the phase shift, which itself does not depend on current state of phase, then only carrier frequency recovery is performed.

It is generally assumed that in satellite-receiver channel the attenuation is a constant, depending only on the carrier to noise ratio at the receiver input. The other effects (clock and frequency errors, phase noise, etc.) are usually counted as occurred in the receiver. Errors in timing recovery are obtained mainly because of the instability of the generator providing a clock frequency for sampling. The main reasons for the carrier frequency errors are the instability of the generator used in low noise converter (LNC) and the Doppler effect caused by the movement of geostationary satellites. The main source of phase noise is a radio-frequency generator in LNB, and the influence of the tuner can be ignored.

The aim of this paper is to provide background information for digital processing in the second generation satellite TV receiver, and to examine the effectiveness of systems for carrier phase recovery.

2. BLOCK DIAGRAM OF DVB-S2 DEMODULATOR

Fig. 1 shows a block diagram of the demodulator of the satellite signals formed according to the standard DVB-S2. Incoming signal with intermediate frequency (IF) is digitized by high speed Analog to Digital Converter (ADC) and submitted to the block Digital Down Converter (DDC). The sample rate F_S in the ADC is chosen such that to satisfy the Nyquist criterion and to be k times larger than the symbol rate R_S of the received signal, where k is an even number. In DDC a two-step process is implemented, in the first one samples from the ADC are multiplied by a periodic sequence, as a result yielding two complex I and Q signals with a frequency equal to half of the input signal frequency

(F_s / 2). In order to avoid unwanted high-frequency components, the resulting signals pass through a low pass filter, and then subjected to a frequency reduction.

In the second step of processing in DDC, the signal passes through a programmable frequency reducer, consisting of digitally controlled oscillator (NCO) and a complex multiplier. NCO is controlled by coarse carrier frequency recovery block. The signal obtained by the complex multiplication is fed to Sample Rate Converter (SRC), which consists of Polyphase filter with a Finite Impulse Response and suitable decimator. Its purpose is to transform the samples rate so that the rate of output samples is an integer times bigger the real rate of the samples.

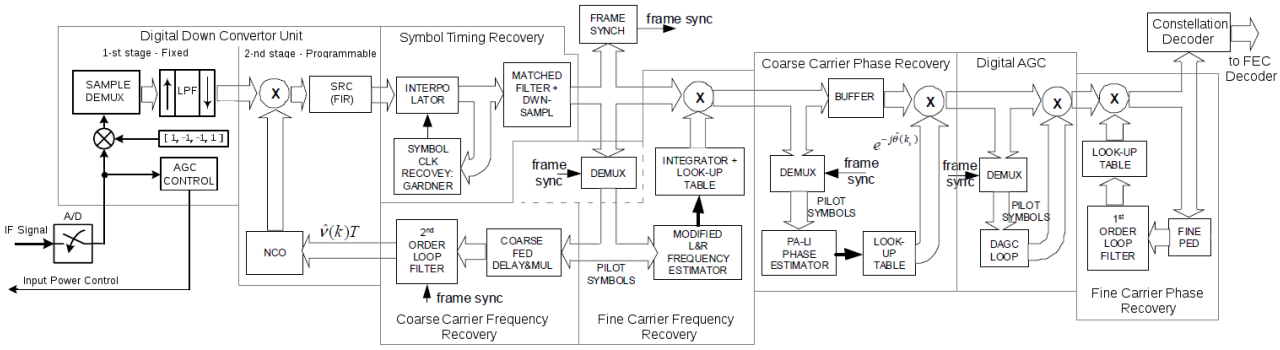

Fig. 1. Block Diagram of DVB-S2 Demodulator

In order to ensure that the signal level of the ADC input will be in its dynamic range, in the DDC is provided a control unit of the system for automatic gain control (AGC) of the IF amplifier.

The signal obtained at the output of the DDC is fed to the Symbol Timing Recovery (STR) block. It consists of a cubic interpolator with Farrow's structure, Gardner Timing Error Detector (TED), as well as the second order filter connected in a feedback circuit. The main task of the interpolator is to calculate the output samples $y(kT_i)$ on the basis of the input samples $x(mT_s)$ and the error information (m_k и μ_k) coming from sub-blocks "Symbol Clk Recovery; Gardner ". When with T_s is denoted the period of input samples, and with T_i the period of interpolated output samples.

The sub-block "Symbol Clk Recovery; Gardner" has several functions, namely: determining the timing error by using Gardner's algorithm, proportional integration through first order loop filter and management of the interpolator. The main advantage of the Gardner's algorithm is its independence from the transmitted information and frequency error. The bandwidth of the filter in the feedback determines the time for synchronization as well as accuracy during operation in search and track modes. For each input sample control device calculated base point m_k and relatively delay μ_k, in order to obtain the corresponding interpolated values.

The last sub-block of the symbol timing recovery system is "Matched Filter + Dwn Sampl." Its task is to ensure a coherent filtering and appropriate decreasing of the frequency of samples generated by STR cycles.

The package synchronization is done by searching the header of the physical layer by suitable correlator, operating symbol by symbol. By using differential decoding correct packet synchronization is possible even in the presence of a large carrier frequency error. The block is implemented through a shift register consisting of 89 elements, divided into two groups - the first (25 elements) is connected to the symbols indicating the start of a packet (SOF), and the second (64 pieces) - with the symbols of the physical layer (PLS). There are 57 connections to the 89 elements of the shift register, as in the second half only 32 of the 64 symbols are known in the receiver. The contents of the shift registers is multiplied by the relevant coefficients and then summed. The maximum value of the outputs of the two adders, whose signal is fed to a peaks detector is obtained when the whole header of the physical layer occur in the shift register.

In DVB-S2 a two-layer system for carrier frequency recovery is used. The coarse carrier frequency recovery is initially performed, by using the second order feedback loop, based on the frequency error detector which use "delay and multiply" (D & M) algorithm. For fine carrier frequency recovery a

modified version of the Lewis and Regianini (L & R) algorithm is used, which is boiling down to averaging the sums of autocorrelation functions for many neighboring fields before calculating the argument of the function. Detailed information, block diagrams and mathematical description of the carrier frequency recovery are given in [9].

The carrier phase recovery can be achieved by single-layer (for QPSK and 8PSK modulations), or dual-layer (for APSK modulations) system. In the coarse carrier phase recovery (applied to any received signals) for evaluation of phase error is used forward link system based on the maximum likelihood (FF-ML) algorithm, using pilot fields. In this technique is carried out finding of the phase trajectory at the time of the data symbols by using a linear interpolation on two consecutive / neighboring pilot fields as for each pilot field was calculated average phase.

The separation of pilot signals is done by the demultiplexer (Demux), while in the block "Pa-Li Phase Estimator" is carried out a mathematical processing and the calculation of the error signal corresponding to the phase during the information signal. Thus, obtained signal is fed to the look-up table, which makes a comparison of the error signal with the coefficient corresponding to an obtained phase error. For the duration of corresponding processing, the signal is stored in the buffer.

For fine carrier phase recovery a feedback system, based on algorithm for determining of the phase error by raising the input signal to the Q-degree (Q = 3 for 16APSK and Q = 4 for 32APSK) is used. The algorithm is applied directly to the transmitted information. When 16 APSK / 32APSK constellations is raised on third / fourth degree and then phase shifted on 0 / π / 4 rad, the inner points of the original constellations are collected in the center, while the outer points form a QPSK constellation.

Raising of the input constellation on the corresponding degree, its phase shifting, as well as the mathematical processing of the resulting signals is performed in the block "Fine PED". The error signal from the output of the block passes through the first order filter and fed to a look-up table in which a comparison of the error signal and the phase error is performed.

Typical for this algorithm is its simplicity as well as the fact that it is relatively insensitive to the amplitude errors, because of the operation "cutting of quadrant". The presented algorithm is not suitable for use in the demodulators with a "hard" decision.

Block digital Automatic Gain Control (DAGC) is placed after coarse carrier phase recovery system. Its purpose is to change the levels of the incoming symbols to those of the reference constellation. This is required because the decoder needs precise "soft" information about the distance between the received symbol and reference point from the constellation. For this purpose, the pilot symbols are separated in the Demux and fed to the block DAGC Loop for evaluation of their amplitude. Based on this evaluation, the appropriate coefficient is selected, with which the data symbols are multiplied.

3. MATHEMATICAL DESCRIPTION OF THE STUDIED ALGORITHMS FOR CARRIER PHASE RECOVERY

The phase estimation in the method of coarse carrier phase recovery is obtained by the using of L_p number of samples from the output of the matched filter corresponding to the pilot signals and by applying the following mathematical operation:

$$\widehat{\theta}^{(p)} = \arg\left(\sum_{k=0}^{L_p-1} \left\{ c^{(p)}(k) * z^{(p)}(k) \right\} \right) = \theta + N_I \quad (1)$$

The second equality is valid at high CNR, as NI denotes Gaussian noise with zero mean value corresponding to the phase evaluation and having dispersion

$$\sigma^2_{N_I} \cong \sigma^2_{\widehat{\theta}^{(p)}} = \frac{1}{2L_p E_S / N_0} \quad (2)$$

In order to ensure that the phase will not grow beyond the interval [-π; π] system to determine the total phase evaluation is used. If with *l* denote the number of the pilot evaluation, the final unwrapped evaluation $\theta'^{(p)}f(l)$ is calculated on the basis of $\theta'^{(p)}(l)$ by the expression

$$\widehat{\theta}_f^{(p)}(l) = \widehat{\theta}_f^{(p)}(l-1) + \alpha SAW[\widehat{\theta}^{(p)}(l) - \widehat{\theta}_f^{(p)}(l-1)], \quad (3)$$

where $SAW[\Phi]=[\Phi]^{+\pi}_{-\pi}$ is a saw tooth non-linearity that reduces Φ to the interval [-π; π], a α e is a parameter in the range $0 \le \alpha \le 1$, which is usually chosen to be equal to 1 ($\alpha = 1$).

The cycle slip probability P_{CS} is determined by the expression

$$P_{CS} = \Pr\{\hat{\theta}^{(p)}(l) - \hat{\theta}^{(p)}(l-1) > \pi\} = \\ = 2\int_{\pi}^{\infty} \frac{1}{\sqrt{4\pi\sigma_{N_I}^2}} e^{-\frac{x^2}{4\sigma_{N_I}^2}} dx \quad (4)$$

The system for fine carrier phase recovery uses an algorithm for determining the phase error by raising the input signal on the Q-th degree. For the given algorithm estimated by the detector phase error has the form

$$e_{\phi}(k) = \mathrm{Im}\{q(k).(sign[\mathrm{Re}\{q(k)\}] - \\ - jsign[\mathrm{Re}\{q(k)\}])\}, \quad (5)$$

where

$$q(k) = \begin{cases} [z(k)]^3 & за\ 16APSK \\ [z(k)]^4 e^{j\frac{\pi}{4}} & за\ 32APSK \end{cases} \quad (6)$$

4. PARAMETRIC ANALYSIS OF THE STUDIED ALGORITHMS

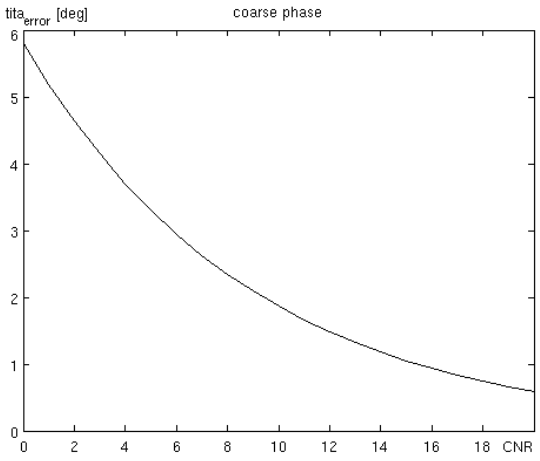

Figure 2. Dependence on phase estimation of CNR

The dependence of the estimated phase error on the carrier to noise ratio for the system for coarse carrier phase recovery is shown on Fig.2. During the simulations it is accepted that there is no residual frequency error, and the number of pilot signals in one sequence is: L_p = 36. From the figure it is seen that with the increase of CNR the dependence of the established phase error becomes weaker, while for large values of CNR it has a value close to 0. The figure allows determining the estimated phase error by the system for a given value of the CNR. In the working range for the DVB-S2 receivers (9 dB ≤ CNR ≤ 12 dB) the value of the estimated phase error varying in the interval from 2,1° to 1,5°.

Fig. 3 shows the influence of the ratio of energy per symbol to the Spectral Noise Density (E_S/N_0) to the cycle slip probability in the system for coarse carrier phase recovery for different number of pilot signal in the pilot block.

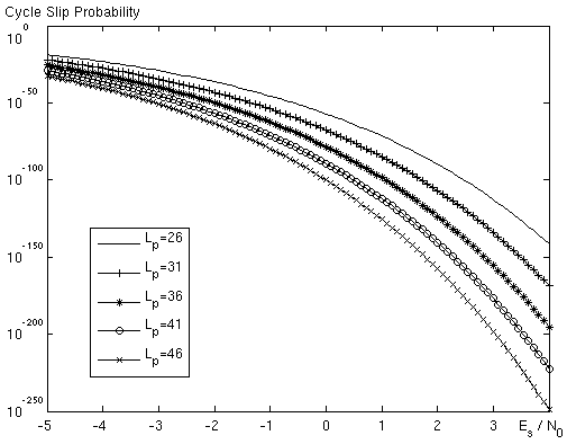

Figure 3. Dependence on cycle slip probabilitay of E_b / N_0

From fig. 3 it is seen that by increasing the number of the pilot signals cycle slip probability decreases. The cycle slip probability for different values of the E_S/N_0 and L_p are given in Table 1. From Table 1 it is seen that even when the E_S/N_0 = -2 dB the cycle slip probability is very small, which allows the given algorithm to be widely used in satellite television receivers from the second generation.

Table 1. cycle slip probability

E_S/N_0	L_p=26	L_p=31	L_p=36	L_p=41	L_p=46
-2 dB	10^{-36}	10^{-43}	10^{-50}	10^{-57}	10^{-63}
0dB	10^{-57}	10^{-68}	10^{-78}	10^{-89}	10^{-100}
2 dB	10^{-90}	10^{-107}	10^{-124}	10^{-141}	10^{-158}
4 dB	10^{-142}	10^{-168}	10^{-196}	10^{-222}	10^{-249}

Fig. 4 shows the dependence on the variation of estimated phase error of the E_S/N_0 at coarse carrier phase recovery system, for different values of the residual frequency error. During the simulations it is accepted that L_p = 36. The figure shows that when reducing residual frequency error below 10^{-3} its influence on the variance of estimated phase error is minimal.

The dependence on the average value of the estimated phase error, of the CNR, at the fine carrier phase recovery system for different modulations is given in Fig. 5. From that figure can determine the value of the estimated phase error depending on

the CNR at the input of the receiver. In the working range for the DVB-S2 receivers the value of the estimated phase error varying in the interval from 3,975° to 3,945° for 16APSK modulation and from 1,516° to 1,5° for 32APSK modulation.

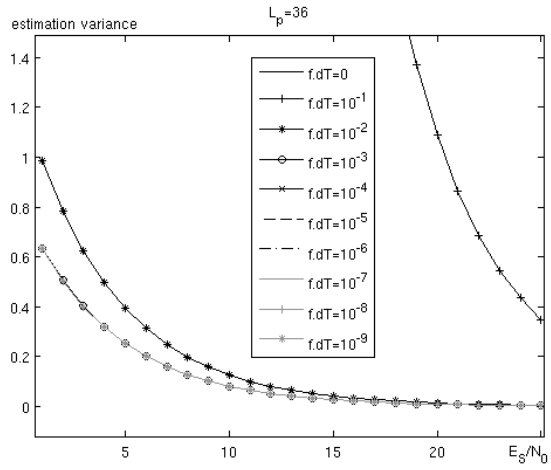

Figure 4. Phase estimation variance vs frequency offset

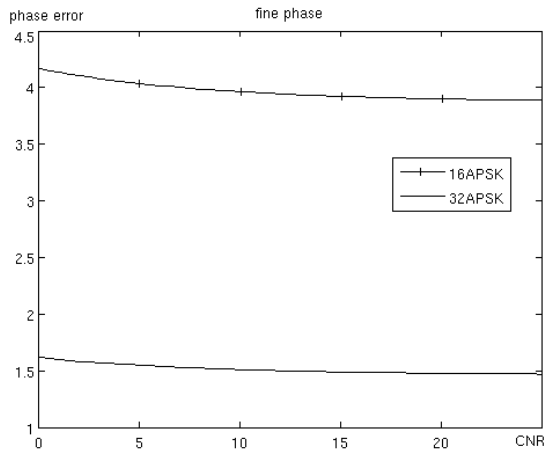

Figure 5. Dependence on average phase estimation of CNR

5. CONCLUSION

Presented in this paper mathematical models and graphical dependencies of the carrier phase recovery systems makes possible to determine the estimated phase error, its dispersion and the cycle slip probability, depending on the carrier to noise ratio as well as the number of pilot symbols in a block and residual frequency error.

6. APPENDIX AND ACKNOWLEDGMENTS

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