Low Power Testable Buffer Logic

Goran Z. Panić[1] and Mile K. Stojčev[1]

Abstract – **This paper describes a testable low power buffer logic circuit suitable for implementation as interface between processing stages in pipeline organized VLSI microprocessor systems. Buffer logic is composed of chained scan cells. Two types of low power scan cells, simple scan cell and scan macrocell, are introduced. Performance concerning propagation delay, area and power consumption for both type of cells implemented in three different technologies (0.35µm, 0.6µm, and 0.8µm) are given.**

Keywords – **Low power systems, Low power scan element, Design for test**

I. Introduction

Most modern electronic device and system designs are confronted today with the problem of delivering high performance with a limited consumption of electric power and possibility of testing [1]. High performance is required by increasingly complex applications in multimedia, wireless communications, cellular phones, laptop computers, instrumentation, industry, electromedicine, etc [2]. Low power consumption is required to achieve acceptable autonomy in battery powered systems and to extend the battery life in portable devices [3]. On-line VLSI ICs testing is necessity because permanent, transient and intermittent faults become dominant failure modes in modern VLSI ICs such as SoC designs [4]. Several low-power and testable design applications have been proposed [5] that are based on the idea of applying power management [6], and built-in possibility for testing circuits at chip [7]. All described solutions suggest the tradeoffs between energy consumption and possibility for testing ICs. This paper introduces low-power flip-flops that interface to processing stage in pipeline organized VLSI processor systems. Recognizing the fact that not all parts of VLSI IC may need to function each clock cycle we identify, firstly, all suitable candidate locations according to which we differentiate active and idle processing stages within the VLSI IC, and secondly, in all these candidate locations we insert testable low power buffer stages.

The rest of the paper is organized as follows. Section II is devoted to power reduction techniques. In Section III the structure of testable low-power buffer stage is described. In Section IV, performance of the proposed solution implemented in CMOS technology are given. Conclusion is given in Section V, and finally references are presented in Section VI.

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II. Power Reduction Techniques

A. Sources of Power Consumption in CMOS ICs

The three major sources of power consumption in digital CMOS circuits are [3]:

$$P_{avg} = p_t \left(C_L \cdot V_{dd}^2 \cdot f_{CLK} \right) + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd} \quad (1)$$

The first term represents the capacitive switching power, and is dominant source of power consumption in CMOS gate. Here, C_L is the loading capacitance, f_{clk} is the clock frequency, p_t is the possibility that the power consumpting transitions occurs and corresponds to the average number of transitions to clock cycle, and V_{dd} is the supply voltage. The second term is due to the direct-path short circuit current I_{sc}, and arises when a current flows from V_{dd} to ground through both NMOS and PMOS transistors during the rise and fall times (ramp times) of the input and output waveforms. Finally, leakage current $I_{leakage}$, which arises from substrate injection (diode leakage current) and subthreshold effects (subthreshold leakage current) is determined by fabrication technology considerations. The first two terms are dynamic sources of power consumption, i.e. they contribute to power only during transitions, while the third is static one.

B. Implementation of Low-Power Design

The implementation-level impact on low-power design (see Fig.1) can be categorized into system level, algorithm level, architectural level, circuit level, and process/device level [8], [9].

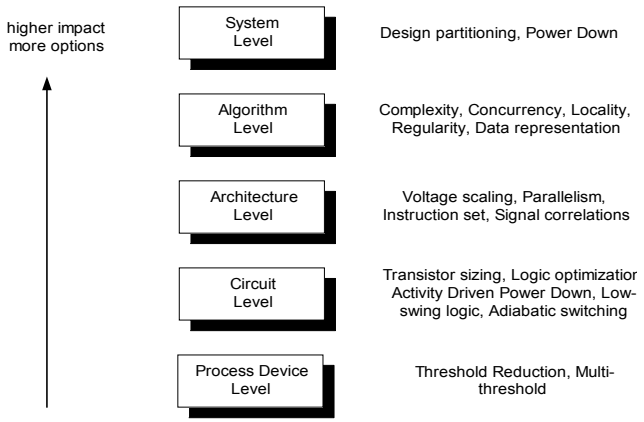

Fig.1. Implementation levels for power reduction

As highest, the system level strongly influences power consumption and distribution by partitioning system factors (for example heavy computation resources and large data storage devices are moved to the backbone server, but not in portable terminal devices). The algorithm level is key to power consumption and efficiency (creation of efficient algorithms is imperative). At architectural level we decide which hardware structure to implement, CPU, DSP, ASIC, ASIP, reconfigurable logic, etc. The circuit level can be explained as module level such as multiplier, memory, ALU, etc. The lowest process/devices level usually leads to voltage reduction.

C. Techniques for Power Reduction at Architectural-, and Circuit-Level in Microprocessor Design

In this paper all our efforts are concentrated towards the implementation of power reduction techniques at architectural-, and circuit-level design. At architectural level we consider the approach of disabling the activity of some building blocks when their states must not change, which reduce the energy consumed by logic circuits internal to the VLSI IC. In other words we shutdown inactive portions of the system. At circuit-level (logic-level) for CMOS technology, we concentrate on techniques aiming at reducing the average energy consumed in the datapath register during an operation. In order to achieve this, the storage elements such as flip-flops and latches must also be as simple as possible and satisfy various requirements of synchronous systems such as rigid timing constraints and low power dissipation. To be competitive, an electronic design must be able to deliver peak performance when requested. Nevertheless, peak performance is required only during some time intervals. Similarly, system components are not always required to be in the active state. The ability to enable and disable components, as well as of tuning their performance, is crucial in achieving energy efficient designs.

At architectural level many modern microprocessors have adopted two global strategies for power reduction. The first is called clock-gating. Figure 2 describes the clock-gating scheme. In this scheme the activation of clock for target flip-flops is controlled by enable signal that is asserted only when needed.

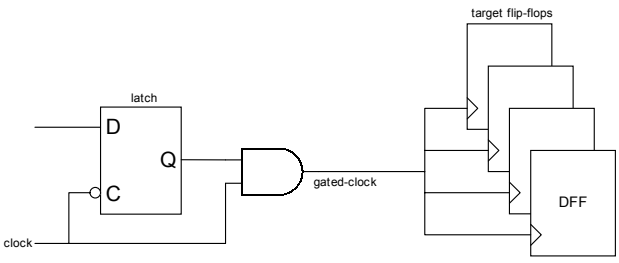

Fig. 2. Clock-gating scheme

The second suitable method for power saving is through data enabling. Data enabling implementation is shown in Fig. 3. The enable signal generates a data signal that indicates whether the current data is valid or not. This prevents input data updates for invalid data or an idle condition. In this paper we propose a solution based on the combination of data & clock enabling.

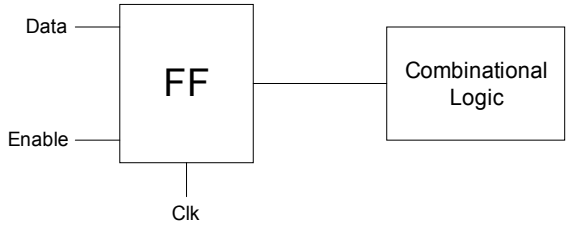

Fig. 3. Data enabling principle

Our choice for power reduction at circuit-level is based on the simplification of the flip-flop structure. In library-based design, power savings from the design of the cell libraries can come from device sizing and from restructuring of the logical and physical schematics of the cell. Device sizing for optimizing switching energy versus delay ensures better power efficiency [3]. The second way to optimize a cell library is the change the schematics of the most commonly used and most power hungry cells in the design. They typically consist of latches and master-slave flip-flops since these have clock needs which switch on at every clock edge. Figure 4 shows our approach of flip-flop redesign that gets rid of clock nodes while still maintaining functionality and performance. Thus it is advisable to replace more dissipative sequential cells described in [10] by more efficient one.

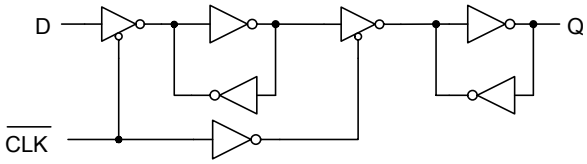

Fig. 4. Low power and low area D-type flip-flop

III. DESIGN FOR TESTABILITY

A. Our Choice for Testability

The reduction in VLSI feature size and increase in modern VLSI ICs has resulted in an abundance of on-chip interconnect and datapath resources, making on-line VLSI testing a necessity. Namely, transient and intermittent faults become a dominant failure mode in modern VLSI, so the widespread deployment of on-line VLSI testing technology has become crucial. A design process or philosophy that leads to good testability is *design for testability*. Here we consider scan testing method as an approach for synthesis of testable circuits.

B. Determining Candidate Locations

In order to implement the principle of testability it is necessary first to identify the suitable candidate locations. In Fig. 5 for a simple pipeline processor architecture, the candidate locations are indicated as shaded boxes.

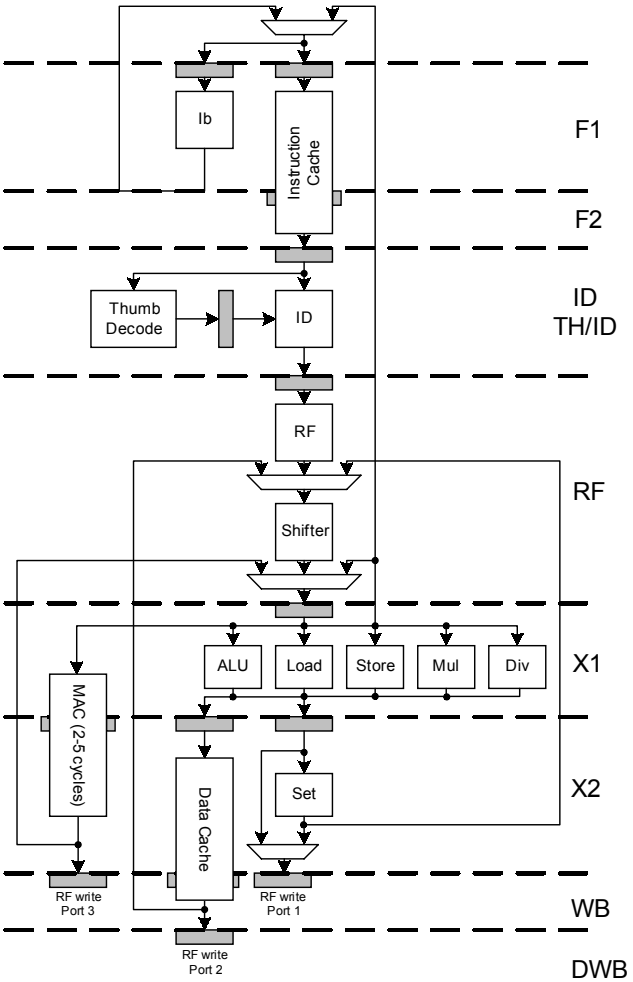

Fig. 5. Candidate locations for implementing testing

C. Scan Cell Implementation

For scan cell implementation we have used the following two types of low power scan cells:

- simple low power scan cell
- low power scan macrocell

The evaluation of the design was done using:

- 0.35µm, 0.6µm and 0.8µm technology [11] with supply voltage of 3.3V for propagation delay; and
- 0.6µm and 0.35µm technology for area and power dissipation

Let as note that, both the simple scan cell and the macrocell support concurrent execution of the following two independent activities:

a) normal operation of the tested logic

b) inputing of the test sequence

Having in mind the choice of cells available to the designer in [11] the D-flip-flop given in Fig. 4 was used as a basic building block of the simple low power scan cell and the low power scan macrocell. The schematics of simple scan cell and scan macrocell are given in Fig. 6 and 7, respectively.

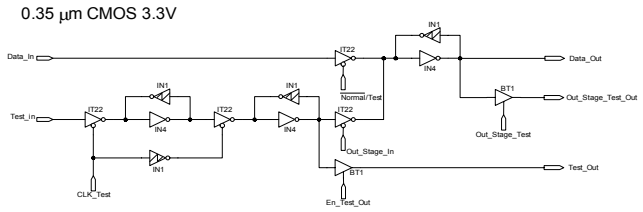

Fig. 7. Schematic diagram of simple low power scan cell

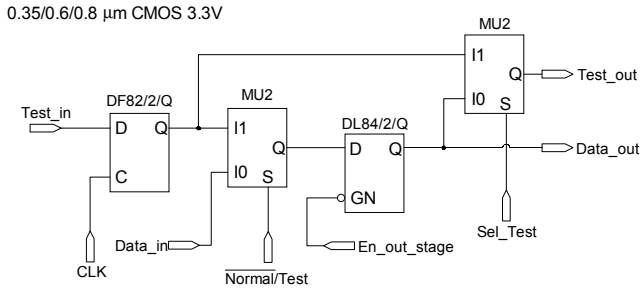

Fig. 8. Schematic diagram for low power macrocell

C. Scan chain implementation

Figure 9 shows a typical pipeline stage which consists of a combinational (tested) logic surrounded by a scan chain.

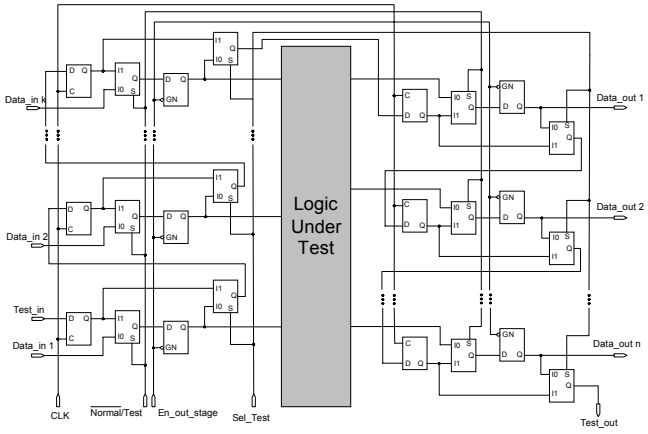

Fig. 9. Implemented scan method

Notice: Test chain is marked with bolded line

IV. PERFORMANCE

In Table I performance concerning simple low power scan cell and low power scan macrocell implemented in 0.35µm, 0.6µm, and 0.8µm technologies [11] with power supply of 3.3V are given.

Typical delays in the datapath involved by simple low power scan cell and scan macrocell for different technologies are given in Fig. 10

TABLE I
PERFORMANCE OF SIMPLE SCAN CELL AND SCAN MACROCELL

Architecture	Simple Low Power Scan Cell	Low Power Scan Macrocell
Technology	Data_in-to-Data_out delay (ns)	Data_in-to-Data_out delay (ns)
0,35 µm	0,51	0,82
0,6 µm	0,65	1,94
0,8 µm	1,55	5,05

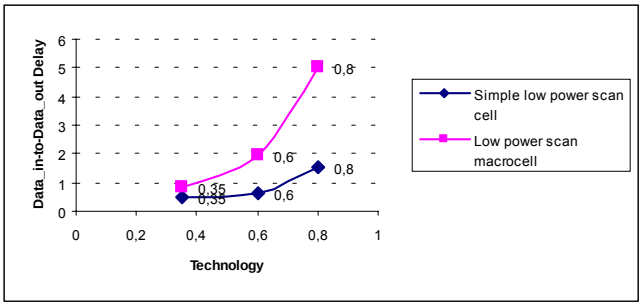

Fig. 10. Typical delay for different technologies

Performance evaluation related to simple scan cell and scan macrocell concerning area and power consumption of the both cells respectively are given in Table II.

TABLE II
PERFORMANCE CONCERNING AREA AND POWER CONSUMPTION

Type of Cells	Simple Scan Cell		Scan Macrocell	
Technology	Area ($mils^2$)	Power (µW/MHz)	Area ($mils^2$)	Power (µW/MHz)
0.35 µm	2,143	8,89	1,212	5,9
0.6 µm	7,19	43,19	3,66	14,4

Analyzing the results presented in Table I and II and Fig. 10 we can conclude the following:

1. With continuing decrease in feature size and the corresponding increase in chip density at the same operating frequency the power consumption decreases (see Table II)
2. Data demonstrating delay characteristics given in Fig. 10 indicate that simple scan cell in respect to scan macrocell involves smaller delay, but with technology scaling the delay difference decreases
3. Power consumption and area of scan macrocell is less than that of simple scan cell

Taking into account the previous consideration we propose the following choice: For technologies with size less than 0.35µm (future trends in CMOS semiconductor technology) the proposed scan macrocell structure has superior performance in respect to simple scan cell.

V. CONCLUSION

We have described two types of scan element design combining the benefits of low power and testability into a single high performance buffer stage intended for implementation into pipeline organized VLSI microprocessor system. Performance of the proposed scan cells were evaluated for three different technologies. This proposal, thanks to minimizing switching in combinational networks, has a significant impact on power consumption, and in addition, it allows testing the VLSI design in order to detect the presence of hardware failures induced by faults in the manufacturing processes or by operating stress.

VI. REFERENCES

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