Synthesis and Optimization of Quaternary Digital Electronic Systems and Circuits

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Abstract – **The principles and possibilities of synthesis and optimization of quaternary digital electronic systems and circuits are described and proposed in the paper. The general principles for synthesis of such systems are considered first. Then methods for synthesis of quaternary CMOS logic circuits are proposed and described. Finally, method for optimization of CMOS quaternary logic circuits is proposed and described. Some of computer simulation results confirming described methods and conclusions are given.**

Keywords – **Synthesis, Optimization, Quaternary systems and circuits, CMOS logic circuits, Computer simulation.**

I. INTRODUCTION

Good characteristics and advantages of multiple-valued (MV) digital electronic (logic) systems and circuits are created great interest for its practical implementation [1-4]. The greatest practical interest is for application of quaternary (where the basis is 4) logic systems and circuits and for implementation in CMOS technology [1-4].

The possibilities and methods of synthesis and optimization of quaternary digital electronic systems and circuits are considered in the paper. The general methods of design and synthesis of quaternary logic systems and circuits are briefly described firstly. Then one method for synthesis of CMOS quaternary logic circuits with any logic function is proposed and detailed described. Finally, method for optimization of CMOS quaternary logic circuits is proposed and described. All proposed principles and circuits and given results have been analyzed and confirmed by PSPICE simulation for one CMOS technology process [5]. Some results of the simulations are given in the paper.

II. SYNTHESIS AND DESIGN OF QUATERNARY LOGIC SYSTEMS

There are two standard methods for synthesis and design of MV logic networks and systems: fully MV systems and mixed systems [1-3]. So, quaternary logic networks and systems can also be fully quaternary systems and mixed systems. The fully quaternary systems and circuits will be considered here only.

The fully quaternary systems, as well as binary systems, can be synthesized by more methods, depending on basic logic components used: using max, min and unary operators (circuits); using operators of sum by module and product by module type; using T operators; using multithreshold operators.

The first method, with quaternary max, min and unary operators, is the most frequently used. One such principal realization of quaternary logic network is shown in Fig.1.

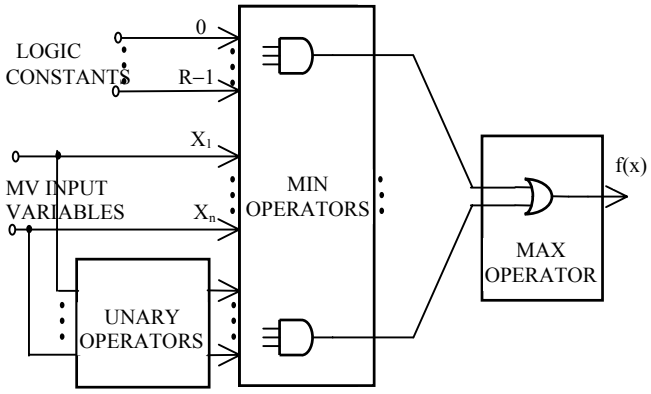

Fig.1. Principle of realization of quaternary logic circuits using max, min and unary circuits.

Methods and procedures for synthesis of standard quaternary networks and systems are very similar to ones used in binary systems [1-3]. Also, the same levels of presentation are used: logic level, functional level and algorithmic level, as well as the same design activities: synthesis, optimization and analysis.

III. SYNTHESIS OF QUATERNARY CMOS LOGIC SYSTEMS AND CIRCUITS

Standard procedure for synthesis of quaternary CMOS logic systems is similar as for binary CMOS logic systems synthesis. It is synthesis of the logic network using standard CMOS quaternary logic circuits. The most frequently used standard logic circuits for the synthesis are max, min and

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unary circuits (see Fig.1.). The standard CMOS quaternary logic circuits, i. e. quaternary CMOS logic cells, should be adequately synthesized and implemented.

One principle for synthesis of CMOS quaternary logic circuits and systems is proposed here. It enables application of methods used for synthesis of standard binary logic circuits and systems. This principle does not use standard CMOS quaternary logic circuits. It uses standard CMOS binary logic circuits and appropriate quaternary CMOS output stage. Such, we obtain more simple procedure for synthesis as well as more simple solutions. The proposed method for the synthesis is shown in Fig. 2.

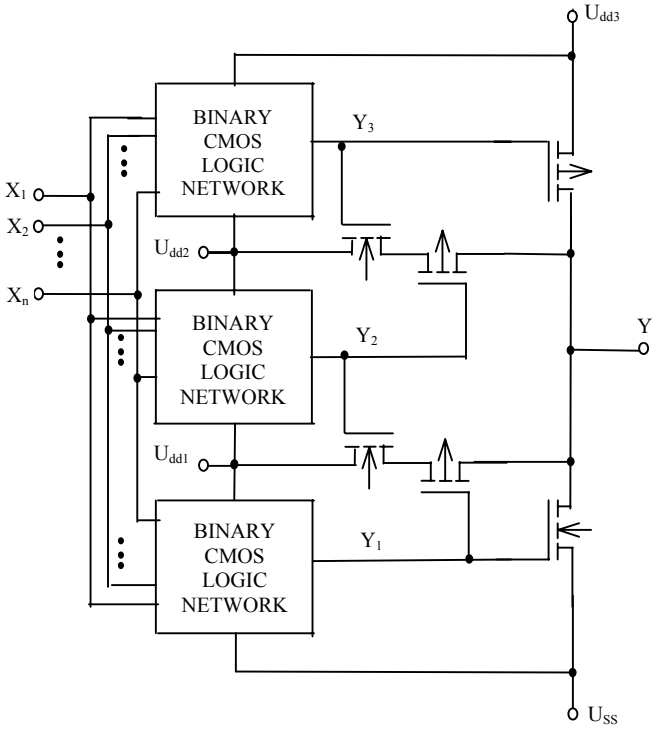

Fig.2. Sheme of proposed method for synthesis of quaternary CMOS logic circuits.

As it can be seen in Fig.2, the proposed method uses three binary CMOS logic networks at the input (conected beetwen diferent supplay voltages) and apropriate quaternary CMOS output stage. The three binary CMOS networks define the logic function of whole quaternary circuit. The CMOS output stage is controled by the three binary CMOS networks and is giving four output states.

The three binary CMOS logic networks at the input are realizing the same binary logic function. That binary function is inverse function of the quaternary output circuit function, i. e. binary function is given by

$$Y_1 = Y_2 = Y_3 = \overline{Y} = \overline{f(X_1, X_2, \dots, X_n)}, \qquad (1)$$

where Y or $f(X_1, X_2, \dots, X_n)$ is the output function that should be realized by the quaternary circuit.

So, this principle of synthesis of CMOS quaternary logic circuit or network is based on synthesis of binary CMOS logic networks with binary logic function given by equation (1). Such, we obtain needed quaternary logic function of realized quaternary circuit or network. CMOS output stage from Fig. 2 gives four quaternary output levels of whole quaternary circuit or network.

Two procedures of the synthesis are proposed here: basic principle and improved principle. The principles will be shown here on the example of synthesis of quaternary circuit with quaternary logic function given by

$$Y = f(X_1, X_2, X_3) = X_1 X_3 + X_2 X_3 . \qquad (2)$$

So, it is necessary to realize three CMOS binary networks with binary function given by

$$Y_1 = Y_2 = Y_3 = \overline{Y} = \overline{X_1 X_3 + X_2 X_3} = \overline{X_3 (X_1 + X_2)} . \qquad (3)$$

The basic principle is very simple. The three binary CMOS logic networks at the input of quaternary circuit are realized using standard CMOS binary logic circuits. So, the same methods as for synthesis of binary logic circuits are used here for synthesis of quaternary logic circuits. That is the advantage of this principle of synthesis.

In the improved principle of synthesis the binary CMOS logic networks at the input of quaternary circuit are realized as the matrixes of CMOS transistors. It reduces the total number of used MOS transistors and number of stages in input binary CMOS networks. So, the total circuit area of the quaternary circuit is reduced and the working speed is increased comparing with basic principle of synthesis.

The practical way of synthesis of quaternary CMOS logic circuit with output logic function given by equation (2) is shown in Fig.3. It is very easy to realize necessary binary logic function given by equation (3) using matrix of CMOS transistors. The same methods used for synthesis of standard binary CMOS logic circuits with more complex output function are also used here. Adequate matrix of CMOS transistors should be synthesized and designed. The output stage is the same as in proposed scheme in Fig.1.

The complete scheme of quaternary CMOS logic circuit with output quaternary function given by equation (2) is shown in Fig. 3. It can be seen from Fig. 3 that all three input CMOS binary networks are the same, connected between four different supply voltages. The input binary networks adequately control the CMOS output stage, such producing four CMOS output quaternary levels.

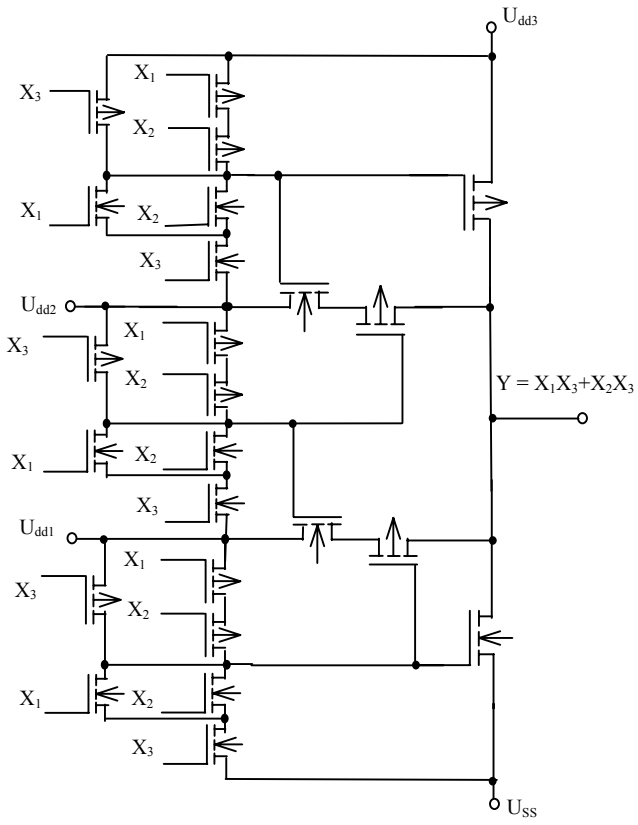

Fig.3. Quaternary CMOS circuit synthesized using CMOS transistors matrix.

IV. OPTIMIZATION OF QUATERNARY CMOS LOGIC CIRCUITS

Next step after synthesis is optimization of quaternary CMOS logic circuit or network. The standard procedure of optimization, as for binary logic circuits, consists of two steps: optimization of each logic circuit (i. e. logic cell) separately and optimization of whole logic network.

The method for optimization of the proposed CMOS quaternary logic circuits is also proposed and described here. It contents two procedures: optimization of binary CMOS logic networks at input of quaternary circuit and optimization of quaternary CMOS output stage.

Since here are used binary CMOS circuits, the optimization of binary CMOS networks at input of quaternary circuit can be realized in a similar way as for optimization of CMOS binary circuits. Here it can be used same principles as for binary CMOS logic circuits.

Optimization is performed according to circuit working characteristics and conditions: average propagation delay time, noise immunity, supply voltage. Optimization should be realized according to circuit area, to obtain circuit with minimal circuit area and appropriate circuit characteristics at the place of application. Here it means that it should determine ratio K of PMOS and NMOS transistor channel width to obtain minimum circuit area and appropriate circuit characteristics.

Here proposed criteria is given by

$$F = \frac{t_{ds}\,\Delta t_d}{NS_R}, \qquad (4)$$

where t_{ds} is average propagation delay time, Δt_d is absolute difference of edge delays of output signal, NS_R is noise immunity referring to supply voltage. It should minimize value F as a function of ratio K. The ratio K with minimal F is value of K that should be applied in the circuit. Criteria F as a function of ratio K should be obtained by computer simulation.

Dependence of criteria F on ratio K for quaternary CMOS circuit from Fig. 3, obtained by PSPICE simulation, is shown in Fig. 4. From the dependence it should be selected ratio K for what criteria F has minimal value.

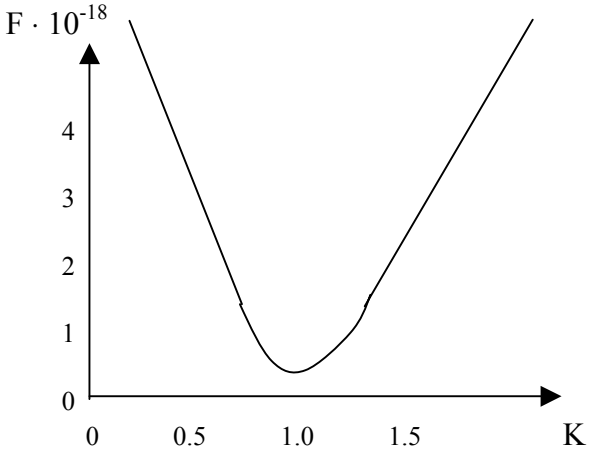

Fig.4. Criteria F as a function of ratio K for quaternary CMOS circuit in Fig.3.

The task of optimization of CMOS quaternary circuit output stage is to determine channel widths of output PMOS and NMOS transistors. Optimization is performed according to working conditions of the quaternary circuit at the place of application. The working conditions are maximally allowed average propagation delay time, fan out factor, and supply voltage.

The optimization should determine minimal value of ratio $k_i = W_i / W_S$, where W_i is output MOS transistor channel width and W_S is standard MOS transistor channel width. For real fan out factor M_r and maximally allowed average propagation delay time t_{dsr}, approximately can be determined k_i . The way of this optimization is principally shown in Fig. 5. The average propagation delay time (t_{ds}) as a function of k_i for fan out factor M=8, obtained by PSPICE simulation, is shown in Fig. 5.

The procedure of optimization is as follows. First, it should be determined by computer simulation dependence of t_{ds} on k_i for known fan out factor M_r of the quaternary circuit. That dependence is shown in Fig. 5. Then, it can be determined from the dependence the real ratio k_i what is necessary for the real allowed average propagation delay time t_{dsr} of the quaternary circuit. It has been illustrated by dashed line in Fig. 5.

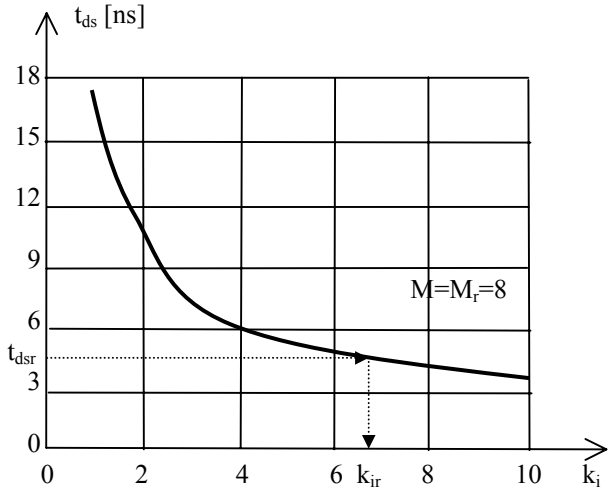

Fig.5. Average propagation delay time as a function of k_i for circuit in Fig.3.

V. CONCLUSIONS

The proposed methods and procedures for synthesis and optimization of quaternary electronic digital circuits and systems are very simple.

The synthesis is based on synthesis of binary logic networks since it is necessary to synthesize three CMOS binary logic networks at the input of quaternary circuit. So, same methods as for binary CMOS logic circuits synthesis are also used here. It can be easily realized CMOS quaternary circuit with any output function.

Optimization is based on optimization of CMOS binary circuits and optimization of quaternary CMOS output stage. The procedures are very similar as in binary CMOS circuits optimization and design.

The proposed procedures are very suitable for realization using computer, as iterative and interactive procedures. Practically the procedures have been realized by personal computer. PSPICE has been used for simulation of circuits

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