Problem Areas by Burn-in of the Electronic Devices

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Abstract **- In this article the method of optimization of "burn-in" duration is suggested. The connection belween the size of the technical resources and the duration of "burn-in" time is established. A system of equations which help to establish an opportunity for calculation of electronic devices exploitation of time for their "burn-in" is proposed.**

Keywordss **- burn-in, reliability of the electronic devices.**

I. INTRODUCTION

Burn-in is defined here as a process that uses a specific type of environmental stress on an accelerated basis, but within design capability, to detect latent flaws or defects that have a high probability of surfacing as infant mortality failures under field conditions.

During the last few years the reliability of integrated circuits and other semiconductors has improved significantly chiefly because the markets supplied by component manufacturers have demanded a greater degree of assurance that the products they use demonstrate a longer and more effective life. The percentage of dead on arrival supplies received has become less and the pressures on goods inwards testing procedures have, to some extent, been reduced. Nevertheless, screening, including burn-in, or rescreening of devices supplied as 'high rel' components remain an important discipline in the manufacture of electronic assemblies.

Early failures, also known as 'infant mortalities', and the concern for extended life in components, therefore, continue to exercise the minds of those companies whose products are required to provide, in use, long mean time between failures with extended operation in the field. The reliability of components and the constant availability of the assemblies they drive have an obvious effect upon the status and ranking of the assembly manufacturer as well as his reputation and, in cases of massive failure, the very existence of the company could be threatened.

Those most at risk in terms of large contracts, life support or defence systems share this vulnerability with, for instance, new companies, those introducing new products, or attempting to move existing products into new markets.

The risk is equally as strong for those who bear the burden of cost of ownership on leased or rented products, where service is built into the price of such leasing or renting. This would include instrument leasing in industry as well as brown goods renting, such as television and video equipment for commercial and domestic use. The ideal production and marketing concept is, that the product supplied to the end consumer, whether industrial, commercial or domestic, shall have uninterrupted life for the optimum time, that is, until a replacement is demanded by age, technological change, or other circumstances.

Into the permutation of failure or replacement comes the whole sequence of electronic of electromechanical cycles by which the equipment is operated: from semiconductors, through populated boards, to the electronic or mechanical output of the whole product. For the electronic and quality engineer, methods exist to help ensure as far as possible the efficient operation of the product, excluding fair wear and tear, negligent use or careless handling.

Excluding components found to be faulty on receipt, semiconductors are subject to early failure: those that survive can be considered robust and reliable. These devices in the main either fail during the first few months of their active life, or continue to perform for the life of the product of which they are a part. Virtually any demonstration of the well known 'bathtub curve' shows the areas of risk by time. The method used to ensure the life and longevity of the components, is to condition them in specially designed equipment by electrical and temperature stress in such a way that, over the period of a week or so, they receive the equivalent of many months initial work. Thus, the period of likely failure is reduced dramatically so that the components the fail burn-in can be rejected and the remainder become a part of production stock as reliable units. The stable, useful life can be accepted as 10 to 15 years.

Semiconductor burn-in is oftenthe surest way of eliminating early early failures. Most intergrated circuits can be stressed for up to 96 hours at 150°C, well above normal working temperatures. Other components are temperature limited to 70°C. So, by burning-in at the discrete component stage, semiconductors can be batched to restrict the possibility of damage by exercising components beyond their acceptable temperature stress levels. Data indicates that burn-in for semiconductors at the higher temperature is equivalent to more than 5000 hours of operation at 50°C, thereby offering a reliability margin against infant mortalities of unstressed components of between 0 and 3000 hours. Burn-in programmes are available which operate devices by time against temperature to cover all component ranges so that those with lower order temperature ceilings can be stressed.

It is obvious that the advantages of the burn-in are indisputable if it will be decided two basic problems:

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-defining of the optimal duration of the burn-in process

-indicated of the influence of the burn-in process and its numeral repeats (in hierarchical level devices, in hierarchical level printed-circuit board, in hierarchical level modules, and in hierarchical level electronic equipment) upon the reliability of the electronic devices.

II. Defining of the Optimal Duration of the Burn-in Process

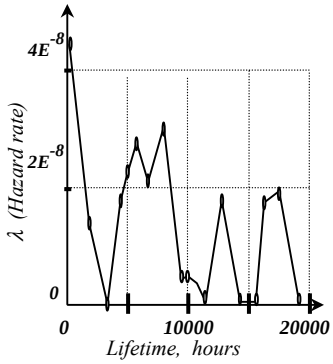

Fig.2 The roller-coaster curve of component hazard rate. Bipolar transistors.

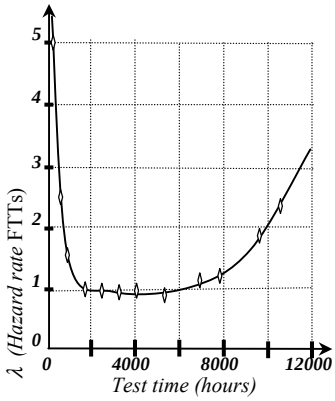

Fig.3 The bath-tub curve of component hazard rate [3].

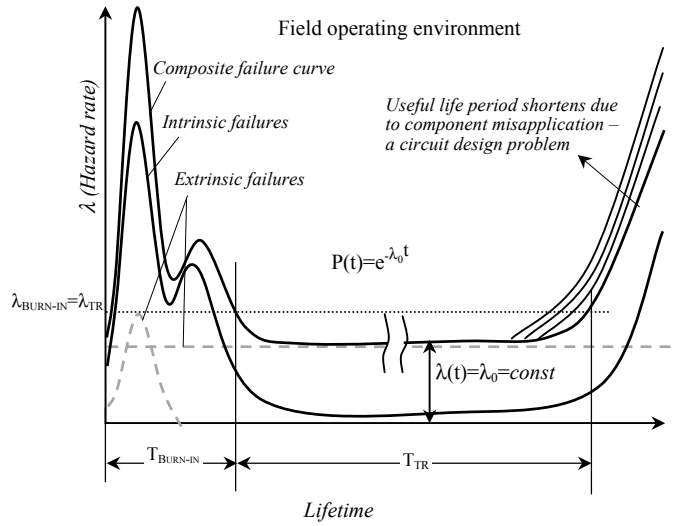

Fig.4 Illustration of intrinsic, extrinsic, and composite reliability curves for component hazard rate in a field-operating environment.

The components used in such lifetests have not at this point been subjected to the destructive or damaging events associated with higher levels of assembly and handling. Very briefly, the early life period often exhibits a fairly high hazard rate. Sometimes the hazard rate shows one or more humps (modes) before it finally attains a low, decreasing pattern, as in Fig. 2 [2].

Sometimes, as in Fig. 3, the early life hazard rate decreases continuously from the very beginning in either case, the underlying cause is the existence of comparatively large built-in defects that quickly grow in size until a failure (usually a short or open circuit) occurs [3]. The term intrinsic infant mortality failures are used to describe these early life failures.

The early life period can under normal operating conditions vary from tens of hours to many thousands of hours.

When in a population of like components, the early life failure have surfaced, the failure pattern enters its low hazard rate period the useful life period. In effect, the intrinsic hazard rate can be zero in this period. If failures do occur, the cause is quite often that there is a tail of early life failures ('residual' failures) caused by defects of an 'intermediate' size. Additionally, failures in the later part of the useful life period will very likely be caused by an early tail of the long-term wearout distribution.

The duration of the useful life period is normally very long for electronic components working under field conditions. One possible criterion for determining the extent of the period is to define it as the 1% percentile lifetime (or some other percentile) after any infant mortality type failures have been eliminated. Another possible criterion is to determine it as the lifetime corresponding to a certain hazard rate value (popularly called a FIT-rate) in the first tail of the wearout distribution. The value of 10 FIT has on occasion been used as a criterion. Useful life periods well above 50 years would not be unusual (beds on results of accelerated lifetimes). However, new technologies with extremely small geometries may possibly have useful life periods of less than ten years.

Although hazard rate curves normally are associated with the intrinsic reliability of components, it is quite feasible to have similar plots for the composite reliability, in other words 'the end results', which is the combination of the intrinsic and extrinsic failures. In order to generate a plot of extrinsic reliability we would need to keep track of a sample of like components being used in a certain system. They would all go through the same handling and assembly procedures and be installed in the same end-use environments. Most components in the sample would come through unscathed, whilst some might have been subjected to electrical overstress, been dropped on the workbench or on the factory floor, been overheated through careless use of a soldering iron, or received some other form of stress that can have weakened them. It is very likely that these weakened components will give rise to an extra number of early failures. These additional early life failures are called extrinsic infant mortality failures, see Fig. 4, as they have been born by circumstances extrinsic to the components [3]. The purpose of the reliability prediction is to separate all the elements, characterizing with high infant mortality failures (faint elements) from reliability (strong) elements.

In the present paper we consider the method, associated with optimization of the duration of time for technological burn-in. This method gives the opportunity for calculating of the technical resources and operating term of the electronic devices, which can be done simultaneously with the time computing for their burn-in.

In order to define the duration of the technological burn-in $T_{BURN-IN,}$ we can use the principle: " the period of burn-in is optimal, if the extended electronic devices owe maximum

reliability in their determining technical resources $T_{BURN-IN}$". It is used the possibility for expression of this index via the exponential law of distribution:

$$R(t) = \exp[-\int_0^t \lambda(t)dt] \quad (1)$$

from where:

$$R(T_{TR}, T_{BURN-IN}) = \exp[-\int_{T_{Burn-in}}^{T_{TR}+T_{Burn-in}} \lambda(t)dt] \quad (2)$$

It is known that the intensity of failure $\lambda(t)$ owes saddle - shaped character, which is shown in Fig.4. That's why we seek a way for minimum of parameter $\lambda(t)$. For this purpose we use the equation:

$$\frac{\partial\lambda(T_{TR}, T_{Burn-in})}{\partial T_{Burn-in}} = 0 \quad (3)$$

As we combine it with equation (2), the final equation looks like:

$$\lambda(T_{Burn-in} + T_{TR}) - \lambda(T_{Burn-in}) = 0 \quad (4)$$

If the values of $\lambda(t)$ in the initial and in the final moment are equal, the duration for technological burn-in will have optimal value.

From all written until this moment notes we can reach to the conclusion that the magnitude of the technical resources depends on the duration of burn-in activities. Consequently, if in the equation (4) we accept for unknown quantity T_{TR}, too, and if this equation is connected with the certain quantitative requirements to the reliability of the electronic devices, we will receive a system that consists of two equations with two unknown quantities. This system gives a chance to estimate the value of $T_{BURN-IN}$ as well as this one of T_{TR}. For example, if $P(t)_{desired}$ is the possibility for failureless work, we have:

$$\begin{cases} \lambda(T_{Burn-in} + T_{TR}) - \lambda(T_{Burn-in}) = 0 \\ \exp\left[-\int_{T_{Burn-in}}^{T_{Burn-in}+T_{TR}} \lambda(t)dt\right] = R(t)_{desired} \end{cases} . \quad (5)$$

The operating term T_{OT} is more compendious index than the index of the technical resorce T_{TR}. Via it we can estimate not only the life – time of the devices, but also their preservation.

$$T_{OT} = \frac{T_{TR}}{T_A} + \frac{\sum_{i=1}^{N} t_{R_i} + \sum_{j=1}^{n} t_{PM_j}}{24}, \quad (6)$$

where:

- t_{PMj} - is a duration of j'th preventive maintanance
- t_R - duration of the regeneration after restoration of the j'th failure
- N - number of the failures (number of the breakdown restrorations)
- n - number of the preventive maintanances
- T_A - average number of working hours for one day of the control electronics, in which are assembled the examined devices.

The technical resources in the Eq. (6) are measured in hours and the operating term is received in days.

III. Influence of Burn-in upon the Reliability of the Electronic Devices

In a lot of cases the technological burn-in of the electronic devices is carried out not only once. Therefore its influence upon the reliable indexes should be indecated.

Now let a load Q^* acts two times upon the device. In the both cases we mark with P_1 the probability that Q^* is less than a collapsing load.

Then $(1-P^2)$ is a moment when, in all probability, Q^* reaches to the limit value of R at least one time. Under such circumstances n-fold effect will lead Q^* to the probability: $1-P^n$. Consequently we calculate:

$$P_n = \frac{dP_1^n}{dx} = n.P^{n-1}.p_1, \quad (7)$$

where p_1 is a current value in the case of only one load.

If the function p_1 is submitted to the law of normal distribution, the function p_n will have a lot of differences in comparison with this distribution.

Consequently, the mathematical expectation and the dispersion will look like:

$$m_{Q_n^*} = \int_{-\infty}^{\infty} x p_n dx = n \int_{-\infty}^{\infty} x P_1^{n-1} p_1 dx; \quad (8)$$

and

$$\sigma^2_{Q_n^*} = \int_{-\infty}^{\infty} (x - m_{Q_n^*})^2 P_1^{n-1} p_1 dx; \quad (9)$$

Therefore, a double load by normal law of distribution should be given by the equations:

$$p_1 = \frac{\exp(-\frac{h^2}{2})}{\sqrt{2\pi}\sigma_{Q_1^*}} = \frac{\Phi(h)}{\sigma_{Q_1^*}}, \quad (10)$$

$$P_1 = \frac{1}{2} + \Phi(h), \quad (11)$$

where $\Phi(h)$ is called Laplas' function and

$$h = \frac{(x - m_{Q_1^*})}{\sigma_{Q_1^*}} \quad (12)$$

is its parameter.

Then indecating the both equations (10) and (11) we calculate the equations as:

$$m_{Q_2^*} = \frac{2}{\sigma_{Q_1^*}} \int_{-\infty}^{\infty} x[\frac{1}{2} + \Phi(h)]\Phi(h)dx = \frac{\sigma}{\sqrt{\pi}} \approx 0{,}56\,.\sigma_{Q_2^*}; \quad (13)$$

and

$$\sigma^2_{Q_2^*} = \frac{2}{\sigma_{Q_1^*}} \int_{-\infty}^{\infty} (x - m_{Q_1^*} - \frac{\sigma_{Q_1^*}}{\sqrt{\pi}})^2 [\frac{1}{2} + \Phi(h)]\Phi(h)dx =$$

$$= \sigma^2_{Q_1^*}(1 - \frac{1}{\pi}) \approx 0{,}83\ \sigma_{Q_1^*}; \quad (14)$$

By this analogy, if the load is a threefold one, the following equations shuold be written as:

$$m_{Q_3^*} = \frac{3}{\sigma_{Q_1^*}} \int_{-\infty}^{\infty} x[\frac{1}{2} + \Phi(h)]^2 \Phi(h)dx = \frac{3\sigma_{Q_1^*}}{2\sqrt{\pi}} + m_{Q_1^*} \approx 0{,}85\ .\sigma_{Q_1^*}; \quad (15)$$

$$\sigma_{Q_3^*} = \frac{3}{\sigma_{Q_1^*}} \int_{-\infty}^{\infty} \left(x - m_{Q_1^*} - \frac{3\sigma_{Q_1^*}}{2\sqrt{\pi}} \right)^2 [\frac{1}{2} + \Phi(h)]^2 \Phi(h)dx =;$$

$$= \sigma_{Q_3^*} \left(1 + \frac{\sqrt{3}}{2\pi} - \frac{9}{4\pi} \right) \approx 0{,}75\ .\sigma_{Q_1^*}; \quad (16)$$

In the case of fourfold load, then the estimations are:

$$m_{Q_4^*} = m_{Q_1^*} + 1{,}029\ \sigma_{Q_1^*}; \quad (17)$$

$$\sigma_{Q_4^*} \approx 0{,}68\ .\sigma_{Q_1^*}; \quad (18)$$

If the load is a n-fold one, we should use the equations:

$$m_{Q_n^*} = m_{Q_1^*} + 3{,}38(1 - n^{0{,}262})\sigma_{Q_1^*}; \quad (19)$$

$$\sigma_{Q_n^*} \approx n^{0{,}262}\ .\sigma_{Q_1^*}; \quad (20)$$

In the common case, the limit state will reach to the reliable parameter by using a load with Q^*. At this moment the equation is:

$$P_n = \frac{1}{2} + \frac{1}{2}\Phi(h) \quad (21)$$

where:

$$h = \frac{(\overline{R} - m_{Q_n^*})}{\sigma_{Q_n^*}}, \quad (22)$$

and m and σ are defined by the equations (19) and (20).

VI. CONCLUSION

In the paper is pointed out the way for optimal calculation of the duration of time for burn-in and of the technical resources of the electronic devices. It is read, too, the influence of the numerous tests upon the reliability of the devices.

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