High Resolution Time-to-Digital Converter

Goran S. Jovanović[1] and Mile K. Stojčev[2]

Abstract – **This paper describes the architecture and performance of a high-resolution time-to-digital converter (TDC) based on a Vernier delay line. The TDC is used as a basic building block for time interval measurement in an ultrasonic liquid flowmeter. Operation of the TDC with 10 ps LSB resolution and 1 ms input range has been simulated using library models for 1.2 m double-metal double-poly CMOS technology. The TDC operates at clock frequency of 200 MHz, and is composed of 500 delay-latch elements. The difference in delay between two chains, one for the start and the other for stop pulse, is controlled by the delay locked loop (DLL).**

Keywords – **Time to digital conversion, Vernier delay line, DLL.**

I. Introduction

The precise measurement of the time interval between two events with very fine timing resolution is common challenge in the test and measurement instrumentation (logic analyzer, ATE system, nuclear instrumentation), industrial control (multichannel DAS, ultrasonic liquid flowmeters), electronic embedded control system (automotive controllers, medical devices avionics), etc. [1-3]. A time-to-digital converter (TDC) is one of the crucial building blocks installed into this type of equipment. High-resolution TDC is primarily used in application areas that require a resolution better than 10 ps, low dead-time (minimum time between two measurement, less than several microseconds) and large dynamic range (maximum time interval that can be measured, can be in the range of hundred seconds) at operating frequency from the minimum of around 1 MHz to the maximum of 500 MHz. Therefore the time intervals of interest for measurements in our case range from 10^{-11} s to 10^{2} s [4].

In principle, time interval measurement performed by the TDC can be decomposed into the following two steps. The first one is called short-time interval measurement, and is characterized with very fine timing resolution in the range from 10 ps up to 500 ps. The second referred as long-time-interval characterizes a coarse time resolution in the range from 3 μs up to 100 s. For evaluating long-time interval measurements standard counter based methods are used. The principle methods of digitizing short-time intervals have been reviewed in [1]. They include utilization of fast counters [5], analog methods based on generating voltage ramp [6] and dual-slope conversion [7], and various CMOS tapped delay line configurations [3,4,8].

[1]Goran S. Jovanović is with the Faculty of Electronic Engineering, Beogradska 14, 18000 Niš, Serbia and Montenegro, E-mail: joga@elfak.ni.ac.yu

[2]Mile K. Stojčev is with the Faculty of Electronic Engineering, Beogradska 14, 18000 Niš, Serbia and Montenegro, E-mail: stojcev@elfak.ni.ac.yu

The goal of this works is to develop a TDC, which would enable the realization of an ultrasonic based liquid flowmeter in pipe under pressure with 1% time-interval measurement accuracy, and 10 ps time-resolution at operating frequency of 200 MHz.

II. TDC Principle of Operation

TDC's can traditionally be divided into the following two groups: analog and digital. In general, analog TDC's are based on current integration, while the digital on some counting methods. Recently alternative TDC architectures have emerged which are somewhere in between these two extremes.

For realization of the TDC that would be implemented into our ultrasonic liquid flowmeter several different candidate architectures have been considered. In the sequel, our experiences about the properties and limitations of such TDC's, mainly acquired involving simulation methods, are presented. The starting point for our comparative study was: a) available, transistor models for 1.2 μm double-metal double-poly CMOS technology, mainly used for synthesis of custom circuits; and b) commercially available FPGA/CPLD circuits (Xilinx, Spartan series) that we used for integration of the digital circuits needed to create a complete interpolating time counter on a single CMOS FPGA/CPLD chip. PSpice 9.2 and Xilinix Projekt Navigator V. 4.2WP2.X software were used as simulation and synthesis tools, respectively.

A. Analog TDC-Based on Current Integration

Analog high resolution TDC consists of a constant current source used to charge a capacitor, whose voltage is sampled when a trigger pulse occurs. An ADC then converts the analog voltage to a digital value. Analog time-to-voltage converters can provide about 10 ps resolution over a dynamic range of 1:50 - 1:1000, but they tend to be nonlinear and are difficult to stabilize. One good way of stabilizing them is to use dual-slope conversion, which is unfortunately also slow and limits the measurement rate and increases dead-time, in some applications such as for example those used time-of-flight particle detectors, laser range finders, and logics analyzers [1,4,9]. In our case, bearing in mind that the time propagation of the ultrasonic signal through the pipe is an order of hundred microseconds [10] the dual-slope TDC represents a good candidate solution. Details concerning TDC based on dual-slope conversion will be given in Section III.

B. Digital TDC-Base on Counter

The counter based digital TDC consists of a Gray code counter running at high speed, which value is sampled when a trigger pulse occurs [1,9]. However, time interval digitalization with sub nanosecond resolution using only a simple frequency counter requires impractical high clock frequencies or long averaging times. In spite of its simple architecture this type of TDC, by our opinion is not a good design choice, primarily due to the prerequisites for high-speed counter operation (order of several GHz).

C. TDC-Based on Vernier Delay Technique

The time resolution of the counter based TDC can be improved significantly by using the gate delay as the basic time unit. The fundamental concept of the delay Vernier technique is that the timing resolution is determined by the difference between two propagation delay values. The interpolation methods implemented in this case is used to interpolate time fractions inside clock cycles. A Vernier structure consists of a pair of tapped delay lines with a flip-flop at each corresponding pair of taps and is presented in Fig. 1. A stop signal propagates through one of the delay chain, while the start signal propagates through the other, clocking the flip-flop at each stage. The difference between the start and stop propagation delays determines the timing between adjacent stages. For more details, see [4].

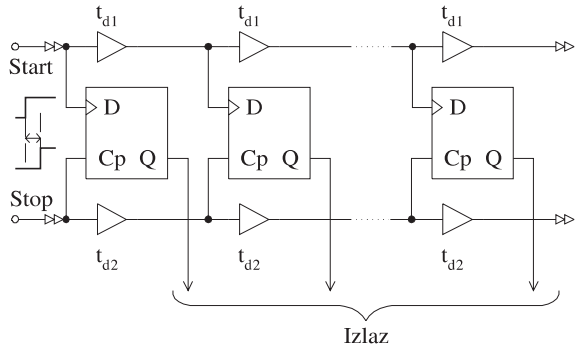

Fig. 1. Typical Vernier delay line

The dynamic range of the TDC based on Vernier delay technique, i.e. the maximum time that can be measured, is limited to $t_{DR} = n \cdot (t_{d1} - t_{d2})$, where n is a number of delay elements of the delay line. However, the range of the TDC can be extended by introduction of a simple counter [3,4,9]. Using Vernier delay technique implemented on commercial available FPGA chips [3] a time resolution of 200 ps can be achieved. However, CMOS process is very temperature sensitive so frequent calibrations with a time reference is required. In spite of the mentioned drawbacks, by our opinion the architecture based on the Vernier principle, represents a very good candidate design solution.

III. Implementation of the TDC Based on Vernier Delay Technique

In order to obtain both high precision and long time measurement we have used the time interpolation technique based on the classic Nutt method [7,11]. It involves splitting the measured interval T_{in} (in our case of order 800 μs), from the rising edge of the start pulse to the rising edge of the stop pulse, into two subintervals. The first subinterval, corresponds to the integer number N_c of the reference clock period T_{CLK} (5 ns), while the second subinterval characterize a duration equal or less than one clock period. The first subinterval, called coarse time interval measurement, is equal to $N_c \cdot T_{CLK}$. It is synchronous to the system clock and is measured with binary counter (*Coarse_Counter*) at 200 MHz clock. More details concerning this problematic can be found in [4,10].

In order to improve a time resolution of the second subinterval, a TDC that use Vernier delay line. In general, the Vernier measurement technique is based on a propagation delay difference between two chains. The chain is realized with delay cells connected in cascade.

In this paper we describe the structure of an analog voltage-controlled delay cell (see Fig. 2). The delay cell represents a basic building block of a delay chain. As can be see from Fig. 2, the delay cell is implemented as a two-stage inverter. Transistors M_1 and M_2 are constituents of the first stage, while transistors M_7 and M_8 form the second stage. Transistors M_3 and M_4 act as current source and current sink, respectively. Voltages $V_{P_{bias}}$ and $V_{N_{bias}}$ regulate currents of M_3 and M_4, respectively. The bias circuit, composed of transistors M_9, M_{10} and M_{11}, provides correct polarization for transistor M_3 and M_4. With order to linearize the transfer characteristic of the delay cell, transistors M_5 and M_6 are used. In Fig. 3, the transfer function, which represents variation of time delay in term of control voltage V_C for the cell pictured in Fig. 2, is presented. As can be see from Fig. 3, for used technology, the variation of a delay is almost linear within the range of 775 ps up to 1025 ps.

The second building block of the Vernier delay line (see Fig. 1) is the storage element. It can be realized as a latch or D flip-flop.

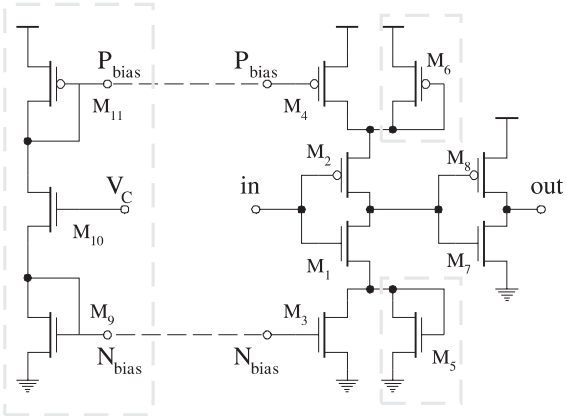

Fig. 2. Analog voltage-controlled delay cell

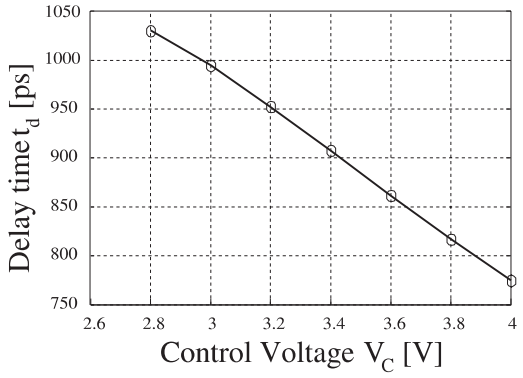

Fig. 3. Propagation delay time in term of control voltage V_C

Two design requirements have to be fulfilled when the Vernier delay line is realized. The first one relate to a measurement resolution (∼10 ps). This resolution can be achieved if the delay difference between the two chains is kept small. The second relate to a wide measurement operating range (up to 5 ns). It can be achieved by installing chain with more then 500 delay cells. Having this in mind, the crucial design challenge now, from aspect of silicon area, can be achieved if we decrease the complexity of both the storage element and the delay cell. Here, we propose one solution where the delay chain of the *start* pulse is modified in respect to [4] such that it includes both, the original delay line (see Fig. 2) and the ladder structure of storage elements, see Fig. 4. The structure of the second chain is composed of delay cells already sketched in Fig. 2.

As can be see from Fig. 4, the delay cell for start pulse consists of three inverters, I_1, I_2 and I_3. Inverters I_1 and I_2 form the chain for the start pulse. At the some time, inverters I_2 and I_3 are connected as latch. In this manner, complexity of the hardware structure given in Fig. 1 is decreased compared to [2-4]. Let note, that I_1 and I_3 are implemented as a three-state drivers, while I_2 as a voltage-controlled delay element.

The structure of the proposed modified Vernier delay line is sketched in Fig. 5. Two control voltages, V_{C1} and V_{C2}, are used. The control voltage V_{C1} is used for delay adjustment of the *start* delay chain, while V_{C2} is intended for delay adjustment of the *stop* delay chain. In our proposal V_{C2} is fixed, while VC1 is determined during calibration phase, see Fig. 6. Namely, during this phase, the inputs *start* and *stop* are driven with pulses of known (in advance defined) phase and frequency. The phase detector generates control signals *up* and *down* by witch it regulates the charging and discharging current of the charge-pump circuit. The voltage at the output of a low-pass filter is then converted by the ADC and then reconverted by the DAC with order to be used as a control voltage V_{C1} during the measurement process.

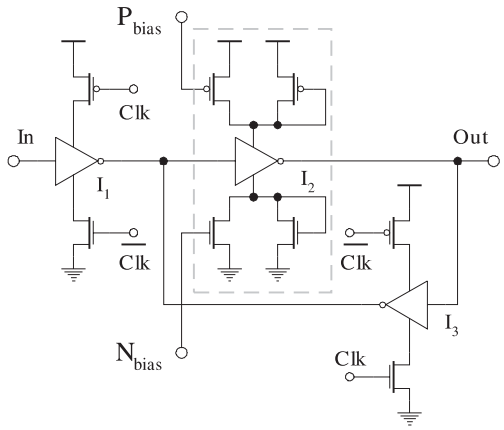

Fig. 4. Hardware structure of a latch with three-state output control and a voltage-controlled delay element

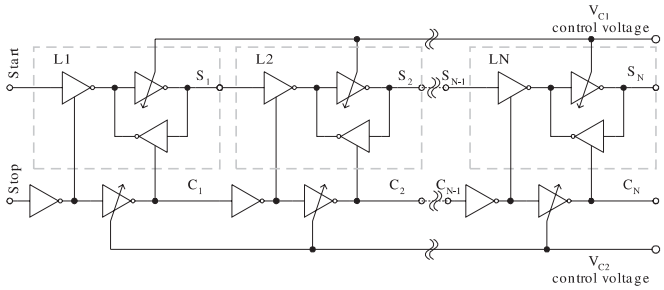

Fig. 5. Modified two chain Vernier delay line

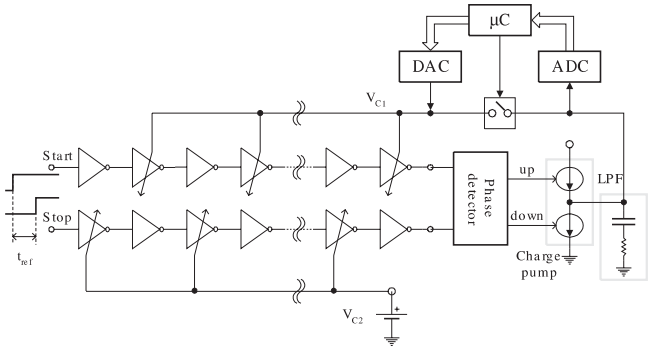

Fig. 6. DLL used in a feedback loop of the Vernier delay line

IV. Simulation Results

Here, we propose a full-custom circuit design approach for implementation of the described TDC architecture based on the Vernier method. Testing and verification of the design was performed using software tool PSpice 9.2 and models of components (transistors, diodes, capacitor, etc.) for 1.2 μm CMOS double-metal double-poly technology. Using simulation method it is possible to evaluate precisely and accurately the propagation time of *start*, S_i, and *stop*, C_i, pulses through both chains (see Fig. 5). For operating system clock frequency of 200 MHz the *coarse_counter* is clocked with pulses of 5 ns duration and its final value corresponds to coarse time interval measurement. From other side, the second subinterval which is less than 5 ns and corresponds to fine resolution interval measurement, have to be estimated with resolution of ∼10 ps. Having this in mind, the hardware structure of the Vernier delay line have to be composed of 500 cells, what corresponds to 5 ns (500·10 ps=5 ns). For better visualization of the simulation results presented in this

paper, a time resolution of 400 ps between two adjustment pulses is adopted for presentation in Fig. 7. Also, the time interval t_x between the *start* and *stop* pulses, in a concrete case, is equal to 4 ns. Under this conditions the waveforms S_i and C_i $(i = 1,,12)$ are generated at the outputs of the corresponding delay cells. As can be seen from Fig. 7, until the delay cell 10 the pulse S_{10} is in advance with respect to the pulse C_{10}. At inputs of cells 11 both pulses arrive at the some moment, while at cell 12 the pulse C_{12} is in advance with respect to S_{12}. This means that the propagation of the *start* pulse is further prohibited. If we analyze the output of the corresponding latch, we see that latches from 1 up to 10 are set to one while latches L_{11} and L_{12} are set to zero.

The principle of operation of both delay chains can be described according to the presentation in Fig. 8. For the some operating condition we see that the delay propagation between the *start* and *stop* signals will be equal after the 10th cell i.e. when the cross-point between two lines appears.

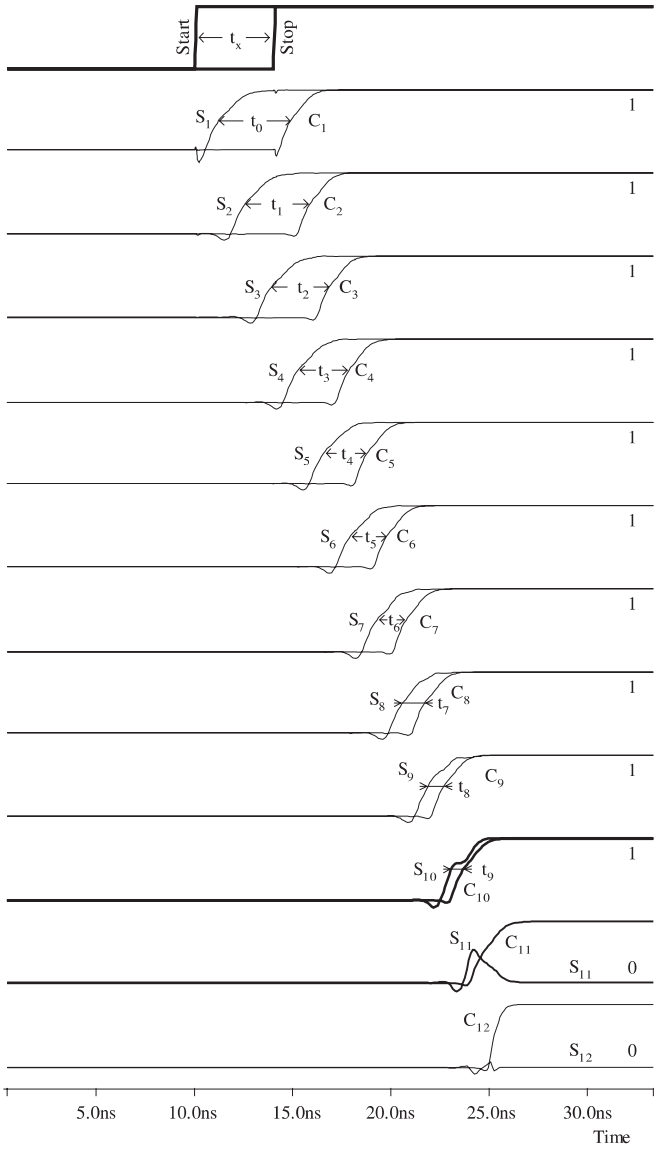

Fig. 7. Propagation of *start* S_i and *stop* C_i pulses

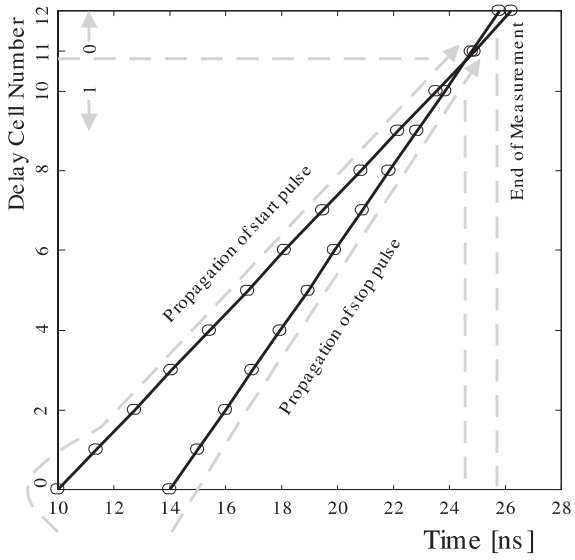

Fig. 8. Number of delay-latch elements set to logic one during fine time resolution measurement

V. Conclusion

An efficient architecture of a time to digital converter, based on the Vernier delay line, intended for high-resolution time interval measurement is presented in this paper. The proposed architecture contains two delay line chains. The first one represents a composition of a delay line and memory cells. The second chain is implemented as a classical chain of a non-inverted stages connected in cascade. The delay of both chains is voltage-controlled. The TDC's operation has been simulated and implemented using models 1.2 μm double-metal double-poly CMOS technology. For operating frequency of 200 MHz and chain composed of 500 delay cell elements a resolution of 10 ps LSB was achieved. Bearing in mind, that the delay of the CMOS cell is sensitive to ambient temperature and supply voltage variations, a delay lock loop is involved in the structure of the TDC in order to compensate these negative effects. For precise and accurate time-interval measurement a calibration procedure is involved. It is primarily intended to achieve a balanced difference in delay between the two voltage-controlled delay chains. To implement this technique a DLL feedback loop is used. The TDC is used as a constituent block intended for precise and accurate time interval measurement in an ultrasonic liquid flowmeter.

References

[1] Porat D.I., "Review of sub-nanosecond time-interval measurement", *IEEE Transaction on Nuclear Sci.*, NS-20, No. 5, pp. 36-51,1973.

[2] Gray C.T., et al., "A sampling technique out its CMOS implementation with 1Gb/s bandwidth and 25ps resolution", *IEEE Journal of SSC*, vol. 29, No. 3, pp. 340-349, March 1994.

[3] Kalisz J., et al., "Single chip interpolating time counter with 200ps resolution and 43-s range", *IEEE Transaction on Instrumentation and Measurements*, vol. 46, No. 4, pp.851-856, 1997.

[4] Dudeck P. et al., "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line", *IEEE Journal of*

Solid-State Circuits, vol. 35, No. 2, pp. 240-246, February 2000.

[5] Sasaki A.E. et al., "1.2GHz GaAs shift register IC for dead-time-less TDC application", *IEEE Transaction on Nuclear Sci.*, vol. 36, pp. 512-516, February 1989.

[6] Stevens A.E., et al., "A time-to voltage converter of analog memory for colliding beam detector", *IEEE Journal of Solid-State Circuits*, vol. 24, No. 6, pp. 1748-1752, December 1989.

[7] Raisanen-Routsalainen E. et al., "An integrated time-to-digital converter with 30-ps single-shot precision", *IEEE Journal of SSC*, vol. 35, No. 10, pp. 1507-1510, October 2000.

[8] Christiansen J., "An integrated high resolution CMOS timing generator based on an array of delay locked loops", *IEEE Journal of SSC*, vol. 31, No. 7, pp. 952-957, July 1996.

[9] Christiansen J., "An integrated CMOS 0.15ns digital timing generator for TDC's and clock distribution systems", *IEEE Trans. on Nuclear Sci.*, vol.42, No.4, pp.753-757, August 1995.

[10] V. Pavlović, et all, "Realization of the Ultrasonic Liquid Flowmeter Based on the Pulse-Phase Method", *Ultrasonics 35* (1997) 87-102.

[11] Nutt R., "Digital time interval meter", *Rev. Sci. Instrum.*, vol. 39, pp. 1342-1345, 1968.