Generation of a Test Strategy for Testing the Analog Part of an Integrated Circuit for Digital Wireless Short-Range Communication

Rumen Iv. Arnaudov[1]and Ivo G. Aldimirov[2]

Abstract – **Subject of this article is the generation and application of a Test strategy for measure and test of Application Specific Standard Product (ASSP) Integrated Circuit (IC) for digital wireless communication. It is given a description of the employed methods for testing the building blocks of the *analog part* of the device. They are based on the way they take place in the industrial test of the mixed-signal IC. Comment and quotation on some existing methods is made. It is emphasized on some potential problems that might influence the test time/cost, the accuracy and the stability of the tests. Suggestions for solving some of those problems are made.**

Keywords – **digital signal processing (DSP), industrial test, mixed-signal Integrated Circuit, test methods, digital tests, device under test (DUT).**

I. Introduction

Fig. 1 shows typical block diagram of a Front-end radio Application Specific Standard Product (ASSP). It is used as a basis for analyses of the methods for test and measurement described hereafter.

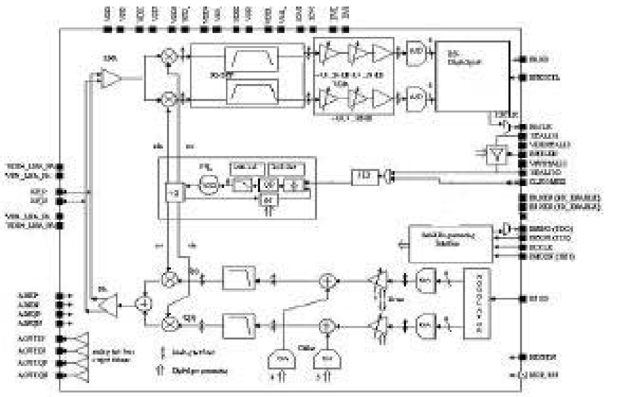

Fig. 1. Block diagram of typical transceiver for digital wireless communication.

The diagram represents typical transceiver with zero intermediate frequency (IF=0). It consists of two parallel I and Q channels in the receive and the transmit part. On the same silicon die is also implemented the digital part, consisting of the corresponding ADCs and DACs, the bank of registers used for initialization and control of the device.

II. Generation of a Test Strategy - Pro and Con.

The test strategy combines in one the test methods employed for measuring the electrical parameters of the functional building blocks of a silicon device. Strictly speaking, generating test strategy is not absolutely necessary. A test engineer can generate a test program entering the test program code based on the device data sheet. There are several problems with this type of undisciplined approach. First, device testability will probably not be identified early enough to allow the addition of test features to the design - design for test (DFT) blocks. The test strategy generation forces the design and test engineers to work through all the details of testing at an early stage in the design cycle. Second, the test engineeer may create test-to-test compatibility problems if the details of all tests are not known up front. For example - a clocking scheme that works well for one test may be incompatible with the clocking scheme required of a subsequent test. The first test may then need to be rewritten from scratch so that the clocking schemes mesh properly. Third, test hardware such as device interface board (DIB) and probe interface hardware cannot be properly designed until all test details are known. The test strategy generation helps to identify which hardware resources of the automated test equipment (ATE) will be used and the possible shortfalls in the target testers capabilities.

III. Test Program Structure

Tester languages vary from low-level C routines, to very sophisticated graphical user interface environments. Despite wide differences test programs consist of all or most of the following sections: creation of wave forms and other test initializations, calibrations of the tester hardware, continuity tests, DC parametric tests, AC parametric tests, digital patterns (also known as functional tests), digital timing tests, test sequence control, test limits and binning control.

IV. DSP Based Test Methods [1,2]

Basic principles for forming DSP test strategy.

AC measurements such as gain and frequency response can be measured with relatively simple analog instrumenta-

[1]Rumen Iv. Arnaudov is with the Faculty of Communications and Communications Technologies, Technical University, Kliment Ohridski 8, 1000 Sofia, Bulgaria, e-mail: rarnaud@vmei.acad.bg

[2]Ivo G. Aldimirov is with the Air Traffic Services Authority (ATSA), Communications department at Plovdiv International Airport, e-mail:aldimirov@yahoo.com

tion. To measure gain, an AC continuous sine wave generator can be programmed to source a single tone at a desired voltage level and frequency. A true RMS voltmeter can then measure the output response from the DUT, and the gain can be easily calculated. The pure analog approach to AC testing suffers from few problems, though. First, it is relatively slow when AC parameters must be tested at multiple frequencies. Second, traditional analog instrumentation is unable to measure distortion in a presence of the fundamental tone. Thus the fundamental tone must be removed with a notch filter, adding to test hardware complexity. Third, analog testing measures RMS noise along with RMS signal, making results unrepeatable unless we apply averaging band-pass filtering.

DSP is a powerful methodology that allows faster, more accurate, more repeatable measurements. DSP based testing is based on the sampling theory. The application of DSP in the industrial test can be briefly described as: time domain captures data (signal sampling), fast Fourier transformations and frequency domain output data (as it is shown on Fig. 2).

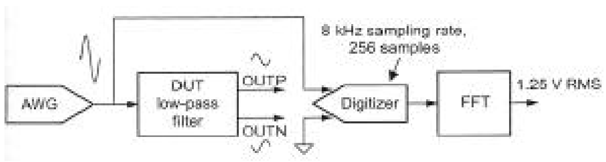

Fig. 2. Configuration of a sampling measurement system.

When testing functional blocks such as LPF, BPF and VGA it has to measure the gain, the THD and the SNR for a number of frequencies in the working range. For that purpose waveforms are software generated and loaded as segments in the memory of an AWG - arbitrary waveform generator, and are applied as a multitone at the input of the analog channel under test. At the output the captured signal is digitized and DSP analyzed using fast Fourier transformation (FFT). The amplitudes and the phases of the spectral bins - elements of the multitone are compared with the ones applied at the input. The spectral bins corresponding to the harmonics of the fundamentals in the multitone are measured too.

The creation of a waveform is based on the sampling theory. Periodical sine signals are described as following:

$$v(t) = A_1 \sin(2\pi \frac{f_1}{f_s} + \varphi_1) + A_2 \sin(2\pi \frac{f_2}{f_s} + \varphi_2) + \ldots + A_n \sin(2\pi \frac{f_n}{f_s} + \varphi_n)\,, \quad (1)$$

where f_1,...,f_n are the frequencies of the multitone, φ_1,...,φ_n are their corresponding phases, f_s is the used sampling frequency.

When waveform is generated or when capture and reconstruction of a waveform occurs, f_s – the sampling frequency is the clock frequency of the hardware instrumentation. In this case:

$$\Phi = f_{\text{bin}} \frac{f_s}{n_{\text{samples}}}, \quad (2)$$

where Φ is the frequency of interest, n_{samples} is the number of captured samples, f_s is the sampling frequency, and f_{bin} is the corresponding to Φ spectral bin.

The approach to develop DSP based tests should be as following:

1. All the frequencies of interest (Φ) that have to be measured must be known and whenever need have to be corrected within reasonable tolerances for getting correct results out of the DSP computations. The choice of f_s and $n_{samples}$ has to comply with the following: f_{bin} has to be mutually prime with the number of samples. Otherwise there is a risk in the measurement results of increased presence of harmonic distortions components, intermodulation distortions components and quantization noise. Whenever FFT is in use n_{samples} must be power of 2. The n_{samples} has to be chosen according to the required frequency resolution (F_{res}) of the measured spectrum:

$$F_{\text{res}} = \frac{f_s}{n_{\text{samples}}} \quad (3)$$

It has also to be considered how close the measured signal level is to the noise floor of the capture instrument. Measurement with insufficient F_{res} integrates the energy of the neighbouring spectral bins and as a result the noise level is higher. Choosing higher F_{res} solves this problem but increases the test time. In this case the test time is related to n_{samples} and the period of sampling or $1/f_s$ according to:

$$\text{Test time} = T_{\text{hw}} + T_{\text{capture}} + T_{\text{mv}} + T_{\text{calc}}\,, \quad (4)$$

where T_{hw} – time for hardware setup, T_{capture} – time for signal capture, T_{mv} – time for moving captured data, T_{calc} – time for calculations. T_{capture} is described as:

$$T_{\text{capture}} = \frac{n_{\text{samples}}}{f_s} = \frac{1}{F_{\text{res}}} \quad (5)$$

According to (4) and (5) the more the number of samples the longer the test time for the corresponding measurement which could be unacceptable in a number of cases.

2. The choice of n_{samples} must comply with the period of the measured signal according to:

$$\frac{n_{\text{samples}}}{f_s} = \text{int}\, T_i\,, \quad (6)$$

where $t_i = 1/f_i$. Equation (6) expresses the requirement for f_s and the period of the measured signal mutual relation i.e. an integer number of period has to be captured. Otherwise the Fourier analyses of a non-periodical signal will produce smearing in the output spectrum as illustrated on Fig. 3.

3. It is important to choose the value of f_s so that the hardware clock (f_s itself) to comply with (6) for most of the AC measurements - signal frequencies. This way reprogramming during the program run will not be needed and test time and test cost will be saved as a result.

V. DSP Based Tests

They are used for testing analog functional block such as RF receive/transmit, BPF, LPF, and VGA.

For testing BPF, LPF and similar blocks requiring characterization for a numb er of in-band and out-of-band frequencies a multitone is applied [1], [2]. The multitone waveform comprises the specific frequencies in the transfer characteristic of the analog block. The spectral bins of the predefined

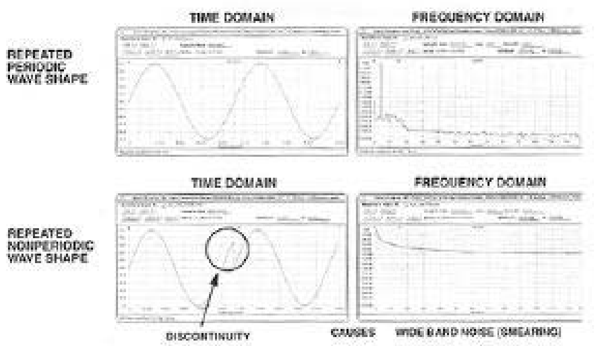

Fig. 3.

frequencies of interest as they appear in the output are subject of analysis. The measurement analysis came across the following problems:

1. The out-of-band frequencies of BPF and LPF are normally highly attenuated and the corresponding amplitudes could be masked under the noise floor of the capture instrument. Increasing the frequency resolution might be unacceptable because of test time requirements (big number of samples). The performed measurements using reciprocal characteristics showed up good results and more in -depth investigation is worthwhile.

2. The base of the DSP based method is the measure of the amplitude of known spectral components (frequency bins). The presence of frequency instability or jitter could have very serious impact on the accuracy and the repeatability of test results. The distribution of the test results in this case might have higher value for σ. In some cases it might become a double distribution. Lowering F_{res} by the purpose of integration the neighboring spectral bins within the effective range of the jitter will lift up the noise level of the measurement. The other way round - seeking for higher accuracy of measuring amplitudes close to the noise levels (poorer F_{res}) will lead to higher inaccuracy and worsen the repeatability. In that kind of cases a compromise should be looked for. One efficient solution would be the implementation of a test technique looking not for the calculated spectral bin of the fundamental but for the maximum amplitude within a certain range in frequency domain. If this frequency range is carefully defined representing with some guard banding the peak values of the jitter, than the higher amplitude within it might be considered as the one of interest. In other words - the so proposed peak-search method could effectively take place for accurate and stable measurements whenever jitter is presented. A major constraint for applying such kind of method is that the jitter maximum value must be less than the spacing between the neighboring elements of interest in the measured spectrum.

When VGA is under test monotone signal is applied at the input. The input amplitude for the different gain levels is calculated by the test program so that at the output to have constant amplitude within the input dynamic range of the capture instrument. This guaranties minim level of introduced noise and harmonic distortions in the measured signal as well highly repeatable measurement results. Not least, avoiding switching the capture instrument input ranges for different amplitudes saves test time - cost.

DSP based methods has taken place by realization of the following tests:

- RF Rx: Rx gain, Rx IIP3, Rx in band power contributed by off band interferers, Rx noise figure;
- RF TX: TX spectrum, TX carrier rejection tuning, TX image rejection tuning;

The choice of the test methods to be employed is not only based on the advantages they give but on the study of a real device measurement, with the purpose to investigate the repeatability of the tests. A criterion for quotation of a particular measurement is the value of C_p - process capability. It is defined according to:

$$C_p = \frac{(\text{USL-LSL})}{6\sigma}\ , \tag{7}$$

where USL, LSL are the engineering limits for the corresponding measurement. Criteria for stability of a test result is its distribution to show up $C_p > 20$ after repetition of the test over one and the same device 100 times. This way the widening of the distribution of the test result because of its instability is eliminated and in cases of marginal to the test limits distribution the yield is improved.

VI. Conclusions

This article analysis the employed methods for testing of the main building blocks of the analog part of an ASSP. It is pointed on the advantages of the proposed methods and on the potential problems as well. Approaches for resolving the problems are suggested:

- Approach for development of DSP based tests.
- Considerations for choosing F_{res}.
- Considerations for choosing the test methods and the criteria for their quotation in a particular engineering project.
- Description of some typical engineering solutions for test of specific analog blocks.
- Test method proposed for solving jitter caused test problems.

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