Generation of a Test Strategy for Testing the Digital Part of an Integrated Circuit for Digital Wireless Short-Range Communication

Rumen Iv. Arnaudov[1] and Ivo G. Aldimirov[2]

Abstract – **Subject of this article is the generation and application of a Test strategy for measure and test of Application Specific Standard Product (ASSP) Integrated Circuit (IC) for digital wireless communication. It is given a description of the employed methods for testing the building blocks of the digital part of the device. They are based on the way they take place in the industrial test of the mixed-signal IC. Comment and quotation on some existing methods is made. It is emphasized on some potential problems that might influence the test time/cost, the accuracy and the stability of the tests. Suggestions for solving some of those problems are made.**

Keywords – **industrial test, mixed-signal Integrated Circuit, test methods, digital tests.**

I. Continuity Test [2]

Continuity test is included in the group of the digital tests because for its execution the digital hardware resources of the mixed-signal tester are used. The continuity tests are executed as a rule in the very beginning of the test program. The purpose of this test is to check the presence of the ESD protection structure of every functional pin of the device. Thus the reliable contact between the device under test (DUT) and the test hardware load board (LB) during the test program run is verified. Although simple this is very important test as it eliminates possible issues caused by misalignment of the docking system - handler to test head. It also prevents activation of potentially device and/or test hardware damaging functions when lack of continuity had occurred.

Major problem with this test is the test coverage versus the test time. Testing devices with big number of pins means multiplied test time hence cost increase.

All the supply pins are connected to GND and current is sourced to the functional pins. Then the voltage drop over the ESD structures towards VDD is measured. Afterwards the current direction is changed and the voltage drop over the ESD structures towards VSS is measured.

In general there are two approaches for performing the continuity test - parallel and serial. Serial test of the pins is a method with 100% coverage but is too slow and thus costly. The parallel method is fast because it uses the so-called per-pin - measurement units of the tester digital hardware.

Unfortunately there is one potential problem that must be considered up front. Whenever there is a short between two neighbouring pins it will result in the expected voltage drop over the ESD structure and the pins will pass the test undetected. The serial approach would not allow this. Third more economical approach should be used balancing between the test cost and the test coverage. Combination of the above-mentioned methods is widely used and is executed on two passes. On the first pass every other pin is being tested while the rest of the pins are connected to GND. The next half of the pins is tested on the second pass. The result of the combination of the two approaches is maximum test coverage and acceptable cost.

II. Digital Tests - Iddq Measurement Method. [1-4]

The purpose of this method is to find out the presence of structure defects in the digital part of the device. The number of the used CMOS inverter cells or gates is normally used for description of the complexity of the digital part. Whenever the device has relatively high complexity of the digital, the test of every CMOS cell would be highly time-consuming thus unaffordable or in many cases even unfeasible. To test the presence of defected inverter cells the Iddq test method is widely used.

Iddq is the supply current consumed by the digital part when it had been driven to a static state (no switching inside) with all outputs left open. Automatically generated test pattern (ATPG) driving the digital part is stopped at the so called Iddq vectors where the majority of the P or N gates are in static state - only the P or the N transistors are in ***on*** state.

Fig. 1 shows CMOS inverter cell in a static state.

Obviously the current flowing into the inverter is negligible and is multiplied by the number of the gates in the digital structure. This way measuring the static current consumption after the ATPG pattern had been stopped at the predefined Iddq stop vectors, conclusion for possible defects presence can be drawn.

Whenever a digital part with high complexity has to be tested the Iddq measurement method is used as a rule in the silicon testing industry. The coverage of the method is specified by the digital design that generates the Iddq vectors.

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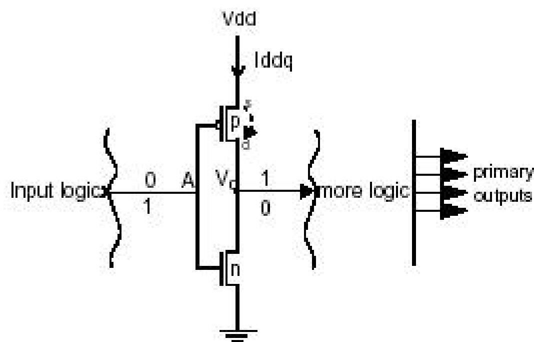

Fig. 1.

Depending of the technology used, the gates number and the temperature, the Iddq value varies and is in the range of few hundreds nano Amperes.

In the modern industrial mixed-signal testers the power supply units are integrated with the measurement facilities for measuring the supplied currents and voltages. In normal working mode the digital part normally consumes several mAmps. Stopping at Iddq vector quickly reduces the consumption down to hundred times.

Applying traditional approach may come across serious problems trying to make quick and accurate measurement of such a quickly switched low value current. Fig. 2 shows in principle the power supply for the digital part of a mixed-signal device and the parasitic capacitance of the supply lines.

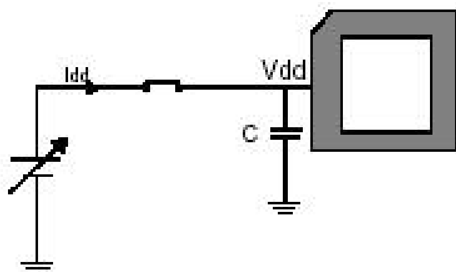

Fig. 2.

For accurate measurement of this many times lower current consumed by the same supply pin, the measurement range of the power supply unit has to be switched over. During this switch over, the inductance of the supply lines and the parasitic capacitance between them cause transients that might last for a number of milliseconds. It has to be added relevant amount of wait time before the real measurement to take place and eventually some filtering and DSP technique have to be used for averaging the measurement result. When digital design had been generated ***n*** numbers of Iddq vectors i.e. ***n*** times run of the test pattern and measure of Iddq, the test time is ***n*** times multiplied including the settle time which in many cases might be unacceptable. Some sources [4] give hardware methods for increasing the low current measuring accuracy, but the major problem - the settling time of the Iddq current that is multiplied by the number of the stop vectors is unresolved. In those cases it is not guaranteed that transients would not occur, more over in some specific cases the Iddq current even shows up oscillations. Possible and with certain efficiency solution would be the implementation of a second current source in parallel to the main one, programmed to provide (and measure) current in the expected range. RC product then could be added on this second supply line to lower the settling time of the switch over process and to produce stable and repeatable test results.

III. ADC/DAC Transfer Curve Tests [2]

There are many similarities testing ADC and DAC and few noticeable differences. The primary difference is the transfer curve - for each input code the DAC generates different output voltages as for a number of input voltages the ADC generates same output codes. Fig. 3 shows the transfer curves of both devices.

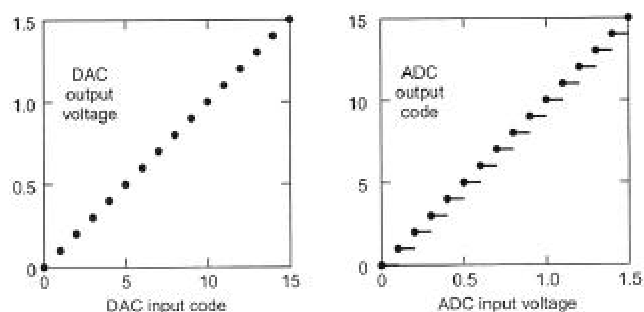

Fig. 3.

IV. DAC test

The transfer curve is being taken during linear (ramp up) increase of the input code. Best definition of the DACs parameters is found by computing the best-fit line. This approach is most preferred, as it is independent of the bit number.

A best-fit line is commonly defined as the line having minimum squared errors between its ideal, evenly spaced samples and the actual DAC output samples. Having this result in hand it is possible to calculate parameters of interest such as:

- **Monotonicity.** Monotonicity testing requires taking the discrete first derivative of the transfer curve, denoted here as $S(i)$, according to

  $$S(i) = S(i+1) - S(i)\ ; \tag{1}$$

  If derivatives are all positive for a rising ramp up input, then the DAC is said to be monotonic.

- **Differential nonlinearity**. The DNL curve represents the error in each step size, expressed in fractions of LSB. DNL is computed by calculating the first derivative of the DACs transfer curve, subtracting one LSB (i.e. V_{lsb}) from the derivative result, then normalising the result to one LSB:

  $$\mathrm{DNL}(i) = [S(i+1) - S(i) - V_{lsb}]/V_{lsb}, \mathrm{LSB}\ ; \tag{2}$$

- Integral nonlinearity. The integral nonlinearity curve is a comparison between the actual DAC transfer curve and the best-fit line.

$$\text{INL}(i) = [S(i) - S_{ref}(i)]/V_{lsb}, \text{LSB} \; ; \qquad (3)$$

V. ADC Test - Linear Ramp Histogram Method

This method implies applying of a rising or falling linear ramp signal to the input of the ADC and collect samples from the ADC at a constant sampling rate. The ramp is set to rise or fall slowly enough that each ADC code is hit several times for example 16 or 32. The number of occurrences of each code is directly proportional to the width of the code. From the so acquired transfer curve the average value of the input voltage for each output code is calculated. The width of each code word - code width (i) in LSB is calculated according:

$$\text{code width}(i) = H(i)/h, \; i = 1, 2, ..., 2\text{pow}N - 2 \; , \qquad (4)$$

where N is the number of the ADC bits, $H(i)$ is the number of the hits for the i-th word and h is the average number of hits for each code word.

For computing the best fit, INL and DNL curves it is used the histogram of the acquired results after their normalisation as it is shown on Fig. 4.

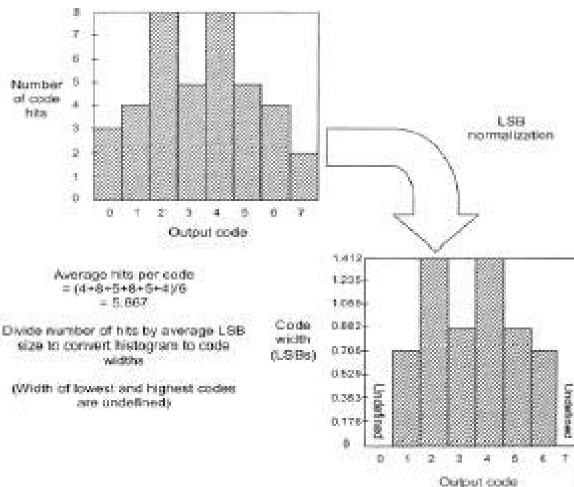

Fig. 4.

Based on the such obtained by the method results INL and DNL are calculated according to:

$$\text{DNL}(I) = \text{LSB}_{\text{code width}}(I) - 1, \qquad I = 1, 2, ..., 2\text{pow}N - 2 \; ; \qquad (5)$$

$$\text{INL}(I) = \sum_{k=1}^{I-1} \text{DNL}(k), \qquad I = 1, 2, ..., 2\text{pow}N - 2; \qquad (6)$$

◇ Local oscilator test - PLL

Although the ”analog” uses of the PLL, from the tester hardware and the employed test method point of view this is purely a ”digital” test. The purpose of the test is to determine the following parameters:

- *lock_time* or the settle time of the VCO for the programmed frequency;
- read out of the DTUNE code which shows up the automated digital tuning;
- CTUNE code representing the automated choice of capacitors bank for compensation of the process spread.

External clock signal is applied and using JTAG protocol it is asserted in the corresponding register the code of the channel (the working frequency). The time till synthesizer_lock goes high is measured - the VCO had settled. Using JTAG protocol the registers containing *DTUNE* and *CTUNE* codes values are read out. The test is executed twice - for the frequencies at the two ends of the working range. The described method practically covers the main PLL parameters and because of its relatively low complexity is cost/test time saving. The use of JTAG as a design for test (DFT) technique for the digital part of the IC provides the opportunity for fast and convenient from test engineering point of view test.

VI. Conclusions

This article analysis the employed methods for testing of the main building blocks of the digital part of an ASSP. It is pointed on the advantages of the proposed methods and on the potential problems as well. Approaches for resolving the problems are suggested:

- It is commented on a balanced approach for execution of continuity tests.
- It is pointed on some possible measurement problems which Iddq current test may come across and on a possible efficient solution for it.
- It is given a description of quick and effective method for testing PLL.
- It is commented on the basic notions of the ADC/DAC test and the way they take place in the industrial tests.

References

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[3] Catalyst Mixed-Signal Programming, *Teradyne Inc*, March 2000.

[4] **Keywords** - <*www.ttt.com*> Copyright (c) 1996,1997 T.T.T., Inc.