Statistical Analysis and Optimization of Voltage Regulator Circuit Using IESD and ORCAD Environment

Galia I. Marinova[1] and Dimitar I. Dimitrov[1]

Abstract – **The paper presents the development of a specialized methodology for statistical analysis and optimization for a voltage regulator circuit. The study is performed in the environment of the simulators ORCAD PSpice 9.2 and IESD. Optimization steps and results from circuit simulation are presented. Conclusions for implementation of the voltage regulator circuit are deduced.**[1]

Keywords – **statistical optimization; voltage regulator circuit.**

I. Introduction

The general methodology for statistical analysis and optimization in electronics is presented in [2]. However different circuits types demand specific implementation of the general methodology. The paper presents a specific implementation of the general methodology for statistical analysis and optimization on a voltage regulator circuit. The tools applied are the statistical simulator IESD, described in details in [2] and ORCAD PSPICE 9.2 [3]. The case study is performed for a linear voltage regulator circuit which is used for power supply in antenna preamplifiers and it is presented on Fig. 1. The circuit is described in details in [1]. The study which is performed in the statistical design environment and the specific methodology developed allows to verify the circuit parameters from [1] , to determine optimal part values and tolerance values with 100% yield over predefined constraints in the Goal function and to enlarge the circuit application area.

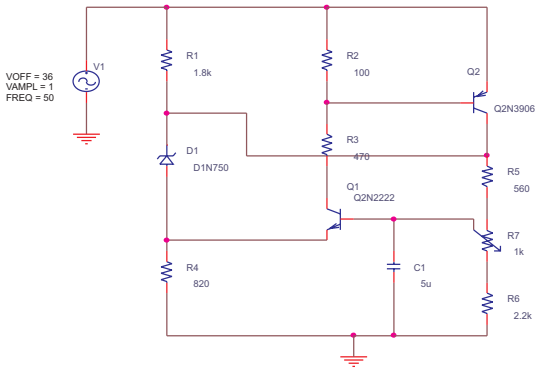

Fig. 1. Voltage regulator circuit

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II. Steps of the Specific Methodology for Statistical Analysis and Optimization of the Voltage Regulator Circuit

The specific methodology developed for the statistical analysis and optimization of the voltage regulator circuit includes the following steps:

- Specification and constraints definition ;
- Nominal analysis and initial choice for part values;
- Statistical analysis of the voltage regulator circuit in ORCAD PSpice 9.2 and in IESD;
- Definition of the Goal function for statistical optimization;
- Statistical optimization of the voltage regulator circuit in IESD with optimal tolerance determination;
- Nominal and statistical simulation of the voltage regulator circuit in a realistic system.

The specific methodology steps are described in details.

III. Description of the Specific Methodology Steps

A. *Specification and Constrains Definition*

The specification of the voltage regulator circuit is:

- The input voltage applied at node IN can have 3 definitions for DC value and pulsation amplitude: 36 V$\pm$1 V, 29 V$\pm$1.2 V and 39 V$\pm$0.8 V. Two frequency values are possible: 50 Hz and 60 Hz.

The constraints are the following:

- The voltage obtained at the output node STAB should be with DC value:24 V with pulsation amplitude inferior than $\pm$10 mV. So the pulsation amplitude at the output should be at least 100 times inferior than the input pulsation amplitude.

B. *Nominal Analysis and Initial Choice for Part Values*

Nominal time analysis in PSpice is performed in order to define the optimal values for R5 and R6 which replace the resistors R5, R6 and the variable resistor R7 from Fig. 1 insuring the constraints from point 2.1 and corresponding to the transistors and diodes chosen. Fig. 2 presents the voltage regulator circuit with new values of R5 and R6. The results from nominal transient analysis in PSpice are shown on Fig. 3.

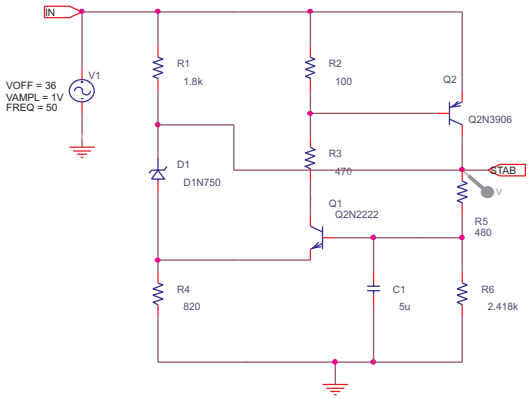

Fig. 2. R5 and R6 values defined from nominal simulation in ORCAD PSpice 9.2

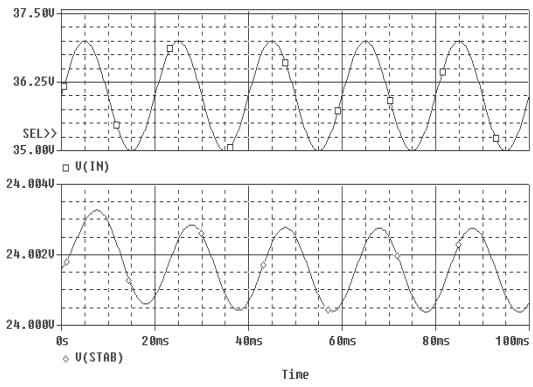

Fig. 3. Applied and stabilized voltages for the circuit from Fig. 2

The nominal analysis is performed for an open circuit. Six cases for the input source V1 definition are estimated: the analysis is performed for two frequencies – 50 Hz and 60 Hz and three groups of DC and amplitude pulsation values : 36 V±1 V, 29 V±1. 2V and 39 V±0.8 V. The results from nominal simulation in these 6 cases are presented in Table 1.

Table 1.

Case	Frequency FREQ	Input voltage V1 source V(IN)		Output stabilized voltage V(STAB)	
		DC value	Pulsation amplitude	DC value	Pulsation amplitude
1	50Hz	36V	1V	24.0010V	± 1.5mV
2	50Hz	29V	1.2V	23.9685V	± 1.5mV
3	50Hz	39V	0.8V	24.0143V	± 1mV
4	60Hz	36V	1V	24.0016V	± 1mV
5	60Hz	29V	1.2V	23.9685V	± 1.5mV
6	60Hz	39V	0.8V	24.0143V	± 0.5mV

The results from Table 2 confirm the good performance of the studied voltage regulator circuit both on 50 Hz and 60 Hz input source. The DC values of the stabilized voltage are similar for both frequencies and the pulsation amplitudes are even lower for the 60 Hz case. The output voltage parameters are good for the 3 cases for DC values and pulsation amplitudes of the input voltage source.

Table 2.

Tolerances for all R and C	DC value variation	Pulsation amplitude variation
1%	-0.4V +4.031V	1.2-1.23mV
5%	-2.747V +4.031V	2-3mV
15%	-4.9V +3.744V	2-3.06mV

C. *Statistical Analysis of the Voltage Regulator Circuit in ORCAD PSpice 9.2 and in IESD*

The circuit from Fig. 2 is analyzed statistically in ORCAD PSpice 9.2. A full Monte Carlo analysis in Time area is performed with 1%, 5% and 15% for all R and C values in the circuit. The variations for the DC value and for the pulse variation for the stabilized voltage V(STAB) is estimated through the option PERFORMANCE ANALYSIS. The DC value variation is calculated with YatX(V(STAB), 30.03 m) and the pulsation amplitude variation is calculated with SWING(V(STAB),20 ms,40 ms).

The results in Table 2 show the very strong stability of amplitude pulsation values . Their value cover the constraints with no dependence from the tolerance values.

A statistical analysis of the voltage regulator circuit in IESD with estimation of the statistical behavior of the transistor Q1 is performed. The transistor 2T6552D is used for Q1. This transistor has a statistical model in IESD and Monte Carlo simulation in performed with the use of this statistical model.

Table 3 present the variations for the stabilized voltage parameters. Fig. 4 presents results from statistical processing in IESD. Fig. 4a presents the histogram for DC value of the stabilized voltage for 1% tolerances on all R and c and statistical model for Q1 and Fig. 4b. presents the linear correlation between the variations of the DC value and the Pulsation amplitude for V(STAB).

Table 3.

Tolerances for all R and C	DC value variation	Pulsation amplitude variation
1%	22.43V 24.8V	0.1 – 1mV
5%	13.367V 25.266V	0.15 – 2mV

The results from the statistical simulation of the voltage regulator circuit in IESD show that the statistical behavior of the circuit is strongly depending from the statistical behavior of the transistor. The transistor 2T6552D is not suitable for the realization of this voltage regulator circuit. Other remark is that there is an inverse linear correlation between the variations of the DC value and the Pulsation amplitude for V(STAB) which corresponds to practical experiments with the circuit and described in [1].

Table 4.

Parts	Tol Step1	Tol Step2	Tol Step3	Tol Step4	Tol Step5	Tol Step6	Tol Step7 Optimal results
R1	**1%**	**2%**	**3%**	**5%**	**10%**	**15%**	**15%**
R2	**1%**	**2%**	**3%**	**5%**	**10%**	**15%**	**15%**
R3	**1%**	**2%**	**3%**	**5%**	**10%**	**15%**	**15%**
R4	**1%**	**2%**	**3%**	**5%**	**10%**	**15%**	**10%**
R5	**1%**	**2%**	**1%**	**1%**	**1%**	**1%**	**1%**
R6	**1%**	**2%**	**1%**	**1%**	**1%**	**1%**	**1%**
C1	**1%**	**2%**	**2%**	**5%**	**10%**	**15%**	**15%**
V(STAB) DC Value variation	**+0.283V -0.169V**	**+0.558V -0.365V**	**+0.280V -0.169V**	**+0.290V -0.186V**	**+0.394V -0.229V**	**+0.511V -0.270V**	**+0.462V -0.300V**

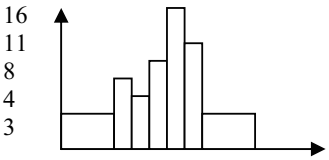

Fig. 4a. Histogram for the DC value of the stabilized Voltage with 1% tolerances for R and C and statistical model for the NPN transistor in IESD, 31% being discarded as too sharply differing values

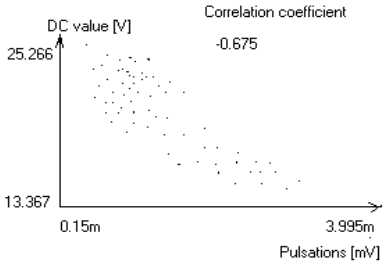

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Fig. 4b. Linear correlation between the variations of the DC value and the Pulsation amplitude for V(STAB)

D. Definition of the Goal Function for Statistical Optimization

Taking in consideration the results from the statistical analysis of the voltage regulator circuit described in previous paragraph the statistical optimization task is defined as follows:

- The objective is to perform optimal tolerancing for the circuit from Fig. 2 with 100% yield following the specification constraints defined in point A;
- tolerancing is limited only on R and C elements and statistical models of transistors and diods are not taken in consideration.

The goal function for statistical optimization of the voltage regulator circuit is to find the maximal tolerance values of all R and C in the circuit which guarantee 100% yield on the constraint for DC value variation for the stabilized voltage V(STAB) ± 0.5 V. The goal function is formulated as follows:

– Max Tol (R1, R2, R3, R4, R5, R6, C1),

– V(STAB) [V(1)=DC 36 V ; Pulse amplitude=$\pm$1 V] : DC 24 V$\pm$0.5 V; Pulse Amplitude $\leqslant \pm 0.01$V]

E. Statistical Optimization of the Voltage Regulator Circuit in IESD with Optimal Tolerance Determination

Since the response to constraints for pulsation amplitude is proved to be independent from tolerances only, the constraint for the DC value variations is considered in the optimization process. Table 4 presents the DC value variation at the different optimization steps for the tolerances of R and C in the circuit for the prescribed tolerance values.

At any step, a full Monte Carlo time domain analysis is performed in IESD. 100 transient analysis are executed for the randomly generated R and C values. The constraint for the DC value of the stabilized voltage is verified for each one of these circuits. If there is not a failing circuit all tolerances are increased If there is a randomly generated circuit which fails, the random values for R and C are inspected and those with the biggest deviations from the nominal values are identified. The corresponding tolerances are decreased at their previous values and they are no more increased up to the end of the optimization procedure. The procedure stops when all tolerances are definitely defined.

F. Nominal and Statistical Simulation of the Voltage

Fig. 5 presents the voltage regulator circuit included in realistic system.

The circuit from Fig. 5 is simulated nominally and statistically. Fig. 6 presents the nominal response – Input voltage V(IN), Voltage on C2 (V(C2:2)) and Stabilized voltage V(STAB). The statistical simulation implements the optimization results from point E (Step 7 in Table 4). The capacitor C2 is considered with 15% tolerance value. Fig. 7 presents the results from statistical simulation for V(STAB) and the histogram for the DC value of V(STAB). The variations for the DC value of V(STAB) and for the pulsation amplitude of V(STAB) are estimated from the statistical simulation results on Fig. 7, as follows:

DC value variation calculated with YatX(V(STAB), 30.03 m) : -0,3781 V to +0.2877 V (DC values are: 23.6221 V to 24.2877 V.

Pulsation amplitude variation calculated with SWING(V(STAB),20 ms,40 ms):1.02 mV to 1.45 mV.

These results confirm that the optimization results are good enough for system implementation of the voltage regulator circuit.

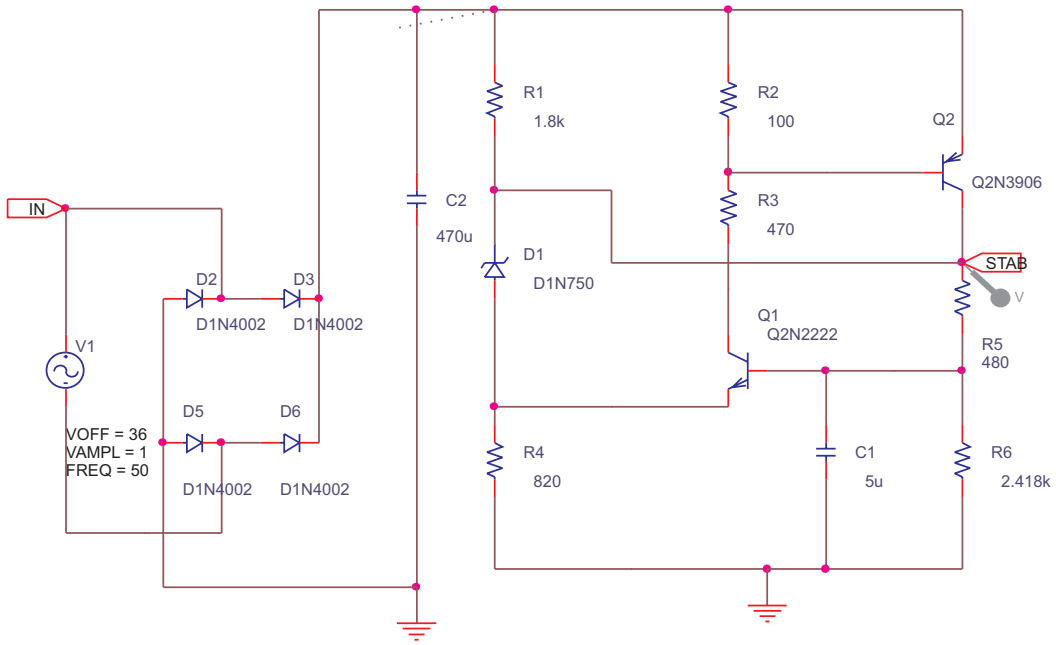

Fig. 5. Voltage regulator circuit in realistic system

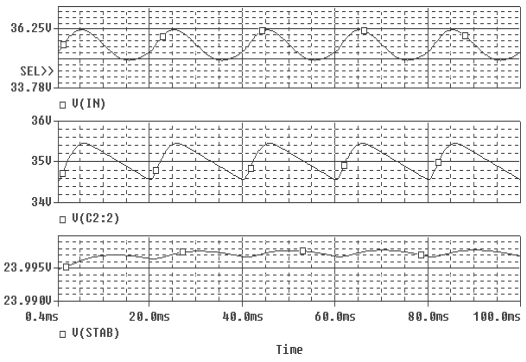

Fig. 6. Nominal response – Input voltage V(IN), Voltage on C2 (V(C2:2)) and stabilized voltage V(STAB)

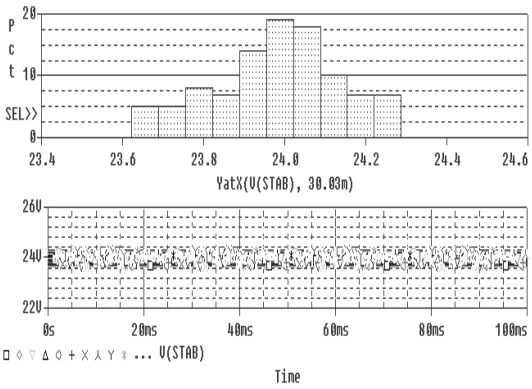

Fig. 7. Statistical simulation for V(STAB). Histogram for the DC value of V(STAB).

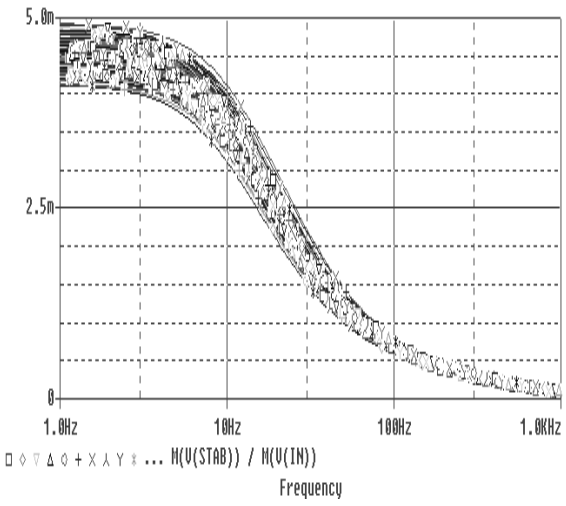

Fig. 8. Statistical simulation of the gain curve

IV. Conclusion

The paper presents a specially developed methodology for statistical analysis and optimization of a voltage regulator circuit.

The voltage regulator circuit studied in the paper is implemented in the TV sets OSOGOVO (SOFIA 11). The application of this methodology permitted to study and to confirm several characteristics of the voltage regulator circuit and to enlarge its application implementation area:

The voltage regulator circuit is suitable for an enlarged voltage supply range both for the European energy net (50 Hz, 220 V±15%) and for the American energy net (60 Hz, 110 V±15%). This conclusion is coming from nominal simulation results in Table 1 and statistical simulation results on Fig. 8 and Table 5.

The statistically optimized voltage regulator circuit with tolerances defined at Step 7 in Table 4 can be realized with hybrid IC technology. If better accuracy is demanded

Table 5.

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a monolithic technology could be applied.

The voltage regulator circuit is suitable for implementation in large band amplifiers and antenna amplifiers. With a little modification, decreasing the stabilized voltage at 15 V, it could be used for positive power supply for operational amplifiers.

The methodology developed will be implemented in further research on load curve, enlarged inverse current characteristic and security chain activation in the voltage regulator circuit.

The experiences performed confirm the interest in specific methodologies development for different types of circuits.

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