Modeling of a Control System of a Transistor Resonant Inverter

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Abstract - **The paper presents a control system of an induction heating transistor resonant inverter operated above the resonant frequency. The self-oscillating control system allows deep control of the inverter output power, by varying the duration of the transistors turn-on time. Control system is described using Analog Behavioral Modeling (ABM) feature provided in OrCAD PSPICE.**

Simulation and experimental results from the investigation of the induction heating transistor inverter are shown.

Keywords – **transistor resonant inverter, control system, induction heating, OrCAD PSpice.**

I. Introduction

There are modern methods for deep regulation of the output power inside the resonant inverter [2], [4], [5]. At the same time the input DC source can be uncontrolled. A method for output power control of resonant inverters, belonging to this group of methods, which has not been thoroughly studied, is based on the change in the transistors turn-on time [2], [4].

The block-diagram of the inverter control system is presented in [2], by which can be realized the given control principle.

In this paper the investigations are extended and the specific variant of the induction heating transistor resonant inverter controls system operated above resonant frequency is proposed.

The control system is described using Analog Behavioral Modeling (ABM) feature provided in OrCad PSpice [3].

II Circuit description and operation

Fig.1 shows the full-bridge induction heating transistor resonant inverter. The power switches used in the circuit are MOSFET transistors.

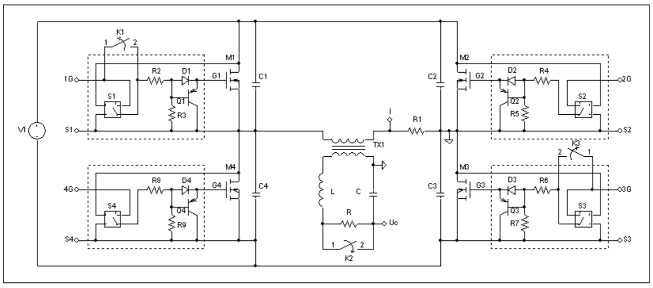

Fig.1. Full-bridge induction heating transistor resonant inverter

The series compensation of the inductor R-L is achieved with the capacitor C and by means of the high-frequency transformer TX1 is obtained a proper match between the inverter and the load.

The inverter circuit is operated above resonant frequency. The transistor individual control circuits are introduced.

These circuits feed the gate drive pulses of the corresponding transistor, if at the individual circuit input has drive signal and the transistor drain-source voltage is practically zero. This control method can be better understood by looking at the waveforms shown in fig.2.

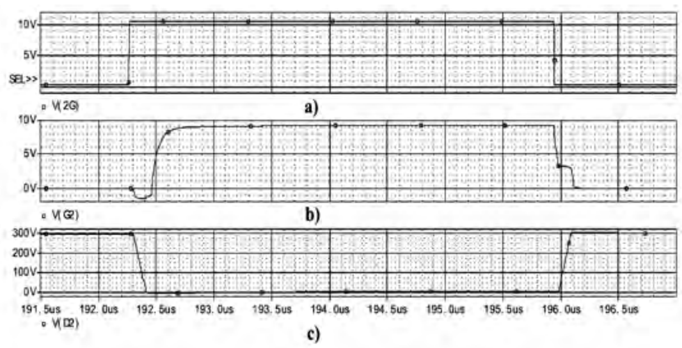

Fig.2. Individual control circuit – a) input driving signals and b) output driving signals. c) The transistor M2 drain-source voltage.

The drive pulse appears on the transistor M2 individual circuit input (fig.2a) immediately after the transistor M3 is turned off, because the two transistors are operated with the voltages, dephased at 180^0.

The drain-source voltage of the M2 (fig.2c) becomes practically zero, after the snubber capacitors C2 and C3 are recharged.

In this way, only by zero voltage of the transistor M2 (ZVS), the gate drive pulse (fig.2b) is ensured.

Like a parameter for deep control of the inverter output power is used normalized transistor turn-on time t'_{VT} [2].

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The inverter has fixed characteristics typical for a voltage source, when $1>t'_{VT}>0{,}45$. In this interval of the parameter's t'_{VT} change, measures should be taken to limit the current in the resonant circuit, in the case of an overload or a short-circuit. The inverter can be considered as a current source, stable at short-circuit mode, when $t'_{VT}<0{,}45$.

III. CONTROL SYSTEM OF THE INVERTER

The control system is described using Analog Behavioral Modeling (ABM) [6]. The ABM feature provided in OrCad PSPICE allows for flexible descriptions of electronic components in terms of transfer function or lookup table. In other words, a mathematical relationship is used to model a circuit segment so the segment need not be designed component by component. Moreover, the combination of significant calculation efficiency with adequate component's modeling is achieved [3].

Fig.3 shows the proposed control system (CS) and fig.4 – the waveforms in significant points, which explain the system operation.

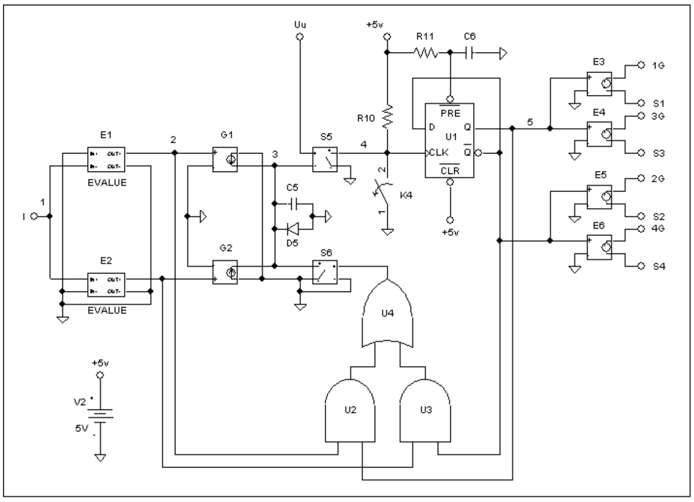

Fig.3. Inverter control system

The operation of the CS is synchronized with the current **i** in the primary transformer winding.

The resistor R1 senses the current trough the resonant link. This information is delivered of the controlled voltage sources (E1, E2), realizing a zero detector, which tracks the resonant current zero crossing.

The shaped pulses (fig. 4a) start the sawtooth voltage generator (fig. 4b), formed by the capacitor C5 and controlled current sources G1 and G2.

The voltage increasing time is equal to the transistors turn-on time - t_{VT}. It by the voltage Uu is formed (fig. 4b).

Uu is delivered on the comparator input, designed with voltage-controlled switch S5. The sawtooth voltage generator (SVG) output is sent to another comparator input. The comparator output shaped pulses (fig. 4c) are used to zeroing SVG and at the same time, are fed to the flip-flop trigger U1. The pulse distributor U1 forms two channels of the control pulses, dephased at 180^0 (fig. 4d). The dependent voltage sources E3÷E6 provide the required power, amplitudes and galvanic separation of the control signals.

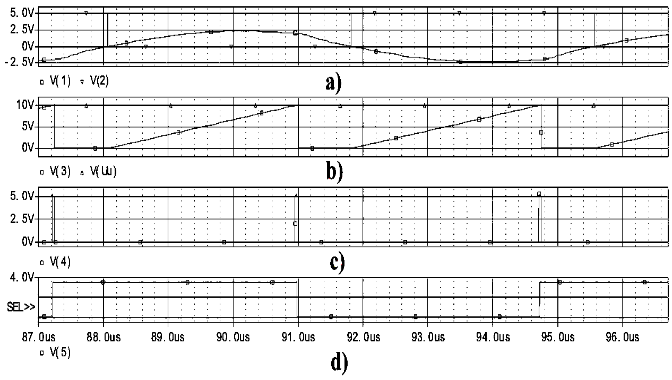

Fig.4. Control system main waveforms

Fig.5 circuit realizes the peak current limit of the inverter, which is fixed through V3 (signal Limit-I), in an advance specified level. The turn-on time of the transistors is achieved through V4, R14, and C9 -signal Time-VT. The peak detector current is formed on S7-S9, U5, E7 and C7, as the current peak value for each half period is stored in the capacitor C7. In fact, this storage is obtained at the moment that corresponds to the zero crossing of the compensating capacitor voltage.

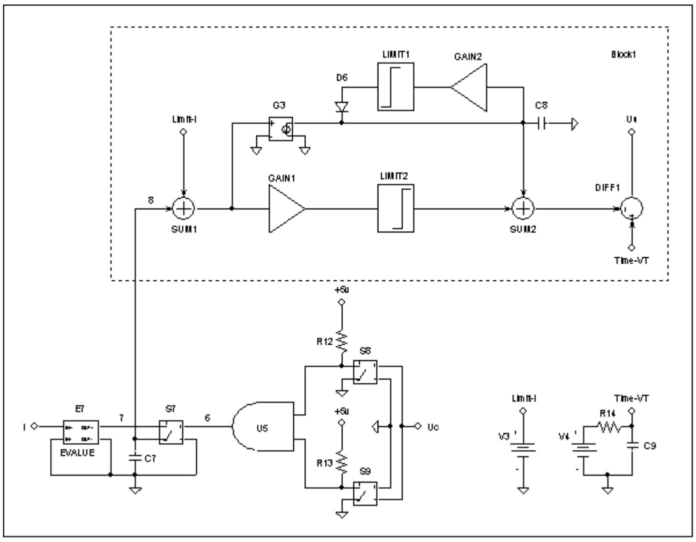

Fig.5. Peak current limited circuit of the inverter

The voltage of the capacitor C7 is compared to the signal Limit-I and according to the PI low (realized by means of the Block1 circuit) changes control signal Uu, thus the transistors turn-on time is decreased. The signal Uu is equal to the signal Time-VT, if the peak current is smaller than the previously specified value.

The peak current limited circuit operation is illustrated, as in the inverter from fig.1 the short circuit mode is simulated by switch K2. Fig.6 and fig.7 show the waveforms, explaining these processes.

From the waveforms are seen that the transistors turn-on time is decreased automatically (fig.7c), after the failure mode has occurred. This is the reason for the limitation of the resonant current.

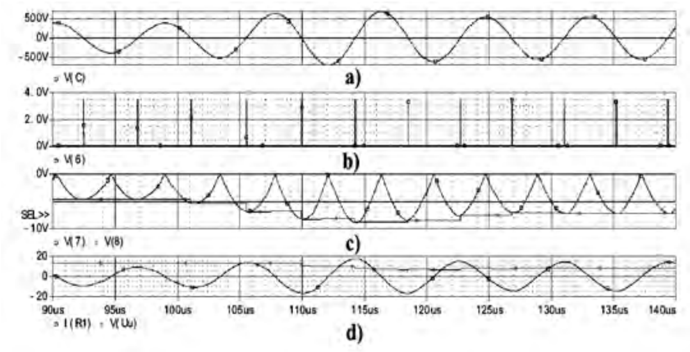

Fig.6. Inverter peak current limited circuit main waveforms

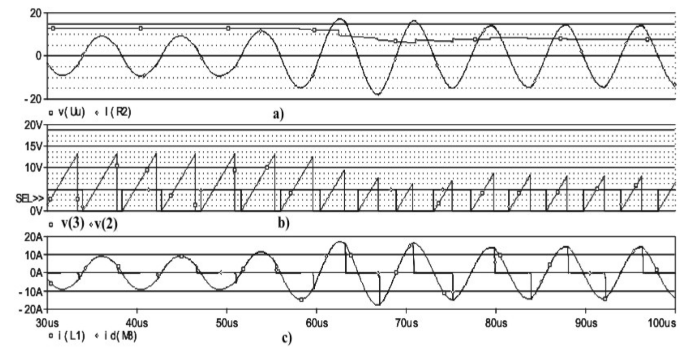

Fig.7 Transistor resonant inverter and control system waveforms in short circuit mode

IV. Experimental results

Based on the above consideration, the stomatology purposes induction melting resonant inverter of the small quantity of Ni-Cr-Co alloys and noble metals was built up and tested. The inverter dc power supply voltage is the rectified single-phase ac supply, the output power is 3kW and the operation frequency at the rated load is 115kHz. MOSFET transistors, type IRFP450 have been used. The heating inductor has inside diameter 40mm, height 40mm and number of turns – 4.

About 50g of melting Ni-Cr-Co alloy is put on the ceramic pot. Under these condition the inductor parameters from [1] are $L=1{,}54\mu H$ and $R=0{,}13\Omega$.

A series compensation and a proper match between the heating inductor and the load are obtained by the capacitor $C=0{,}95\mu F$ and reducing transformer (ferrite core section $S=840mm^2$ and number of turns $w_1=20$; $w_2=2$).

Fig.8 shows the working point trajectory during the semiconductor switches commutation. This trajectory is favourable, because it is found near the i(u) coordinate axis.

The transistor commutation losses are proportional to the area enclosed by the trajectory and they reduce with increasing the snubber capacitors value. During the experiment snubbers' value is 1nF.

Fig.9 shows transistor voltage and resonant link current at the rated load.

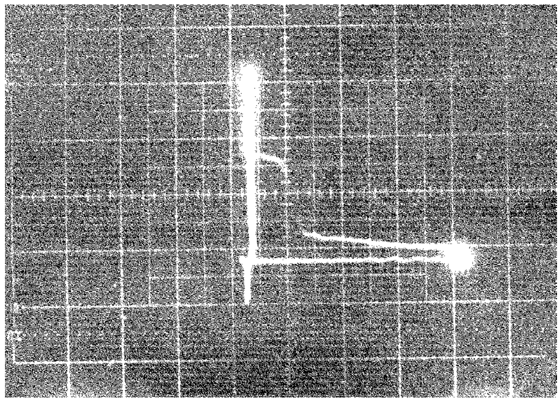

Fig.8. Trajectory of the working point at commutation of the transistor (x=50V/div.; y=5A/div.).

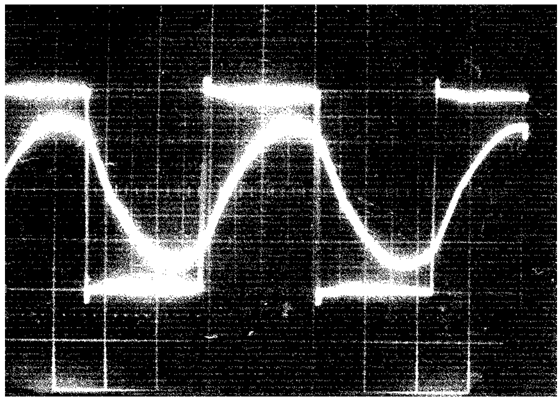

Fig.9. Voltage of the transistor-50V/div and current through the resonant circuit-10A/div. (x=2μs/div.).

V. Conclusions

The proposed control system ensures deep regulation of the inverters output power, by varying the duration of the transistors turn-on time.

Each transistor owns an individual control circuit, which allows the devices turn-on only by zero voltage (ZVS). As a result of the introduced current limited system, the inverter stays efficient even nearly short circuit mode.

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