Optimization of output spectrum of direct digital synthesizers for application in hybrid frequency synthesizers

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Abstract- **Investigation of the output spectrum of direct digital synthesizers for best performance in hybrid DDS and PLL synthesizers. Optimization of the connection between the output of the DDS and the output filter for best impedance matching.**

Keywords- **Direct Digital Synthesizers, noise, spurious and alias frequencies, output filters impedance matching.**

I. INTRODUCTION

Direct Digital Frequency Synthesis (DDFS) becomes a very popular technique for generating frequencies whenever very precise frequency resolution and fast frequency switching is needed. The most common DDFS architecture includes a periodically overflowed phase accumulator, for generating and storing phase information and uses a ROM based look up table to compute the sine function. The digitally generated sine from the ROM is next passed to a digital to analog converter (DAC) where it is converted to a pulsed analog form and finally this form is filtered by a low pass filter. The frequency of the generated sine wave is controlled by the Frequency Control Word (FCW). The output frequency could be defined from Eq. (1):

$$f_{out} = FCW \; \frac{f_{clk}}{2^{j}} \qquad (1)$$

Where f_{out} is the synthesized frequency, f_{clk} is the clock frequency and "j "is the word length of the phase accumulator. The spectral density of the generated signal could be expressed with the help of the formulae, given in Eq. (2):

$$S(f) = e^{-j\pi f/f_{clk}} \frac{\sin(\pi f/f_{clc})}{\pi f/f_{clc}} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} c_m \sigma(f - nf_{clk} - mf_{out}) \qquad (2)$$

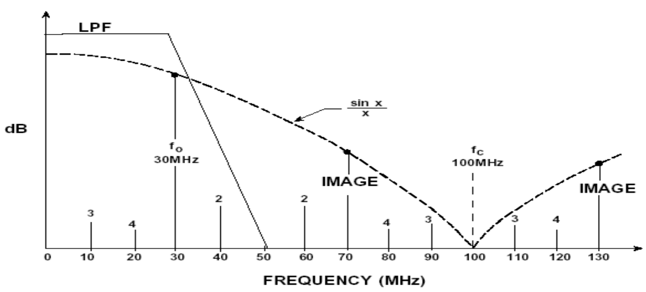

Fig.1

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As can be seen from Fig.1 the DDFS causes all frequency components residing in the generated signal to be aliased about every harmonic of the clock frequency fclk. If the output is a perfect sine wave, then the spectrum contains the frequencies $nf_{clk} \pm f_{out}$. The component, corresponding to n=0 is the desired sine wave and the others are the images or alias frequencies. It is of great importance to define the location and the amplitudes of the spurious components in the output spectrum. In many hybrid synthesizers the quality of the output signal depends to a great degree from the appropriate choice of the clearest part of the spectrum of the DDS.

For many applications, the DDS solutions have distinct advantages over the equivalent frequency synthesizers, employing PLL circuitry. These advantages could be used more completely if we know the real nature of the synthesized output sine wave in DDS. One important subject is the generation of spurious spectrum lines and the noise at the output of the DDS and the appropriate measures for diminishing their influence on the purity of the output spectrum.

In this paper the sources of the noise and spurious frequencies will be analyzed and the influence of the output impedance matching between the output of the DDS and the antialias filter on the quality of the generated signal will be discussed.

II. NOISE AND SPURIOUS SOURCES IN DDS

As we have seen before, the most dangerous and difficult to handle are the spurious frequencies, arising from the digital nature of the generated signal. But the output spectrum contains additional spurious frequencies and wideband noise, which had to be taken in consideration. The most important of them are:

1. Spurious lines and noise due to the truncation of the phase accumulator bits addressing the sine ROM.
2. Noise due to the distortion from the compression of the sine ROM.
3. Errors, due to the limited precision of the samples, stored in the ROM.
4. Noise from the nonlinearities in the digital to analog conversion.

We need to know the carrier to noise (C/N) ratio for every one of these noise and spurious sources. From [2] it is calculated that the worst case C/N caused from the truncation of the least significant bits in the phase accumulator is from Eq. (3):

$$C_t/N \approx 6.02\,K - 3.92 \quad \text{dBc} \qquad (3)$$

where k is the number of most significant bits of the phase accumulator, used for programming the ROM table.

The finite character of the quantization in the sine ROM values also leads to the output DDFS spectrum impairments. The carrier to noise ratio for this case could be calculated from Eq. (4):

$$C_q/N \approx 6.02\,m + 1.76 \quad \text{dBc} \qquad (4)$$

III. OUTPUT SPECTRUM OPTIMIZATION

A program was created in MATLAB in which all of the factors were taken in consideration. With the help of this program it is possible to choose the frequency range where the spurious frequencies have lowest values and this range could be used for reference frequency in a hybrid PLL plus DDS synthesizers. Graphical results are shown for two different frequencies for a direct digital synthesizer with accumulator length of 32 bits, 21 truncated bits and 12 bits for the ROM. The clock frequency of the DDS is 12.8 MHz.

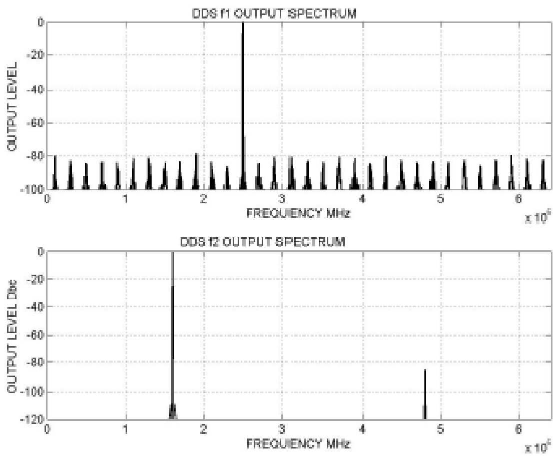

Fig.2

In high speed and high resolution (>10 bits,>50 MHz) DDFS most of the spurs are generated from the analog errors in the DAC. In the advanced high speed DDFS the DAC is the most critical component. The anomalies in the output spectrum, caused by the DAC do not follow the sin(x)/x roll off response.

The carrier to noise ratio on the output of the DAC could be defined from the well known formulae in Eq. (5):

$$C/N \approx 6.02\,n + 1.8 \quad \text{dBc} \qquad (5)$$

where "n" is the number of bits in the DAC. In almost every state of the art DDS the number of bits after truncation in the phase accumulator is big enough in comparison with the bits in the DAC, so here one can assume that the main source of wideband noise at the output of the DDS is the quantizing noise of the DAC, which can be well predicted. For an example if we take the AD9854, which has 48 bits phase accumulator, 17 bits after truncation and 12 bits DAC the C/N from the truncation can be calculated and is more than 102dB and the C/N from the DAC in this case is 72 dB.

Another important consideration is that, unlike a PLL-based system, the higher order harmonics of the fundamental output frequency will fold back into the baseband, because of aliasing. These harmonics cannot be removed by the antialiasing filter as shown in fig.1. For instance if the clock frequency is 100 MHz and the output frequency is 30 MHz the second harmonic of the 30 MHz signal appears at 60 MHz out of band but also at 100 – 60 =40 MHz, and the fourth at 120 – 100 = 20 MHz. Higher order harmonics products also fall within the Nyquist bandwidth.

The nonlinear process in the DAC is generating harmonically related spurs in the output spectrum. The amplitude of the spurs is difficult to predict, but the location of the spurs is harmonically related to the output frequency of the synthesizer. A detailed analysis could be done for every particular DAC. At this stage of the development of the direct digital synthesis it could be seen that only the lack of high frequency and linear DACs is that stops their more intense application in the frequency bands for portable and computer wireless communications. The comparatively high level of wideband noise and the presence of alias and image frequencies prevents their applications in precise measurment equipment. On fig.3 the output spectrum of the synthesizer after the DAC for two frequencies is shown. Clear degradation of the spectrum can be seen for the two frequencies.

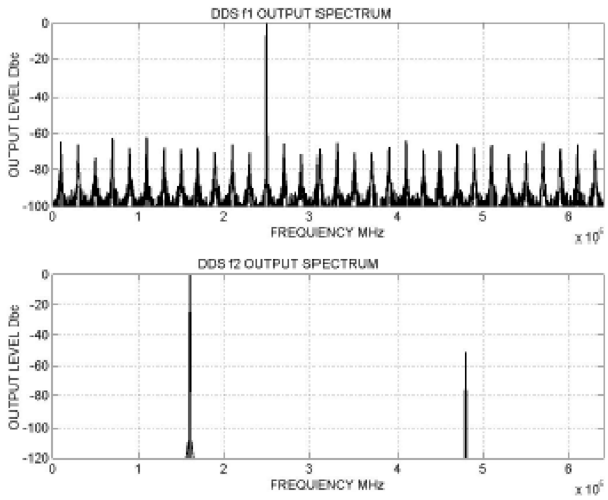

fig.3

If we summarize the analysis we can make the conclusion that the main sources of spurious frequencies and noise at the DDS output are the digital nature of the signal at the output and the quantizing and nonlinearities noise from the DAC.

IV. OUTPUT INTERFACE CONSIDERATION

High speed DDS IC's with integrated DAC's provide an output current witch can be pumped into any resistive load as long as voltage, developed at the DAC output does not exceed the maximum level. Normally the outputs are terminated to ground through a resistor as shown in fig.4.

For example the AD 985X family DDS will source current into a load, according to the equation: Iout= 39.93/Rset. The DDS/DAC output resistance specification is the combined impedance of the CMOS devises that comprise the switches and the current source circuitry. The DAC output resistance is very high and can be ignored in our calculations. Another important feature of the mentioned DDS is that the output current is unipolar and if the terminating resistor is connected to the ground the voltage will vary from zero to some positive value. This causes that the output sine wave will be DC offset from the load termination potential by one half of the full-scale voltage. This may be an important consideration when applying this signal to a dc coupled amplifier.

One solution to this problem is if we use the two outputs of the DAC witch are 180 degrees out of phase**.** These two signals can be combined in a center-tapped RF transformer to produce a symmetrical output waveform as shown in fig.4. When combining these two complementary currents in a transformer the dc offset is lost and the signal can be easily filtered and amplified. The low impedance way to ground through the transformer center tap is better than taking the reactive pathway through a LC filter that is terminated only at the filter output.

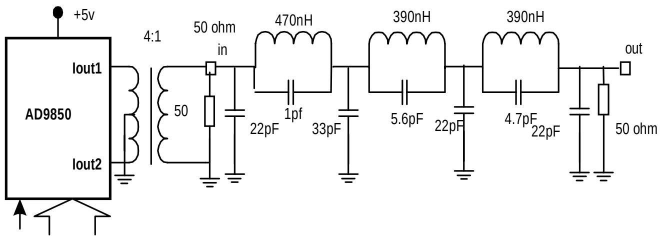

fig.4

Without a transformer, the next best method is to apply the DAC current output to a LC filter that is doubly-terminated, as shown in fig.5.

Regardless of what output termination scheme is chosen, experience has shown that optimum spurious and harmonic suppression are achieved when both Iout1 and Iout2 outputs are terminated equally. This is very important at higher output frequencies, where every dB of SFDR (spurious-free dynamic range) counts and this practice will give a cleaner output spectrum, lower spurs and higher SFDR. This practice is especially applicable to situations where only one of the outputs is utilized.

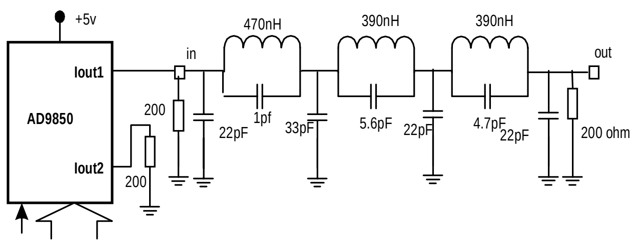

fig.5

V. FILTER DESIGN CONSIDERATIONS

For every particular application of the DDS these spurious frequencies have to be minimized to levels that are compatible with the spectrums of the other frequency sources. In almost every DDS this is accomplished from the low pass filter after the DAC. The frequency response of an ideal low pass filter would be 1 over the Nyquist band $(0 \le f \le Fs/2)$ and 0 elsewhere. Such a filter is not physically realizable and this results in the sacrifice of some portion of the available output bandwidth in order to match the no ideal response of the antialias filter.

The parameters of the output filters are very important for the overall performance of the DDS and the requirements they have to met define the purity of the synthesized signal.

The proper choice of the filter is connected with the reaching of some compromise between the contradictionary requirements for the great steepness of the transitional part of the frequency response of the filter and the flatness of the group delay time characteristic, which is needed for digital communication systems.

For a proper choice of a filter we need to define the different applications of the DDS and we can divide the applications in three types:

Direct digital synthesizers used individually or as a part of hybrid synthesizer where the whole possible frequency band has to be utilized.

DDS, used for a reference oscillators for hybrid DDS-PLL combination, where the only a part of the possible band of DDS is used and no need for wide band digital modulation.

DDS for a relatively narrow frequency band in mixer type hybrid synthesizers where wide band digital modulations have to be implemented.

Every one of these types has a need from particularly designed low pass filter. The most serious demands are for the first application where the aim for achieving a wider bandwidth leads to reaches to the Nyquist limit of fclk/2 in which case the first image fclk-fout is getting closer to fout and it becomes impossible to separate these two frequencies with the known filter approximations.

An important parameter of the filter is the group delay time or GDT, which is the first derivation of the phase and is a measure for the delay of different frequencies, when passing through the filter. GDT could be comparatively easily measured and used for criteria for the time domain characteristics of the filter.

There are lot types of filters known from the theory [3] and practice but the most popular are Butterworth, Chebyshev and Kauer (elliptic) approximations.

On the basis of these analysis and consideration a program in MATLAB [4] was designed where the input parameters are the $(f_{\mathbf{clk}}\text{-}f_{\mathbf{out}}/f_{\mathbf{out}})$-$\Omega$ ratio, the ripple in the passband and the minimal attenuation in the stopband. The definition of the limits for all these parameters depends exclusively on the specific application of the synthesizer but for the start a ripple of 1dB, Ω of 1,2 and attenuation of 60dB and 80dB were chosen. A filter for cut off frequency of 100 MHz designed with this program is connected to the output of the DAC as shown in fig.5.

When the requirements to the purity of the output spectrum of the signal of DDS are more stringent there is a possibility for further improvements with the use of tunable or bandpass filters.

VI. CONCLUSION

In this paper an analysis of the output spectrum of the DDS is done with respect to their application in the hybrid frequency synthesizers.

Three ways of optimization were analyzed and proposed in this paper:

First an optimal choice of a frequency band is done for minimal parasitic lines in the output spectrum.

Second the choice of optimal matching network for the output of the DAC is analyzed and experimented.

Third the choice of the output antialiased filter is discussed in respect of optimal filtering and matching of the DDS output.

Two programs in MATLAB are made for the investigation of the most appropriate output frequency range for reference clock applications. Solutions for best interface between the output of the DDS and the antialias filter are proposed.

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