Voltage Controlled Active Delay Element

Goran S. Jovanović[1] and Mile K. Stojčev[2]

***Abstract* – Variable delay elements are often used in different types of high-speed integrated circuits mainly intended for delay compensation, skew equalization, etc. These circuits are realized as hybrid, composed of digital and analog controlled parts. Digital part is used for coarse-grain while the analog for fine-grain delay variation. In this paper is propose a new analog delay element architecture and develop analytical equation for the delay of the circuit. The proposed circuit has linear transfer function, delay in term of control voltage in a full range of regulation.**

***Keyword* – Delay, CMOS circuit design, programmable delay element, current starved delay element.**

I. INTRODUCTION

Variable active delay elements have numerous applications in semiconductor VLSI IC's technology. Typically in meet them, as constituents, in Delay Locked Loops (DLL) [1-9], time-to-digital converters (TDC) [6], frequency multipliers [8], poly-phase clock generators [2], etc.

Active delay elements can broadly classified as digital or voltage controlled. Digitally controlled delay elements are usually realized as series of elements of variable length. The number of elements determines the amount of the delay. These kinds of delay elements are suitable for coarse-grain delay variation in a wide range of regulation. Analog voltage controlled delay elements are usually realized using shunt capacitor [1,3,5] or current starved delay elements [1-3,6-7]. Shunt capacitor delay element is capacitive loaded inverter, where a transistor, connected as a linear resistor, defines the charging and discharging current of the load capacitor. This type of delay element has the following disadvantages: a) the output capacitor occupies large silicon area; b) delay value and regulation range is small. Current starved delay elements are implemented with current supplied inverters. Varying the charging and discharging currents of the output parasitic capacitor we can control the propagation delay of these elements. Analog delay elements are suitable for fine-grain delay variation in limited range of regulation. Therefore, a combination of analog and digital delay elements, called hybrid, is used in many applications as an optimal solution [4,7].

Within the range of regulation, digitally controlled delay elements are linear, i.e. each delay element involves equal delay. Contrary to this, analog delay elements are non-linear, i.e. delay variation in terms of control voltage is non-linear function [1]. This means that for identical voltage increment constant delay difference, in a full range of voltage variation, is hardly to achieve.

Having this in mind, in this paper we focus our attention towards realization of linear hybrid delay line in a full range of voltage regulation. In our proposal, as digital controlled delay element we adopt the solution described in [7]. So, in the next all our efforts will be directed towards realization of linear voltage controlled analog delay element. The proposed solution is based on modification of the current starved delay elements. Improved linearity is achieved by involving symmetric load circuits. Simulation results which relate to 1.2 μm CMOS double-poly double-metal technology show that the proposed delay element has linear transfer function, delay in term of control voltage, in the full range of voltage regulation.

This paper is organized as follows: In Section II, we briefly explain the standard realization of the current starved delay element. In Section III, the proposed version of the modified current starved delay element is presented. Also, a detailed analysis of the modified circuit, which includes: results of simulation; testing linearity of the delay element and an analytical model of the propagation delay. Finally, Conclusion is presented in Section IV.

II. CURRENT STARVED DELAY ELEMENT – STANDARD REALIZATION

In order to explain our proposal, concerning modification of the current starved delay element, in the sequel, we will first briefly explain its standard realization [1], given in Fig. 1.

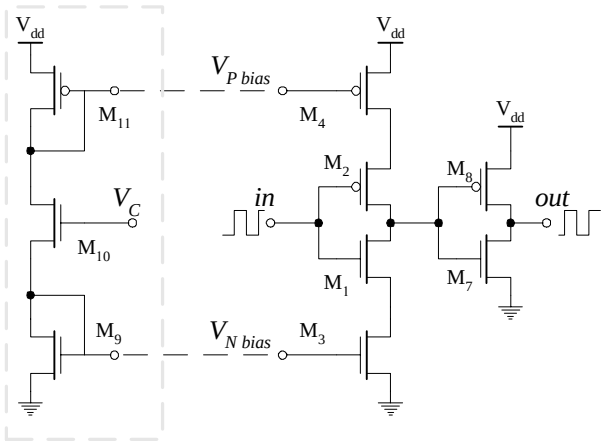

Fig. 1. Current starved delay element

[1] Goran S. Jovanović is with the Faculty of Electronic Engineering, Beogradska 14, 18000 Niš, Serbia and Montenegro, E–mail: joga@elfak.ni.ac.yu

[2] Mile K. Stojčev is with the Faculty of Electronic Engineering, Beogradska 14, 18000 Niš, Serbia and Montenegro, E–mail: stojcev@elfak.ni.ac.yu

As can be seeing from Fig. 1, the voltage controlled delay cell is implemented as a two–stage inverter. Transistors M_1 and M_2 are constituents of the first stage, while transistors M_7 and M_8 form the second stage. Transistors M_3 and M_4 act as current sink and source, respectively. Currents of transistors M_3 and M_4 represent discharging and charging currents of the output parasite capacitance, during rising and falling edge of the pulse, respectively. Voltages V_{Pbias} and V_{Nbias} regulate currents of M_3 and M_4, respectively. The bias circuit, composed of transistors M_9, M_{10} and M_{11}, provides correct polarization for transistor M_3 and M_4. The second inverter composed of transistors M_7 and M_8 involves some small constant delay. Also, second inverter improves rising and falling edge of the clock pulse at the output of delay element. It increases the slope of the rising and falling edges of the output pulse, too.

In Fig. 2, the propagation delay of the starved delay element (from Fig. 1.) in term of control voltage V_c is given. This curve is obtained using Spice simulation for transistor models of 1.2 μm CMOS technology, at supply voltage V_{dd}=5V. As can be seen from Fig. 2, the range of delay variation is large but nonlinear, and is analytically defined as [7]:

$$t_p = \frac{C_L \cdot V_{dd}}{K_p (V_C - V_t)^2} \qquad (1)$$

where: C_L - output load capacitance; V_{dd} – supply voltage; K_p – technology parameter $\mu C_{ox}(W/L)$; V_t - threshold voltage; and V_C - control voltage.

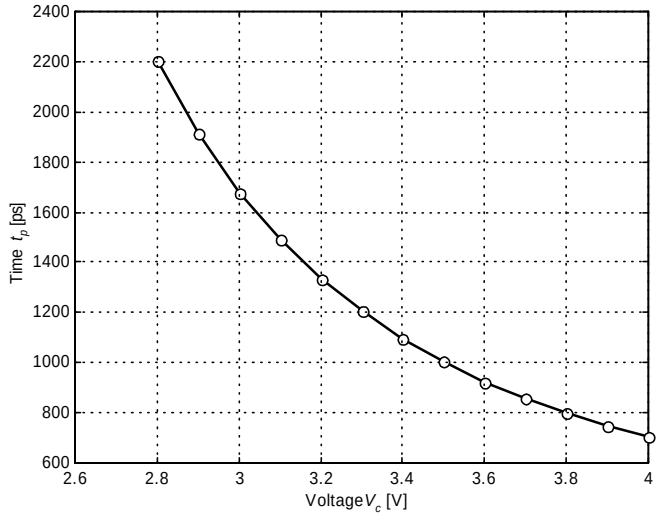

Fig. 2. Propagation delay t_p in term of control voltage V_c

III. CURRENT STARVED DELAY ELEMENT WITH SYMMETRIC LOAD

The modified version of the current starved delay element is pictured in Fig. 3. In parallel with transistors M_3 and M_4, symmetric load circuits, transistors M_5 and M_6, are added. By involving symmetric load circuits we provide a condition that transistors M_3, M_4, M_5 and M_6 operate in saturation mode. Also, the charging and discharging currents of parasitic capacitor C_L, are increased. This modification results to shorter propagation delay in respect to standard current starved delay element (Fig. 1.).

In order to derive an analytical model of the signal propagation delay trough the delay element we will use schematic given in Fig. 4. Here we assume that transistors M_1 and M_2 (Fig. 3.) are ideal switches, M_3 and M_5 act as current sinks, and M_4 and M_6 as current sources.

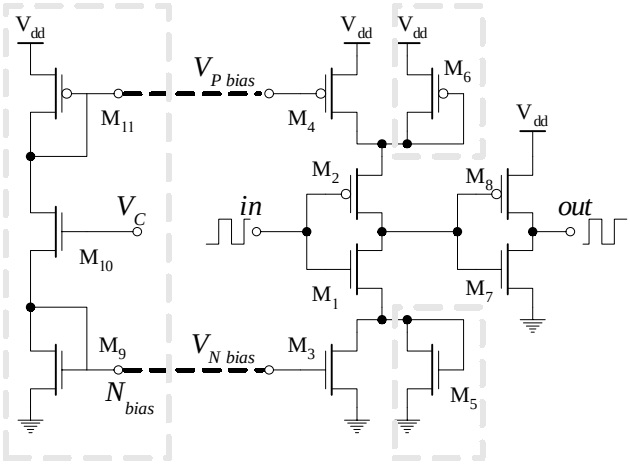

Fig. 3. Current starved delay element with symmetric load

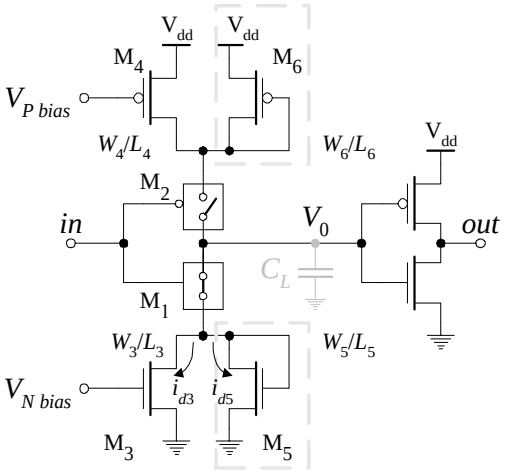

Fig. 4. Simplified scheme of the current starved delay element with symmetric load

If at the input *in* rising pulse edge is present, transistor M_1 act as closed switch. The parasitic capacitor C_L, at the output of first inverter stage, discharges from V_{dd} to 0V. The capacitor discharging current consists of i_{d3} and i_{d5}, and the following is valid:

$$-C_L \frac{dV_0}{dt} = i_{d3} + i_{d5} \qquad (2)$$

where i_{d3} i i_{d5} a currents of transistors M_3 and M_5 respectively. Both transistors M_3 and M_5 operate in saturation mode, so that the following is valid:

$$-C_L\frac{dV_0}{dt}=\frac{k_n}{2}\frac{W_3}{L_3}(V_g-V_t)^2+\frac{k_n}{2}\frac{W_5}{L_5}(V_0-V_t)^2 \\ =k_1(V_g-V_t)^2+k_2(V_0-V_t)^2 \quad (3)$$

Eq. (3) can be simplified by involving following substitutions: $k_1=(k_n/2)(W_3/L_3)$ and $k_2=(k_n/2)(W_5/L_5)$. By solving the differential eq. (3) on obtain

$$\int\frac{d(V_0-V_t)}{\frac{k_1}{k_2}(V_g-V_t)^2+(V_0-V_t)^2}=-\frac{1}{\tau}\int dt \quad (4)$$

where $\tau=C_L/k_2$. For initial values t=0 and $V_0=V_{dd}$, Eq. (4) has the following solution:

$$t=\frac{\tau}{\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}\left[\arctan\frac{V_{dd}-V_t}{\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}-\arctan\frac{V_0-V_t}{\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}\right] \quad (5)$$

Using the well know trigonometric transformation

$$\arctan u+\arctan v=\arctan\frac{u+v}{1-uv} \quad (6)$$

we obtain following form

$$t=\frac{\tau}{\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}\arctan\frac{(V_{dd}-V_0)\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}{\frac{k_1}{k_2}(V_g-V_t)^2+(V_0-V_t)(V_{dd}-V_t)} \quad (7)$$

The propagation delay of the first inverter t_{p1} is derived when the logical threshold voltage is $V_0=V_{dd}/2$, and is equal to:

$$t_{p1}=\frac{\tau}{\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}\cdot\arctan\frac{\frac{V_{dd}}{2}\cdot\sqrt{\frac{k_1}{k_2}}(V_g-V_t)}{\frac{k_1}{k_2}(V_g-V_t)^2+\left(\frac{V_{dd}}{2}-V_t\right)\cdot(V_{dd}-V_t)} \quad (8)$$

where: k_1 and k_2 are constants determined by technology parameters and transistor geometry; V_g - corresponds to gate to source voltage of transistors M_3 and M_4; V_t – threshold voltage; V_{dd} – voltage supply.

The total delay time is obtained as a sum of the propagation delays, that correspond to both inverters, i.e. $t_p=t_{p1}+t_{p2}$. Propagation delay time of the first inverter t_{p1} depend of gate to source transistors voltage V_g, and is given by Eq. (8). Time delay of the second inverter is independent of V_g and is defined by [10]:

$$t_{p2}=\frac{C_L}{K_p(V_{dd}-V_t)}\left\{\ln\left[4\left(\frac{V_{dd}-V_t}{V_{dd}}\right)-1\right]+\frac{1}{2}\right\} \quad (9)$$

where: C_L - output load capacitance; V_{dd} – supply voltage; K_p – technology parameter $\mu C_{ox}(W/L)$ and V_t - threshold voltage.

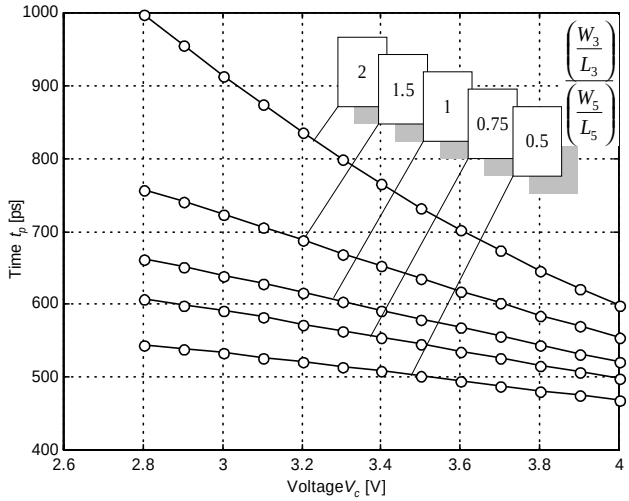

Fig. 5. Time delay in term of control voltage for current starved delay element with symmetric load

In Fig. 5, simulation results for the proposed circuit are given. For Spice simulation transistor models for 1.2 μm CMOS technology and supply voltage V_{dd}=5V are used. Sketched curves relate to different ratios $(W_3/L_3)/(W_5/L_5)$ and $(W_4/L_4)/(W_6/L_6)$. Where W_3, W_4, W_5 and W_6, and L_3, L_4, L_5 and L_6 correspond to channel width and length of transistors M_3, M_4, M_5 and M_6 respectively. As can be seen from Fig. 4, the range of delay regulation, in respect to standard current starved delay element (Fig. 2.) is decreased, but the linearity is drastically improved. According to the Fig. 4, one can conclude that for greater ratio $(W_3/L_3)/(W_5/L_5)$ and $(W_4/L_4)/(W_6/L_6)$ we obtain greater range of delay regulation. This means that if dimensions of transistors M_3 (M_4) are greater then that of M_5 (M_6) the range of delay regulation increases, in contrary it decreases.

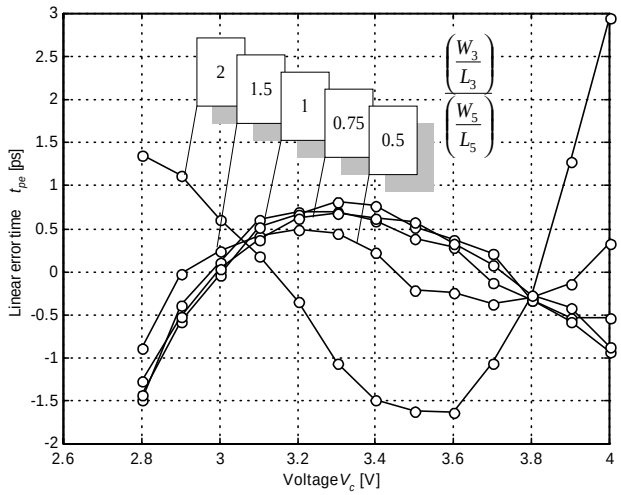

Fig. 6. Delay linearity errors in term of control voltage for different ratios $(W_3/L_3)/(W_5/L_5)$ and $(W_4/L_4)/(W_6/L_6)$ as parameters

In Fig. 6, linearity errors of the modified circuit (Fig. 3.) for different ratios of $(W_3/L_3)/(W_5/L_5)$ and $(W_4/L_4)/(W_6/L_6)$ are given. In general, in worst case errors are small (<1%) and depend of the ratio $(W_3/L_3)/(W_5/L_5)$ and $(W_4/L_4)/(W_6/L_6)$.

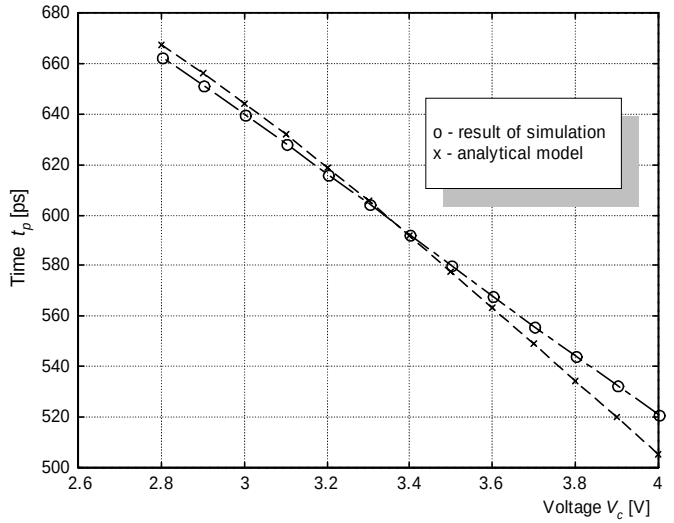

Fig. 7. Results of simulation and analytical model for time delay in term of control voltage

In Fig. 7, result of simulation and derived analytical model, Eq. (8), for fixed ratios $(W_3/L_3)/(W_5/L_5)=1$ and $(W_4/L_4)/(W_6/L_6)=1$, i.e. $k_1/k_2=1$, are given. As can be seen from Fig. 7, good agreement (<5%) between the analytical model and result of simulation exists.

IV. CONCLUSION

In this paper we propose new architecture for an analog voltage controlled delay element. This circuit represents a modified version of the current starved delay element with symmetric load. Analytical model of propagation delay is derived. The circuit is implemented in CMOS 1.2 μm double-poly double-metal technology. The obtained simulation results show that the circuit has linear transfer function, delay in term of control voltage in a full range of regulation. Delay linearity error is less then 1%. Agreement between analytical model and simulation results is good, i.e. the error is less then 5%.

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