Comparison of Energy Factors of Transistor Invertors for Induction Heating Using PSpice

G. Kunov[1], M. Popov[2], E. Gadjeva[3]

***Abstract*: In the present paper *PSpice* computer models are developed for the basic transistor inverter types – series, series-parallel and current-fed parallel inverters. Based on the same conditions - voltage across and current through the transistors, output power comaprison has been made within the different inverter topologies. The computer simulation allows a detailed investigation of the commutation processes in the inverter circuits taking into account the real characteristics of the active components. The commutation processes are simulated, and the static and dynamic dissipated power on the transistors is calculated.**

***Keywords:* Power Electronics, Transistor Invertors, Induction Heating.**

I. INTRODUCTION

The transistor inverters are widely used in the high-frequency induction heating technologies for power greater than 10 kW and frequency above 20 kHz. From the great variety of transistor inverters being used in the field of high frequency induction heating, the bridge topologies are the most widely used [1].

The point of study in the current article is: bridge series resonant inverter, series-parallel resonant inverter and bridge parallel current-fed inverter. These topologies (Fig.1a,b,c) have been *PSpice* analyzed.

The commutation processes are specific for each inverter circuit type, and their adequate modeling is of significant importance for the transistor driver circuit composition. These processes of the active and passive components are simulated, and the static and dynamic dissipated power on the transistors is calculated.

Examples are given, illustrating the validity, the specific features and the efficiency of the developed *PSpice* models. The simulation is performed using the *OrCAD PSpice* simulator.

The major processes in the series resonant inverters are widely analyzed and described in the engineering literature like [1], [2] ect.

The waveforms of the voltage (V_{AB}) across and the current (I_{Rs}) through the diagonal of the bridge are *PSpice* simulated and shown in Fig.2.

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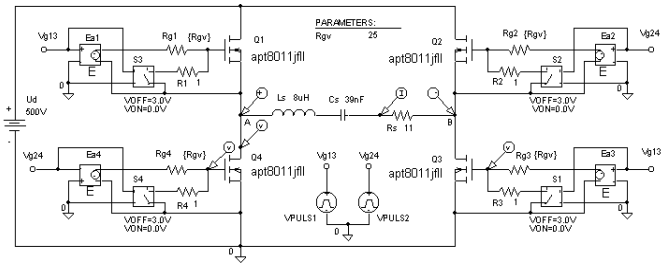
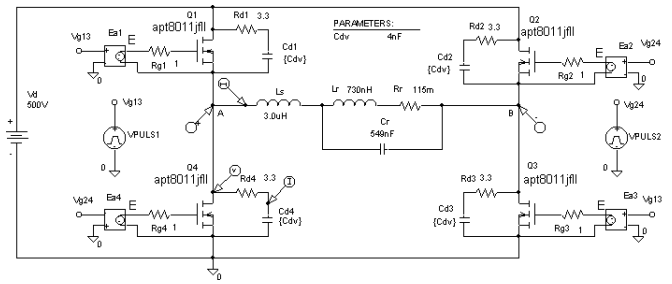


a)



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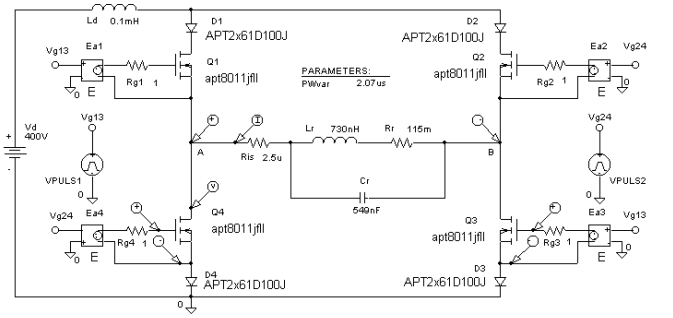

c)

Fig. 1. The basic investigated inverter circuits

The shape of the voltage waveform is rectangular and the magnitude equals the value of the supply voltage (V_d). The shape of the current is a sine wave. When the frequency of the gate drive pulses (VPULSE1,2) equals the resonant frequency of the series oscillation loop ($f_{sw} = f_o$), then the transistors are commutated at zero current ZCS.

The operation of the series-parallel resonant inverter at active load is analyzed in [2] while the simulation at complex load is analyzed in [4] and [5]. A characteristic feature is the rectangular shape of the inverter voltage waveform (V_{AB}), which magnitude is equal to the value of the supply DC voltage. The diagonal current waveform (I_{LS}) resembles trapezoid shape (Fig.3). The inductance L_s makes sure the inverter operates in inductive mode while the load is fully compensated. When having enough dead time between the gate-drive pulses, this mode ensures that the switches are commutated at zero voltage (ZVS).

Unlike the SCR [6], the transistor inverters are recommended to be operated in inductive mode of the load oscillator loop ($f_{sw} < f_o$). This mode eliminates the current in the body diodes.

The shape of the voltage across the diagonal (V_{AB}) is a sine-wave. The current (I_{Ris}) is rectangular (Fig.4).

For comparison purposes the same supply voltage, load, operation frequency (250kHz), maximal voltage across and maximal current through the switches are selected. In this way the similar working conditions give the possibility to compare the power characteristics of the different topologies i.e. the active power in the load and the power loss in the switches.

II. EVALUATION CRITERIA BASED ON THE MAXIMUM POWER DISSIPATED IN THE LOAD

In this evaluation, the approach used in [3] is applied. The output power is defined as a multiplication of the inverter voltage, current through the diagonal and $\cos(\beta)$, where β is the phase angle between these two parameters.

In the case of *series resonant inverter* the amplitude of the rectangular inverter voltage in the diagonal of the bridge is equal to the max. voltage across the switches i.e. $V_{AB} = V_{Dm}$. The RMS value of the inverter voltage is defined by the equation:

$$V_{AB(RMS)} = \frac{4V_{Dm}}{\pi\sqrt{2}}.$$

The RMS value of the current across the diagonal is defined by the equation:

$$I_{AB(RMS)} = \frac{I_{Dm}}{\pi\sqrt{2}}.$$

Because these two parameters are phased, the power equation will be as follows:

$$P_S = \frac{4V_{Dm}}{\pi\sqrt{2}}\frac{I_{Dm}}{\sqrt{2}} = \frac{2V_{Dm}I_{Dm}}{\pi} = 0.636V_{Dm}I_{Dm} \qquad (1)$$

In the case of *series parallel resonant inverter* the RMS voltage is the same as in the previous case. The RMS value of the trapezoid current is defined by the equation:

$$I_{AB(RMS)} = \frac{4I_{Dm}\sin(\beta)}{\pi\beta\sqrt{2}},$$

where β is the rise time from zero to max and vise versa of the current in Radians [RAD]. In fully compensated mode of operation this angle matches the phase angle between the inverter current and voltage.

Consequently the equation of the power will be stated as follows:

$$P_{SP} = \frac{4V_{Dm}}{\pi\sqrt{2}}\frac{4I_{Dm}}{\beta\pi\sqrt{2}}\sin(\beta)\cos(\beta) = 0.729V_{Dm}I_{Dm} \qquad (2)$$

The following parameters can be defined in Fig. 3: t_β=250ns which is equal to β=22.5° or 0.393 rad [5] for switching frequency of 250kHz.

In the case of *parallel current-fed inverter* the equations of inverter voltage and current are the same as in the series resonant inverter but their positions are swapped.

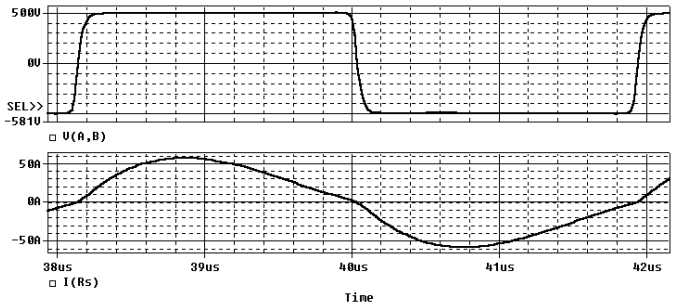

Fig. 2. The waveforms of the voltage V_{AB} and the current I_{Rs} of the series resonant inverter

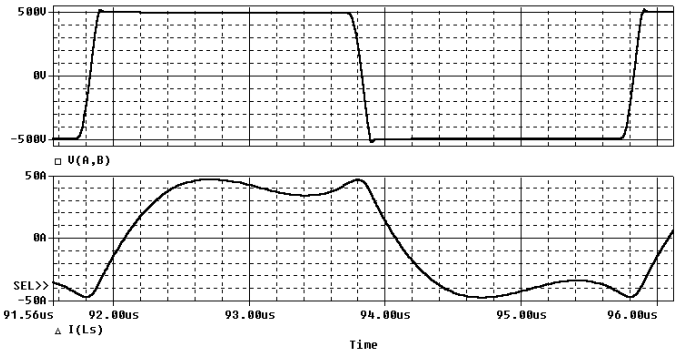

Fig. 3. The waveforms of the voltage V_{AB} and the current I_{Ls} of the series parallel resonant inverter

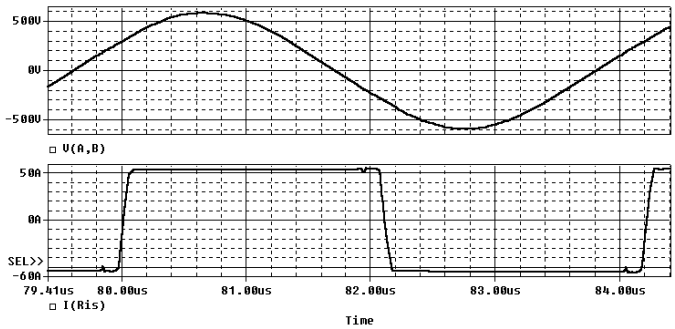

Fig. 4. The waveforms of the voltage V_{AB} and the current I_{Ris} of the parallel current-fed inverter

When β=22.5° then:

$$P_P = \frac{V_{Dm}}{\sqrt{2}}\frac{4I_{Dm}}{\pi\sqrt{2}}\cos(\beta) = 0.588V_{Dm}I_{Dm} \qquad (3)$$

From (1) , (2) and (3) becomes evident that at identical initial conditions, the series parallel inverter will deliver the biggest power, while the parallel will deliver the smallest power in the load.

III. PSPICE SIMULATION AND POWER LOSS EVALUATION DURING THE TRANSITION OF THE SWITCHES

Duding this simulation and evaluation, *PSpice* models of the following transistors and diodes are used:
Switch: APT8011JFLL
Diode: APT2x61D100J
Manufacturer: Advanced Power Technology [9].

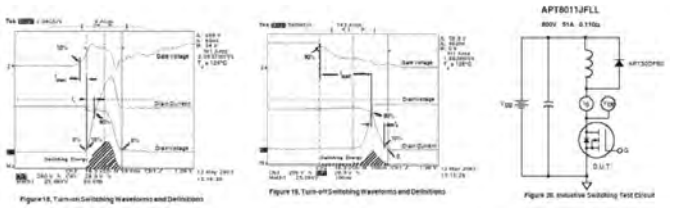

Fig. 5. The test setup for the power loss during transition given by Advanced Power Technology manufacturer

All manufacturers use the test setup shown in Fig.5 to measure the power loss during transition.

It is a severe mode for the transistor, when hard switching is applied. In this case additional power loss is encountered during the saturation of the switch, caused by the free willing current running through the body diode.

The purpose of the following *PSpice* simulations is the measurement of the power loss into the real applications.

In the case of *series resonant inverter* specific commutation features in each leg of the inverter bridge characterize ZCS in bridge resonant inverter. The input and reverse capacitance of the conducting transistor are zero charged at the end of each current sine wave. At that time the capacitance of the opposite transistor in the same leg is charged to the value of the supply voltage. When this transistor is turned on the current running through, is initially discharging its own capacitance while charging the capacitance of the other transistor in the same leg. The capacitance current running at the end and the beginning of each current sine wave, determine the loss during transition.

This simulation was done in parametric mode analysis. The value of the gate resistor **{Rgv}** is the variable parameter. This resistor is limiting the value of the charging current in the input capacitance. It results in decreasing du/dt and di/dt. This approach is used in [7] and [8] as well. The results from this simulation are shown in Fig. 6.

Increasing the value of *Rg* will result in smoother transition through active mode. The benefit is the decrease of the maximum value of power loss and du/dt across the switch.

As seen in Fig. 7 the total power (sum of commutation and static power) decreases when *Rg* increases. In this example this value is equal to 120W when $Rg = 20\,\Omega$.

In the case of *series parallel resonant inverter* the inductive character of the load in the diagonal of series-parallel inverter is a typical case of ZVS. Installing an additional capacitor drain to source (C_{dv}) will split a part of the current out of the switch during turn off. The bigger the ratio C_{dv}/C_{ds} is, the bigger part of the current is split out. This results in decreasing the maximum power dissipated across the switch (Fig. 8).

The transistor power loss in this inverter is mostly concentrated in the turn off cycle. In this example Cd= 6nF which results in equal power loss as within series inverter (Fig.9).

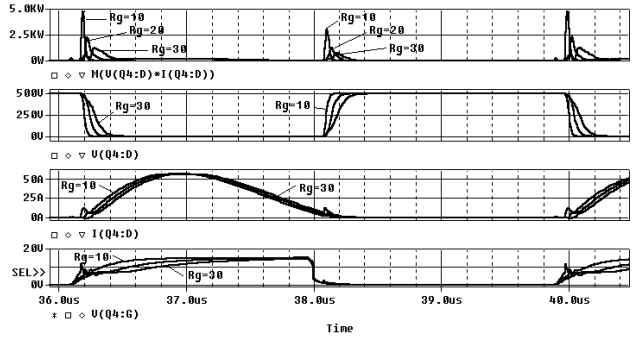

Fig. 6. The results of *PSpice* simulation of the commutation processes for series resonant inverter

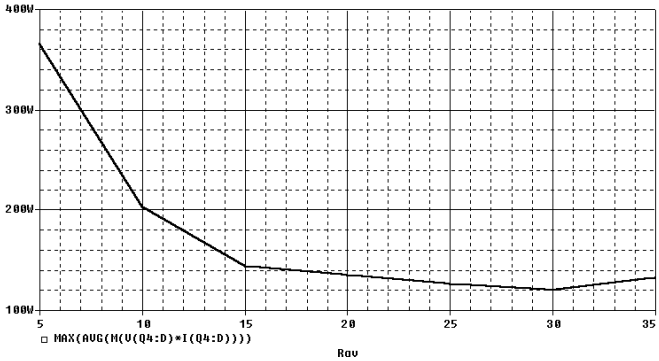

Fig.7. The dependence of switching losses on R_{gv} for series resonant inverter

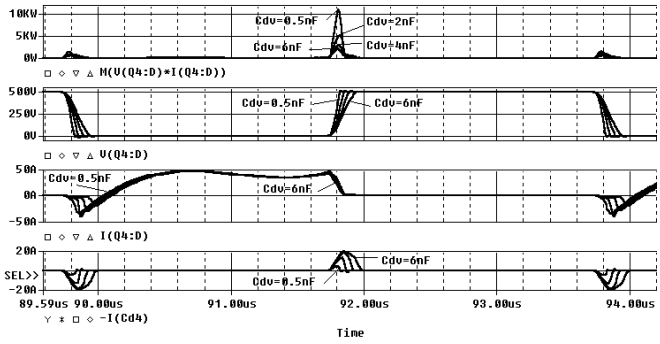

Fig. 8. The results of *PSpice* simulation of the commutation processes for series parallel resonant inverter

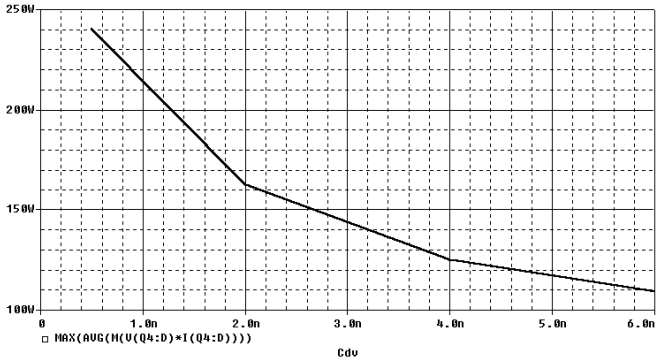

Fig. 9. The dependence of switching losses on C_{dv} for series parallel resonant inverter

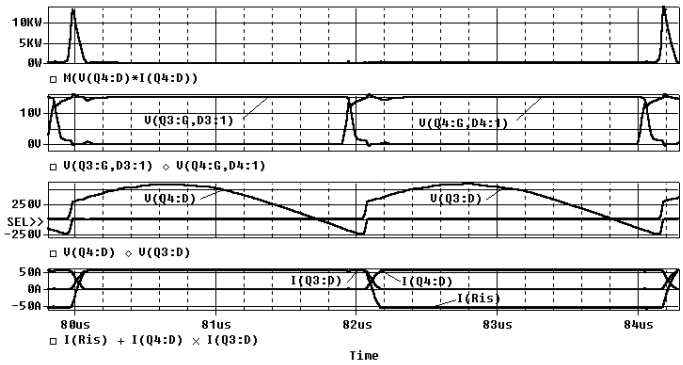

Fig. 10. The results of *PSpice* simulation of the commutation processes for parallel current-fed inverter

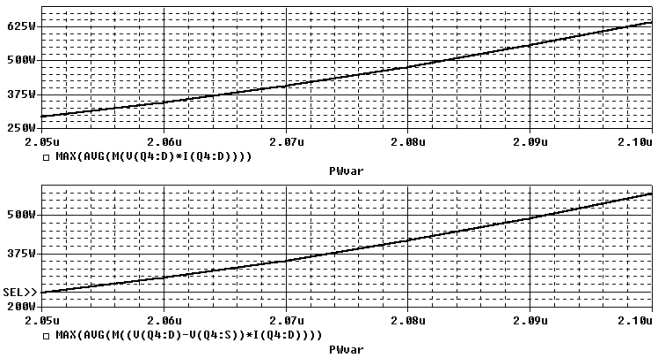

Fig. 11. The dependence of switching losses on f_{sw} for parallel current-fed inverter

Because the *parallel current-fed inverter* is powered by a current source, no time interval when all switches are turned off is acceptable. The inductive mode of the oscillating load loop ($f_{sw} < f_o$) ensures smooth current transition in the inverter legs (Fig.10).

As seen from the simulation results, commutation loss is observed just during turn on of the switch. The amplitude of this loss is relatively high. Increasing the inductive mode (decreasing the switching frequency will result in power loss increase (Fig. 11).

This topology encounters the most power loss compared to the other two topologies.

IV. Conclusions

Resulting the analysis of the research, the following statements can be concluded:

1. The series-parallel inverter delivers the highest output power to the load.

2. Concerning the power loss in the switches, the series and the serial-parallel inverter are equal while the parallel inverter encounters the highest power loss.

3. By optimal selection of the gate resistor in the serial inverter and by increasing the value of the additional drain to source capacitor, the power loss can be optimized.

The less possible inductive mode of the oscillating load loop must be applied with the parallel inverter.

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