Modern PWM drives voltage sags sensitivity

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Abstract – **In this paper it is presented investigation in modern PWM drives voltage sags sensitivity. The simulation results, presented below, were collected from the variable speed drives with different control algorithms: simple V/Hz control, indirect rotor flux oriented control and direct torque control. The achieved results refer to various types of symmetrical and asymmetrical voltage sags and show the significant influence of PWM inverter control algorithm.**

Keywords – **voltage sag, adjustable speed drive, power quality, control**

I. INTRODUCTION

According to the appropriate IEC and IEEE standards (IEC 61000-2-8 and IEEE 1159-1995) voltage sags are defined as a temporary short duration voltage magnitude reduction in any or all of the phase voltages (in single or poly-phase electrical network). Beside voltage thresholds, voltage sags are expressed by time duration (0.5 cycles – 60 seconds) and type of voltage sag variation: the three-phase balanced and the different unbalanced. Basically, voltage sags are classified in two ways: in the first of them it is taken into consideration the number of sagged phases and the presence of asymmetries; and the second one divides sags into several ranges regarding to sag duration and/or magnitude ([1], [2]). The newest proposals for voltage sags classification and presentation taking into consideration phase shifts and points on wave at the sag initiation and at the voltage recovery, sag shape, etc.

The fact that adjustable speed drives (ASD) with induction motors are highly sensitive to voltage sags can cause long re-start delays and production losses. An extra increase of expenses (for example in continuous processes as paper industry, glass production, etc.) caused by ASD voltage sags sensitivity which also leads to a numerous experimental and simulation studies. The main aim of the studies mentioned above is to determine the sensitivity factors, and to propose prevention of the ASD's from tripping as a result of voltage sags.

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This paper presents the effects of the influence of the different control algorithms on ASD voltage sag sensitivity. Using basic library blocks from Matlab/Simulink and SimPowerSystem toolbox, power converter and supply network model are built and also presented three different control algorithms: open loop V/Hz, speed closed loop indirect field oriented control (IFOC) and speed closed loop direct torque control (DTC). Various types of symmetrical and asymmetrical voltage sags are used in simulations with different loading and operating drive conditions. It was also presented simple methods on each at a time, by which speed drops were reduced during voltage sag.

II. ASD AND VOLTAGE SAGS

There are three reasons for tripping ASD's because of voltage sag. The first one is that the control electronics power supply of the drive also sensitive to voltage sag. If the power supply cannot obtain adequate voltage for the control electronics, the drive has to be shut down as a safety measure against losing control of the drive. It is necessary the drive to be equipped with an uninterruptible power supply (UPS) for the control electronics. In industrial plants it is the most common approach by which control electronics operation is obtained during voltage sag or interruption.

The second reason is that DC voltage drop under predefined minimum level or output motor currents go through the over-current limit. DC voltage drop under minimum level can lead to the appearance of the high inrush input current when the power-up again.

The third reason is that some processes with ASD (for example multi-motor and speed synchronized drives) cannot tolerate the loss of accurate speed or torque control, even for a few seconds due to damage the final product or halt of the process.

Figure 1 show a typical PWM ASD equipment topology, which consists of a three-phase diode rectifier, DC-link and an inverter. There are two basic types of rectifiers: the uncontrolled (diode) and the controlled (thyristor or IGBT) rectifiers. In this paper we only considered a diode rectifier.

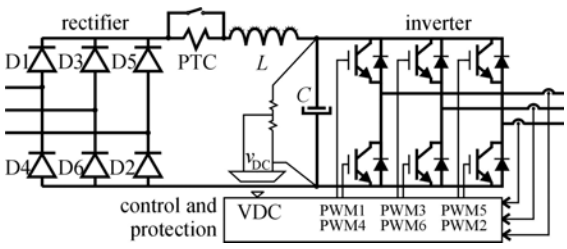

Fig. 1. Typical PWM frequency converter

The DC-link consists of LC filter for smoothing the pulsating DC voltage and the charging circuit suppresses high inrush current during converter power-up. ASD's typically have between 75 and 360 mF of capacitance per kW of drive rating and the DC-link inductor (typically, 2%-5%). The inverter controls the frequency of the motor voltage according to signals (pulses) from control circuit. The control and protection circuit can transmit and receive signals to/from rectifier, the intermediate circuit and the inverter.

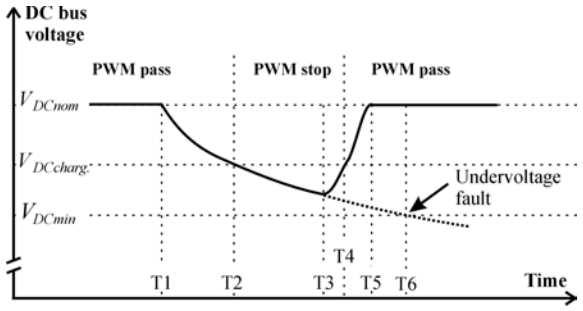

Fig. 2. DC link voltage during voltage sag

In the Figure 2 is shown important occurrences to explain ASD sensitivity to voltage sag. At T1 period the voltage sag is appeared and, due to reverse bias of input diodes, DC bus voltage begins to drop rapidly. When $V_{DCcharg}$ value is reached (level where the drive goes into pre-charge) output to the motor is stopped. Between T2 and T3 the rate of decay on the bus voltage is much slower because the drive is not producing output power to the motor.

If the line voltage is restored at T3 period, the DC bus voltage will begin to rise. Between T3 and T4 the input line current is limited by the pre-charge circuit. This prevents high inrush currents and DC bus over-voltage. At T4 the PWM inverter control starts and output to the motor resumes. If the line voltage not restored at T3, a line loss fault or under-voltage fault could occur at T6 (DC bus voltage falls below a minimum level V_{DCmin}). This minimum DC voltage level may be the lowest safe point when the internal control power supply can be in operation.

The voltage sag type (single-phase, two-phase or three-phase) and duration of the sag influence drive sensitivity. Loading and operating conditions of both the drive and controlled motor also have significant influence on drive behaviour during the sag. Thus, different load types, variations in loading torque and operation with reduced motor speeds should be also regarded as the factors of influence in the assessment of the PWM drive sensitivity.

Adjustable speed drive complexity, numerous of influential parameters and request for special equipment usage (voltage sag generator, programmable load and measurement equipment) make difficult the experimental investigation of ASD voltage sag sensitivity. According to Ref. [6] appropriate simulation model must have the following important parameters: a) the DC link components; b) the power consumption of the load (loading torque including induction motor *qd*-model); c) under-voltage / over-current protection settings including current/voltage sampling effects and RMS calculation; and d) control algorithm. The importance of the influence of the last mentioned parameter is stressed in this paper.

III. MODELLING AND SIMULATION

Complete ASD model with the power supply voltage sag generator is built in Matab/Simulink software. In control circuit we modelled three different control algorithms: open loop V/Hz with stator resistance voltage drop compensation ([3]), speed closed loop indirect rotor field oriented control (IFOC) ([4]) and speed closed loop direct torque control (DTC) ([5]). All parameters of the power unit and control circuit of the frequency converter are shown in Table 1.

TABLE 1. POWER UNIT AND CONTROL CIRCUIT PARAMETERS OF THE FREQUENCY CONVERTER ([5]).

Power unit	Input	3~, 400V, diode bridge rectifier
	Output	3~, IGBT inverter, I_{outnom}=9.5A
	DC link	C=2x640μF in series, (dis)charging time 17ms, L=1.5mH
Protection settings	Under-voltage protection	$V_{DCcharg.}$=320V (57% of V_{DCnom}=560V); sampling period T_s=250μs
	Fast over-current protection	I_{outmax}=20.4A rms, (215% of I_{outnom}=9.5A), $f_{bandwidth}$=5kHz
Control methods	V/Hz control	switching frequency f_{SW}=7.5kHz, with stator resistance voltage drop compensation
	IFOC	speed closed loop, f_{SW}=7.5kHz, torque limit T_{max}=160% T_{nom}.
	DTC	speed closed loop, f_{SW}=7.5kHz, torque limit T_{max}=160% T_{nom}.

In this paper we used induction motor with the following parameters: 3x230/400V, D/Y, 50Hz, nominal speed n_n=1440rpm; rated power: P_n=4kW; stator and rotor leakage inductance: L_{ls}=L_{lr}=0.013mH; mutual inductance L_{lm}=0.130mH; stator and rotor resistance: R_s=1.13Ω, R_r=0.9Ω; inertia J_m=0.015.

Firstly we tested ASD sensitivity against three-phase symmetrical voltage sags with different load torque values and with nominal reference speed. Achieving results are presented in Fig. 3. All drives have identical settings of protection control circuit and in a speed control schemes PI speed controller parameters are adjusted equally.

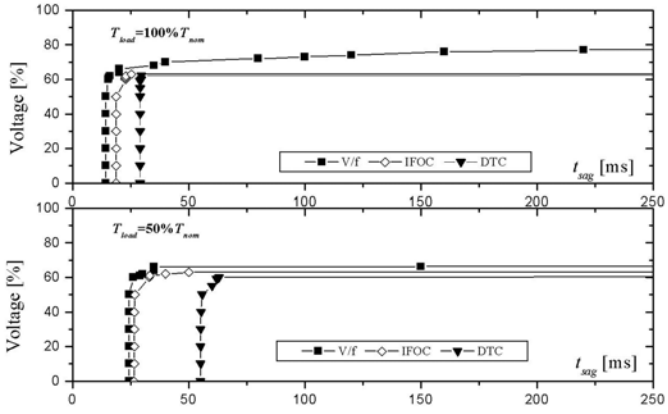

Fig. 3. Sensitivity of ASD drives to symmetrical three-phase sags with different load torque values: T_{load}=100%T_{nom} (top); T_{load}=50%T_{nom} (bottom)

The vertical parts of the drive voltage-tolerance curves are determined under-voltage protection response. Small difference between drives is the consequence of different DC voltage ripple and motor electromagnetic torque (stator currents) during sag. If the supply voltage recovers before the DC bus voltage reaches the under-voltage protection level, a high charging current is drawn from the supply network and may blow the fuses. If this possible, high inrush current can flow to induction motor and activate over-current protection. In V/Hz drive, horizontal part of the voltage-tolerance curve represents this effect. Due to the torque limit (torque limit is set on 160% of nominal torque) drives with IFOC and DTC are not able to cause fast over-current reaction.

Figure 4 compares voltage-tolerance curves obtained in simulations for three-phase voltage sags with different motor speeds. Decreasing the adjusted motor speed also results in lower drive sensitivity.

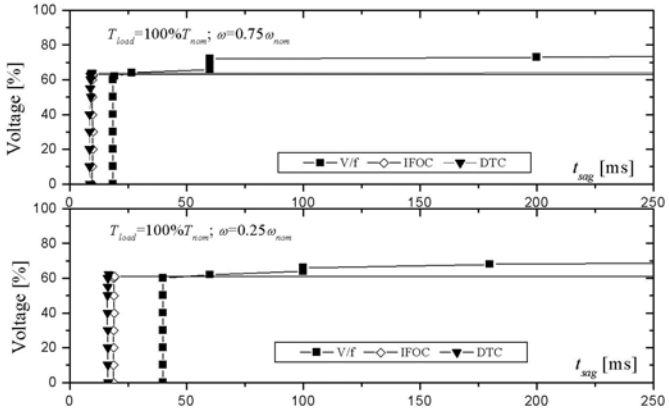

Fig. 4. Influence of different motor speeds on sensitivity of PWM drive to symmetrical three-phase voltage sags.

In Fig. 5 are shown voltage-tolerance curves for two-phase voltage sags with rated voltage in un-sagged phase and with different motor speeds (constant torque load type and rated loading torque value). The similar behaviour is identified in this case - decreasing of the adjusted motor speed results in lower drive sensitivity. Two-phase voltage sag characteristic is DC bus voltage ripple and a significant torque ripple increase (for example, in DTC drive thereabout 300% of rated regime values).

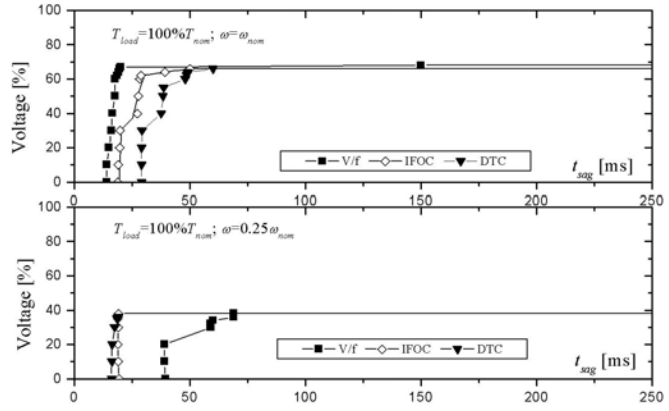

Fig. 5. Sensitivity of VSD drive to two-phase sags.

For single-phase sags with rated voltage in un-sagged phases no-trip occurs in all types of drives.

IV. MOTOR SPEED DROP

Some processes driven by the motors, like multi-motor drive application (speed synchronization or torque load sharing regulation) will not be able to tolerate the drop in speed or the torque variations due to the sag.

In ASD with IFOC the problem of adequate adjusting flux-producing stator current component (i_{ds}) is appeared. Before voltage sag, this component is equal to nominal value i_{dsnom}, as in the period after voltage dropping. During the voltage sag flux-producing current component can be adjusted according to: 1) the rated value; 2) the value which is appropriate to DC bus voltage value during the sag; 3) the dynamic *d*- and *q-axis* current sharing strategy which obtain higher transient torque and minimum speed deviation.

A sudden step supply voltage decrease takes place next, at time instant zero, leading to the operation of the inverter at the maximum allowed stator current value i_{smax}:

$$i_{s\max} = \sqrt{i_{ds}^{*2} + i_{qs}^{*2}} \ . \qquad (1)$$

The available current is to be distributed into *d*- and *q-axis* current. Here asterisk denotes commanded (reference) values and indices *d* and *q* remark *d-q axis* components of the stator currents. The algorithm that is developed here is characterized with the following rules:

$$i_{ds}^{*} = 0 \qquad i_{qs}^{*} = i_{s\max} \qquad \text{for } 0 < t < t_1 \qquad (2)$$

$$i_{ds}^{*} = k \cdot i_{dsnom} \qquad i_{qs}^{*} = \sqrt{i_{s\max}^{2} - i_{ds}^{*2}} \ \text{ for } t_1 < t < t_2 \,, \qquad (3)$$

where: t_1 is the time when the *d-axis* motor current component drops to the decreased value which is matched with the sagged DC bus voltage, t_2 is the time of the power-up and $k = V_{DC} / V_{DCnom}$. V_{DC} and V_{DCnom} denote actual and nominal DC bus voltages. After sag ending, flux-producing current component resets to the nominal value. Developed simulation model takes into account sampling times and frequency bandwidths for currents and voltages measurement loops.

In Fig. 6 is presented the comparison of the simulation results, for three methods mentioned above, in case of symmetrical three-phase voltage sag.

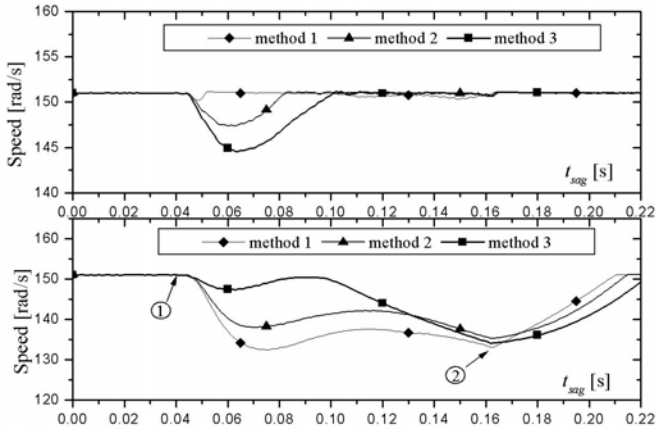

Fig. 6. Motor speed drop during voltage sag in drive with IFOC (① - point of sag start, ② - point of sag end): U_{sag}=80%U_n (top); U_{sag}=70%U_n (bottom)

As it can be seen in Fig. 6, the proposed method of the dynamic current sharing of the inverter maximum current, leads to the minimum speed drop. The adjustable speed drive with IFOC where the third method is implemented reacts faster than the first two ones because of forcing torque-producing current component. It should be noted that in practice there is a problem of the proposed algorithm in detection of the voltage sag magnitude value. Beside the simulated rectangular voltage sag, the experimental researches present that voltage sags which are neither rectangular in most cases nor voltage magnitude is constant during the whole period. This can make problems in practical implementation, which will be target in future research.

In the case of ASD with DTC is modelled very simple algorithm where is the commanded value of the stator flux chosen according to the following equation:

$$\psi_s^* = k \cdot \psi_{snom}^* , \tag{4}$$

Where: ψ_s^* and ψ_{snom}^* actual and nominal stator flux reference value, respectively. In the simulation ψ_s^* is reached as output from look-up table with V_{DC} as an input. More detailed explanation of the simulation model of ASD with DTC can be found in [5] or in request of the first author. In Fig. 7 are shown simulation results in speed drop for DTC classical model (without stator flux correction) and for model in which Eq. (4) is implemented.

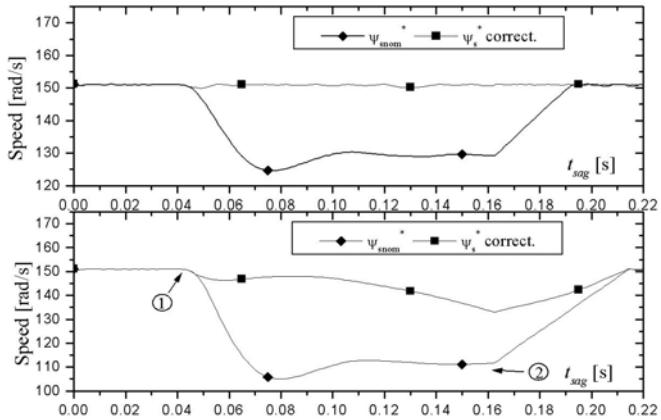

Fig. 7. Motor speed drop during voltage sag in drive with DTC (① - point of sag start, ② - point of sag end): U_{sag}=80%U_n (top); U_{sag}=70%U_n (bottom)

Flux and torque hysteresis controller in DTC bring to excellent dynamic performances in transients. Response rapidity will be dominant determined by low-pass filter transfer function in DC-bus voltage measurement loop.

Having in mind that the induction motor, whose parameters are given in this paper, with small pull-out torque (177%T_{nom}), for all voltage sags with voltage magnitude less than 77% of nominal supply voltage, leads to the motor torque less than nominal load torque and speed drop is unavoidable. Generally, induction motors have pull-out torque greater than 200% of rated torque; so it is the way when speed drops during voltage sags at 70% of nominal value can be avoided.

V. CONCLUSION

PWM inverter drives will shut down at voltage sag, initiated by their under-voltage or over-current protection scheme. As can be seen from the results shown previously the type and magnitude of symmetrical and asymmetrical voltage sags have significant influence to the ASD sensitivity. Also, different motor loading conditions and different motor speeds influence on ASD voltage sag sensitivity. It should be stressed that the presented results of simulation show significant influence of control algorithms to adjustable speed drives sensitivity. Modern adjustable speed drives (IFOC and DTC) demonstrate lower voltage sag sensitivity especially due to impossibility of the over-current reaction (if the user settable maximum current/torque values lower than maximum protection ones).

In this paper is also presented the voltage sag influence on the drop of speed. Regular control algorithms are able to cause the drop of speed which cannot be accepted in some industrial application. Control algorithms in IFOC and DTC drives can be simple modified to maintain speed drop at a minimum. Very good dynamic performances are found in regard to speed drop in both speed closed loop ASD's. Having in mind motor speed drop, DTC drive is simple to adapt to voltage sag than one with IFOC. Future researches will be faced to practical implementation of the proposed algorithms for speed drop minimization during voltage sag and speed synchronization in multi-motor drives along and after the voltage sag.

REFERENCES

[1] S. Ž. Djokić, J. V. Milanović, D. J. Chapman, M. F. McGranaghan, "Shortfalls of Existing Methods for Classification and Presentation of Voltage Reduction Events", (to be published in IEEE Trans. On Power Delivery)

[2] M.H.J. Bollen, "Characterisation of voltage sags experienced by three-phase adjustable-speed drives," *IEEE Trans. Power Delivery*, vol. 12, no. 4, pp. 1666-1671, oct. 1997.

[3] W. Leonhard, "Control of Electrical Drives," *Springer - Verlag*, Berlin, 1996.

[4] I. Boldea and S. A. Nasar, "Vector Control of AC Drives," CRC Press, 1992.

[5] V. Kostic, N. Mitrovic M. Petronijevic and B. I. Jeftenic, "Direct Torque Control", 12th International symposium on Power electronics, Novi Sad, Serbia and Montenegro, T2-1.5, CD-ROM, 2003.

[6] S. Ž. Djokić, J. V. Milanović, K. Stockman and R. Belmans, "Voltage-tolerance Curves of PWM Drives: Comparison of Simulations and Measurements", 12th International symposium on Power electronics, Novi Sad, Serbia and Montenegro, T6-1.3, CD-ROM, 2003.