Equipment for Direct Digital Synthesis of Synchrounous Analog Test Signals.

Petre Tzvetanov Petrov

Abstract: **The paper is giving description of equipment for direct digital synthesis of synchronous analog signals with staircase function approximation. The board is EPROM-based with two 8-bits DACs and could generate simutaneously two analog signals with sampling factor N=Fd/Fs from 1 to 256. Also, it is producing up to 32 diffrenent preprogrammed test signals. Moreover, a set of synchronous pulses produced by additional board could be generated. Several bords with common clock and reset could be used to generate more than two synchronous analog test signals. The equipment is build for educational, research and testing purposes.**

Keywords: **direct digital synthesis of analog signals**

I. Introduction and advantages of the method

Sometimes during the testing of electronic equipment it is necessarily to generate simultaneously and sinchronously two analog test signal, eg. sinusoisdal signal (SS) and cosinusoidal signal (CS) or a SS with frequency F and SS with frequency 2*F, etc. One of the simpest and chipest method to do that is with the so-called method of "direct digital synthesis of analog signals" (DDAS). With this method the samples are directly read from a table and then put into a DAC data register without any additional calculations.

The method has the following advantages compared to the analog signal generation:

1. High precision and predictability of all parameters of the generated signal (frequency, amplitude, phase, total harmonic distortion (THD), intermodulation distortion (IMD) etc.)
2. Opportunity to generate almost every analog signal given by a formula or a table with digital codes.
3. Changing of all parameters of generated analog signal in a large scale.
4. Fully programmability of all parameters.
5. The equipment is useful for automatic test or control equipment.
6. Programmable and controlable spectrum of the produced analog signal.

Petre Tzvetanov Petrov is mith Microengeneering-Sofia, Bulgaria. Emails: ppetre@caramail.com , ptzvp@yahoo.fr

7. Large band of generated analog signals (from direct current to megahertz).
8. Possibility of simultaneous and synchronous independent generation of many analog signals.
9. The equipment based on the method is simple and low cost and could have a lot of implementations based on different programmable components.
10. The equipment is useful as a programmable function generator.
11. The equipment could be used as a prototype for building specialized programmable boards, blocks and integrated circuits.
12. The DDAS is the fastest possible digital method for analog signal generation because the programmable synchronous counter is the fastest programmable digital processor, for addressing a table with signal data.

All these advantages and many others are the main raisons to develop and implement several digital boards for DDAS and one of them is discussed in this article.

II. General description of the method and the board

The discussed board for DDAS, shown in Figure 1, is based on tables with analog samples and is built from the following blocks:

1. Table with pre-calculated samples. The samples could be put within any appropriate type of programmable memory devices. In this case two 8KByte EPROMs (one per output function) are used. The board is generating synchronously two output signals with 1 to 256 samples per period. Each sample could have from 1 to 8 bits ot data.
2. Address generation unit. This unit is generating the addressees within the tables with digital codes representing the analog signals to be generated. Synchronous binary or decimal counters could be used. A fast RISC microcontroller is a possible but not always acceptable alternative.
3. Output register to hold the codes read from the memory.
4. DAC to convert the digital codes read from the memory into an analog signal (current or voltage).

The equipment is intended to be used with:

1. Additional analog filters for adjusting the form (spectrum) of the generated analog signal.
2. Amplifiers in order to obtain higher voltage, current and power.
3. Clock generator with fixed or variable output frequency Fd between DC and several megahertz. In this case Fd is limited mainly by the access time of the memory and the convertion time ot the DACs.
4. Spectrum analyzers.
5. THD and IMD measurement equipment.

The used DAC AD558 has typical conversion time of 800ns (Tctyp=800ns, Fctypmax=1/Tctyp=1.25MHz). This is giving the opportunity to use clock frequency higher than 1 MHz in most of the cases.

In Table 1 are given the maximum frequencies of the generated output "analog" signal (a staircase function approximation (SF) of a SS) depending on the selected sampling frequency Fd and sampling factor N=Fd/Fs.

Table 1. Frequency of the output sinusoidal signal Fs, depending on the sampling frequency Fd and sampling factor N=Fd/Fs.

Fd=640KHz, Td=1.5625us							
N =Fd/Fs	4	8	16	32	64	128	256
Fs [KHz]	160	80	40	20	10	5	2.5

Notes: 1. Fd is the discretization (sampling, conversion) frequency. Fs is the output (analog) signal frequency, the frequency of the generated SF or SS. 3. N=Fd/Fs is the sampling factor or number of signal's samples per period.

III. Hardware implementation

The equipment has two principal units: 1/ function generator and 2/ synchronous pulses generator. Only the first part is shown in Figure 1 and a short explanation of the blocks in the unit is given below:

1. Input stage with Shmitt trigger and protection to produce square wave signal with good quality for the address counters. The sampling (discretization) frequency Fd shold be applied at the input Fd (external clock).
2. An 8-bit programmable synchronous binary counter built by two LSTTL ICs 74LS161/3 for address generation. The maximum number of addresses in one page is 256. Decimal counters 74LS160/2 could be used instead but in this case the size of one page is 100 bytes and the sampling factor N=Fd/Fs will be from 1 to 100. The initial value of the counters is programmed with mecanical switches. The counters could be stopped by stopping the external clock and cleared by external Reset.
3. EPROM 27XXX (in this case 2764 is used but this is not obligatory) with tables of digital codes representing the staircase functions of analog signals to be synthesized. Up to 32 pages (tables) are available in one memory 2764 (32pages x 256 bytes=8192 bytes). One table contains one or more periods of signal to be generated. For example one page could have one period with 256 samples, two periods with 128 samples each, four periods with 64 samples each, etc. Also, one period of the signal could contain any number of samples from 1 to 256 (N=Fd/Fs from 1 to 256) because the address counters are programmable. The contents of both EPROMs are independant and two-diferent sychronous signals are generated.
4. The output data registers 74ALS273 for writing and maintaining the code read from the EPROM in the end of each clock cycle Td. The register is obligatory in order to maintain the stability of the output voltage of the DAC and to reduce the dependability of the DAC output from the EPROM access time.
5. One eight bit DAC AD558 per output channel (analog signal), with typical conversion time (Tc) of 0.8us and with maximum conversion time Tcmax=1.5us.
6. The output code from the EPROM is brought to the connector and could be used from any suitable external DAC and synchronous pulses generation unit.
7. Block with switches for selection of the active page in the memory. Each page is 256 bytes long. The starting address of the page is $XX00 and the last address is $XXFF, where XX is the memory page number from 0 to 31 (from $00 to $1F).

The equipment is giving the opportunity to experiment with nimber of bits n from 1 to 8 bits and to simulate a DAC with the same number of bits. The used method could be masking (truncation) or rounding of the unused bits. This is giving the possibility to evaluate the parameters (form, spectrum, THD, etc) of the output signal in function of the selected number of bits n. The equipment could produce one fraction of the period, one or more periods of a periodic signal.

IV. Conclusion and field of application of the described method and equipment

The disscussed signal generation method and board are useful in the following research and educational areas:

1. Evaluation THD of the generated signal (in particular SS) in function of conversion factor N=Fd/Fs;
2. Evaluation THD of the generated signal (in particular SS) in function of number of digital bits n (from 1 to 8) of the code.
3. Selection of analog or digital filters in function of the parameters of the signal to be generated.
4. Digital synthesis of "analog" signal with almost any form.
5. Comparison between rounding and truncation of the digital codes during the signal generation.
6. Testing and selecting DACs for signal synthesis.

The principal method is based on pre-calcualted tables with digital codes representing a staircase function and has the following advantages:

1. The contents of the memory could be standardized and used for standard tests and calibration procedures in order to compare electronic equipment from different sources.
2. The highest frequency of the digitally generated analog signals because the synchronous counter is the simplest and perhaps the fastest processor able to address the memory table with the signal codes. The arithmetic methods are giving lower frequency range are more expensive and more complicated.

3. The method could generate the analog signals with almost any possible form described with formula or table.
4. The frequency of the output signal is from direct current (DC) to many megahertz, depending on the implementation.
5. The output signal could be unipolar (with or without offset) or bipolar depending on the used DAC and amplifiers.
6. The amplitude of the output signal could be adjusted in large range with additional DAC or digital potentiometers, voltage dividers, amplifiers etc.
7. The methods with tables is simple, clear and reliable and has two independant phases: 1/ Calculating the contents of the table, which could by done on a PC, MPU/MCU kit, MPU or MCU system and there is no need to be done in real time. 2/ real time generation of the analog signal with the digital codes in the table.
8. The proposed method and electronic boards could be implemented with low cost ICs. Moreover, the board could be realized as programmable peripheral board, block or specialized ICs, controlled by a MPU or MCU, or even to be incorporated in a MCU or digital processor as a programmable output block for signal synthesis.
9. The method is giving possibility to produce a standart memory IC with large volume e.g. 64Kx8bits EPROM 27512 (256 pages x 256 bytes) with many standard signals in order to evaluate and compare analog and digital equipment and to do a research in the field of sampling and filtering.
10. The memory size, the number of bits of the counters and number of bytes in one page could be easy augmented in order to produce SF with higher precision (number of bits) or samples per period.
11. The method is giving the possibility of simultaneous and synchronous synthesis of two or more analog signals with the same or difference frequencies and the same or different forms (e.g. sinusoid, square wave, triangular wave etc.) with the same or separate address counters, but with individual memories and DACs.
12. The boards could be used with digital frequency synthesizer in order to obtain more output frequencies.

The method is simple and flexible for application. It gives the opportunity not only to examine the results of discretization of analog signals but also to evaluate low frequency equipment such as amplifiers, filters, preamplifiers, loudspeakers, voltmeters etc.

The discussed electronic boards has the following main areas of application:

- didactic and research equipment for studding digital signal synthesis
- testing equipment for low frequency amplifiers, filters measurement systems, analog and digital filters etc.
- systems for special sound effects
- control equipment
- programmable peripheral block with MPU or MCU control.

More information about the integrated circuits in the equipment and a lot of useful application notes how to use them could be found in [1, 2, 3]

V. References:

1. Texas Instruments. Selection Guide and data Book. Logic CD ROM. February 2000. USA
2. Analog Devices, Integrated Circuits. 1984 Data Book. Volume 1.
3. Intel Corp. Memory components Handbook 1993. USA.

VII. Appendix

Schematic diagram of the electronic board for direct digital synthesis of two synchrounous staircase functions, representing analog signals (Figure 1)