Failure Analysis of Semiconductor Devices

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Abstract - **This paper is devoted to problems, connected with failures of semiconductor devices. It is made a review of some fundamental requirements, which should be completed from semiconductor devices, reliability prediction approach, and prognostication methods. Some requirements, completed from the conditions by which the semiconductor devices and integral circuits should be tested, are presented by means of tables. Special attention is paid to the reliability problems, connected with the failures in some Insulated Gate Bipolar Transistors (IGBT). Failures of some power semiconductor devices are analyzed and their operated reliability is predicted.**

Keywords - **failure analysis, reliability of the electronic device.**

I. Some Requirements for the Reliability of the Semiconductor Devices

Reliability is the characteristic expressed by the probability that the part will perform its intended function for a specific period of time under defined usage conditions.

Every Company, producing semiconductors, should achieve best-in-class quality and reliability performance on all their products through a systematic approach that emphasizes quality at every phase of product development through manufacturing. From initial design conception to fabrication, test, and assembly; quality is built-in and assured through stringent SPC monitoring of fabrication and assembly processes, materials inspections, wafer level reliability, new product qualifications, reliability monitoring of finished product and strict change control management.

There are 2 basic types of failures, Early Failures and Wear Out Failures. These are reflected in the curve known as the Bathtub curve (fig. 1).

Companies, producing semiconductors, should use Reliability Testing to ensure all its products are below targets set for Early Failure Rates in PPM and Wear Out Failures in FITs.

Qualification. *New processes and new packages.* New processes and New Packages are qualified using a minimum 3 lot (77 units per lot) testing for: 1. Early Failure Testing (915 samples); 2. Operating Life Test; 3. Temp and Humidity Biased Test; 4. Temperature Cycling; 5. Auto-Clave; 6. ESD/ Latch-Up; 7. Board Level Temp Cycle (for packages). Power cycling and data retention testing is also done when applicable.

Smart quals. Products designed to process and package design rules and using qualified processes and packages are released using 168hr reliability data. This approach supports Time to Market needs without compromising reliability. In order to ensure there is no customer risk, it should be `create` a continuous reliability monitoring in place.

Reliability monitor program. An ongoing reliability mo nitor is in place to ensure that products manufactured to qualified processes under qualified reliability standards, has not drifted.

Dates of the reliability monitor program should be published in catalogs, reference book and handbook for semiconductor device; Test frequency is as posted below (Tab 1).

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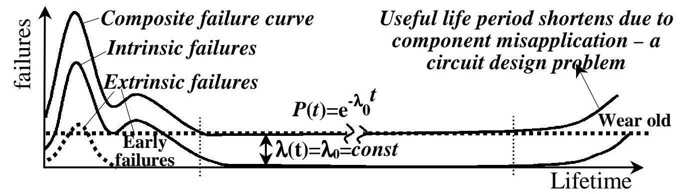

Fig.1 Illustration of intrinsic, extrinsic, and composite reliability curves for component hazard rate in a field-operating environment.

TABLE 1.

Test	Frequency
EFR (All major processes)	Every week
OPL (1000 hr)	Every 8 weeks
THBT (1000 hr)	Every 8 weeks
ACLV (96 hr)	Every 8 weeks
TMCL (1000 cycles)	Every 8 weeks

Fix reliability testing capabilities reliability test services and ESD and Latch-up testing labs are fully equipped to support the reliability qualification testing. Details of the lab equipment are listed in the following two tables. Reliability testing services equipment inventory.

TABLE 2. EQUIPMENT IN THE ESD/LATCH-UP LAB

	(eytek Zap Maste	RCDM	MK-2
Max Pins	256	N/A	768
HBM Voltage	25÷12000	50÷4000	50÷8000
MM Voltage	25÷2000	N/A	50÷2000
IEC 1000 Capable	Yes	No	No
On Board Clock	No	No	Yes
Vectored Latch-up	No	No	Yes

Failure mechanisms/failure models. Various failure mechanisms are tested during Reliability Testing. Major ones are listed below.

Determination of failure rate (point estimate). Failure rate can be determined by using actual test results. Determine “demonstrated” failure rate from actual test data as follows:

Failure Rate=No. rejects/sample size x no. hours.

Example 1. Assume a sample size of 13500, 2 failures and test duration of 500 hours. To calculate FR: FR=2 rejects/13500 devices x 500 hours; FR=2/6750000 device-hours=296.10^{-9} rejects per device-hour; 296 FITS (reciprocal of 296.10^{-9}) or 3375,000 hours MTBF.

In expressing failure Rate, the equivalent values below may be helpful.

Determination of failure rate (statistical estimates). In addition to point estimates, FR and MTBF may be estimated by using the chi-square statistic at 2(r+1) degrees of freedom. The 50% probability statistic would give the “best estimate”; the 60% or 90% probability statistic would give the upper confidence limit.

Acceleration factors. In order to express accelerated test results in terms of expected failure rate at actual use conditions, semiconductor manufacturers commonly use the Arrhenius model. The Arrhenius model assumes that degradation of a performance parameter is linear with time, with the rate of degradation depending on the temperature stress. To put it another way, the Arrhenius equation relates *t* where: he time rate of change of a process to the temperature at which the process

is taking place. If appropriate, the calculated acceleration factors listed in the following table may be used.

TABLE 3. FAILURE MECHANISM AND MODEL

Mechanism	**Model**
Failure Mechanism	Failure Model
Electromigration	Blacks Model
Excessive Intermetallics	Kidsons Model
Reverse Bias Breakdown	Tasca
Stress Dependent Diffusive Voiding	Okabayashi Model n NE 1, Okabayashi Model n EQ 1
Time Dependent Dielectric Breakdown	Fowler Nordhiem Tunnel Model
Slow Trapping	Positive Gate Voltage Model, Negative Gate Voltage Model
Metallization Corrosion	Plastic Metal Corrosion, Hermetic Metal Corrocion
Modular Case Fatigue	Shear Fatigue Model Case
Modular Case Fracture	Shear Fatigue Model Case
BGA Solder Fatigue	Time to fail by Creep,
Discrete Solder Fatigue	Dis Solder Jnt Cap 90pb10sn, Dis Soldr Jnt Fat Cap 63sn37pb
Flip Chip Solder Fatigue	Inner Flip Chip Revised, Hybrid Flip Chip Revised
Lead Seal Fracture	Principal Stress Model
Lead Solder Joint Fatigue	Thermal Cycle Fatigue Model
Lid Seal Fracture	Tensile Strength Model
Substrate Attach Fatigue	Substrate Attach Fracture Model, Substrate Attach Fatigue Model
Wire Bond Fatigue	Hu Pecht Dasgupta Model, Wirebond Pad Shear Failure, Bond Pad Fatigue Revised
Wire Fatigue	Hu Pecht Dasgupta Model
Electro Static Discharge	Wunsch and Bell Model, Wunsch and Bell Model, Wunsch and Bell Model

TABLE 4. RELIABILITY PARAMETERS

No. Failure Per Device-Hours	**Failu Rat**	**% Per 000 Hour**	**PPM, Hours**	**FITS**	**MTBF Hours**
$1/10^9$	10^{-9}	10^{-4}	10^{-3}	10^0	10^9
$1/10^8$	10^{-8}	10^{-3}	10^{-2}	10^1	10^8
$1/10^7$	10^{-7}	10^{-2}	10^{-1}	10^2	10^7
$1/10^6$	10^{-6}	10^{-1}	10^0	10^3	10^6
$1/10^5$	10^{-5}	10^0	10^1	10^4	10^5
$1/10^4$	10^{-4}	10^1	10^2	10^5	10^4
$1/10^3$	10^{-3}	10^2	10^3	10^6	10^3

Calculation of applicable junction temperature. Failure rates and MTBFs obtained from operating life tests pertain when the junction temperature is the same as the ambient test temperature. Temperatures used during OPL tests are usually T_A= 1250°C or T_A=1500°C. In most cases, these ambient temperatures are very close to the junction temperature T_J. However, when a significant difference between T_A and T_J exists, respective T_J must be considered. This would be the case with parts that dissipate significant amounts of power, such as certain linear and MOS devices.

To obtain FR and MTBF for a specific application where T_J differs significantly from T_A do the following: 1. Determine junction temperature for given application; 2. Calculate FR of MTBF at the applicable T_J, using the Arrhenius model. The equation for junction temperature for given application is:

$$T_J = T_A + P_D Q_{JA}\,, \tag{1}$$

where: T_J - junction temperature for given application; T_A - ambient temperature; P_D - power dissipated on the device (see datasheets for device); Q_{JA} - thermal resistance from junction to ambient (see datasheet).

TABLE 5. ACCELERATION FACTORS FOR COMMON JUNCTION TEMPERATURES AND COMMON ACTIVATION ENERGIES

Est. R_J accel. tests	Estimated TJ9 normal use application					Energies for Activation, eV
	25°C	35°C	45°C	55°C	85°C	
125°C	49	31	18	12	3.7	
130°C	58	35	22	14	4.3	0.4
150°C	89	60	37.4	24	7.3	
125°C	134	71	39.4	22.6	5.1	
130°C	160	85	47	27.1	6.1	0.5
150°C	317	169	92.6	53.4	12	
125°C	942	388	171	77.6	9.7	
130°C	1,218	500	219	101	12.6	0.7
150°C	3,159	1,300	569	259.1	32.7	
125°C	2,540	914	358	145	13.6	
130°C	3,377	1,221	476	193	18.1	0.8
150°C	10,041	3,632	1,414	575	53.8	
125°C	6,691	2,140	735	272	18.8	
130°C	9,174	2,964	1,006	370	26	0.9
150°C	31,256	0,10	3,429	1,261	88.2	

Example: Assume use condition for device LM741 is T_A= 50°C, $V_S = \pm 20$V. Determine T_J.

Solution: Datasheet for LM741 gives P_D = 150mW, and Q_{JA}= 150°C per walk. T_J = 50°C + 0,150 × 150°C = 72,5°C.

Confidence Factors. The failure rate resulting from a High Temperature Bias test is an average, or estimate, of the typical expected failure rate for a product or process; but has no statistical boundaries established.

Companies, that produce semiconductors, should use generally states the upper 60% confidence limit for failure rate estimate using the chi-squares statistic, per the following formula.

$$\lambda\max = \frac{\chi^2_{1-\alpha}[with\ df = 2(r+1)]}{2t} \tag{2}$$

where: λ_{max} - maximum failure rate or worst case; χ^2 - chi square distribution; r - number of failures; df - degrees of freedom; t - total number error test hours (number of devices x number of hours); α - statistical error expected in estimate (for 60% confidence α=0,6). α can then be interpreted to mean that we can state with statistical confidence of α (i.e., 60%) that the actual failure rate is equal to or less than the calculated max. failure rate (λ_{max}). Values of chi square are found in a number of statistical tables. A few more typical values are shown as follows (Table 6).

The fundamental theory governing the process of evidence evaluating is a principle of logic known as prediction (Bayes') theorem. The Bayes' prediction approach to reliability prognostication has been used for many years in specific applicati-

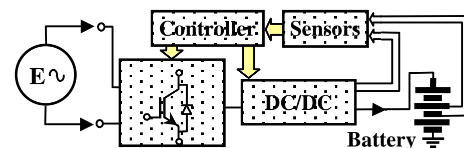

Fig. 1 The block diagram of a battery charger

ons due to certain advantages over traditional reliability analysis. Prognostication of the reliability is needed in the desing process to be able to build dependable systems that fulfill strict requirements regarding reliability and availability. Several models exist that are able to provide designers with an estimate of device or system reliability, however they have been found inadequate to predict the reliability of components in a number of situations, leaving the design engineer without a valuable tool for estimating the reliability of a system. The lace of accuracy of the models is usually related to the difference among the factors used to generate the model and the ones found in actual applications. Only when the application is very close to the one intended in the model, reliability prognostication can be done with a certain lover of confidence on the results.

Among the lots of components that are part of even the simplest electronic system, power devices play a fundamental role. These components are part of the power supply circuit that feeds the rest of the system, or part of the actuators that interact with the environment as outputs of the system. In each case, power devices have to work under heavy stress conditions; hence highly reliable components are required.

TABLE 6. PERCENTILES OF THE CHI^2 DISTRIBUTION. (VALUES OF CHI^2 CORRESPONDING TO CERTAIN SELECTED PROBABILITIES)

Typical Use		AQL	Best Estimate	60% Confidence	LTPD or 90% Confidence
Probability, %		5.0	50.0	60.0	90.0
1-α		0.05	0.50	0.60	0.90
df	Total Failures				
2	0	0.103	1.390	1.830	4.61
4	1	0.711	3.360	4.040	7.78
6	2	1.640	5.350	6.210	10.60
8	3	2.730	7.340	8.350	13.40
10	4	3.940	9.340	10.500	16.00
12	5	5.230	11.300	12.600	18.50
14	6	6.570	13.300	14.700	21.10
16	7	7.960	15.300	16.800	23.50
18	8	9.390	17.300	18.900	26.00
20	9	10.900	19.300	21.000	28.40
22	10	12.800	21.300	23.000	30.80
26	12	15.400	25.300	27.200	35.60
32	15	20.100	31.300	33.400	42.60
42	20	28.200	41.300	43.700	54.10

II. RELIABILITY OF THE POVER SEMICONDUCTOR DEVICES

Novadyes, the desing of highli efficient power supples can be accomplished using new power devices like Insulated Gate Bipolar Transistors (IGBTs). This kind of devices csn be directli connected to AC power supplies and can be used at switching frequencies of up to 40 kHz, whith allaws for the design of power supplies with very low harmonic distortion and high efficency. The general diagram of a battery charger that uses IGBTs in the rectifier stage shows in fig. 1, and table.7 shows some results from the reliability testing of IGBT.

Different current levels are supplied to the battery through an integrated modular DC/DC converter. The entire system is monitored and regulated by a controller that uses information from external sensors and an algorithm to perform an optimized charge.

High dependability is a fundamental requirement for this system, because of the potential harm to the environment (persons or machines) that can result from a failure. Our research focuses on the design of dependable systems through the use of highly reliable components and the application of design techniques that ensure correct operation or, in case of failure, safe outputs.

TABLE.7 RESULTS FROM THE RELIABILITY TESTING OF IGBT

Part Number Type		Package		Die Type	
HGT4E40N60B3S		TO-268		49052	
Stress	**Conditions**	**Duration**		**Results**	**Sample Size**
Drain Bias	Tc=150°C, Vds=80% Rated	1000	Hrs	2[(1)]	40
Thermal Fatigue	PD=40W, delta Tj=100°C	10,000	Cyc	INC	40
Temp Cycle	-65°C, +150°C, Air	1000	Cyc	2[(1)]	40
Relative Humidity	Ta=85°C, RH=85%	1000	Hrs	2[(1)]	40
Pressure Cooker	Ta=121°C, 15psi	168	Hrs	0	40
Operating LIfe	Tc=150°C, Vds=15V	500	Hrs	0	40

Note 1. High ICEs/IGEs due to cracked Nitride

This paper describes our work on the first aspect, i.e., highly reliable components. The target device that we characterize is the IGBT because of its fundamental role in the system depicted in fig 1. IGBTs combine the best features of MOSFET and bipolar transistors, delivering high output impedance (insulated gate), and low conduction loss (bipolar transistor). Typical applications are AC/DC switch-mode power supplies, high voltage DC/DC, power factor correction stages, automotive ignition systems and motor drive systems.

A. Reliability tests and results

Design of dependable systems is done on the basis of accurate reliability prediction models that help the design engineer to choose the appropriate components for every application, and impose design c1onstraints of the system by providing the expected mean time to failure. Prediction models such as described by MIL-HDBK-217 are widely accepted in industry, however they do not provide accurate values in a number of situations. In this section we present the reliability tests that are part of the first phase of our research, where the goal is to determine degradation models for the power device presented in the previous section. Several environmental tests, as described in [4], have been applied to a set of ten IGBT pairs. Tab. 8 shows a short description of the tests and their characteristics.

Every test has a well-specified set of conditions, and a detailed application procedure. For instance, under test 103B, (Tab. 8) devices are exposed to high relative humidity (90 to 95 percent), at an elevated temperature (40°C), for a period of time that depends on the test condition. There are four conditions, *A*, *B*, *C*, and *D* that correspond to lengths of 96, 240, 504 and 1344 hours each. Materials that are sensitive to moisture can deteriorate rapidly under the mentioned conditions.

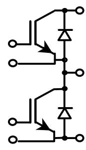

Fig. 2 Symbol of the IGBTs under test

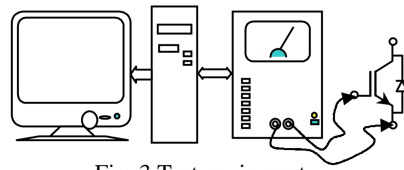

Fig. 3 Test equipment

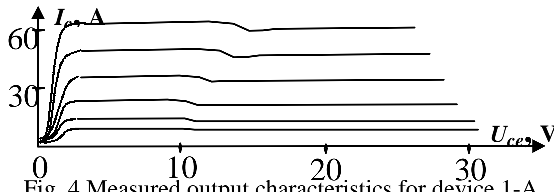

Fig. 4 Measured output characteristics for device 1-A

Fig. 2 shows symbol of the IGBTs under test, and Fig. 3 shows our current layout to carry out the tests Devices are placed in a climatic box, where accelerated tests take place. A programmable high-power curve tracer, attached to a PC for data analysis, is used to extract and compare the electrical characteristics of the power devices before after each test. We evaluate not only the number of components that pass/fail every test, but also the degradation of the characteristics of the devices with time. Several software packages - some developed in our group, are used to software packages - some developed in our group, are used to interact with the curve tracer, store and analyze experimental data.

B. Experimental results

The experiments were conducted using a sample of 12 IGBTs. These devices come in pairs enclosed in a ceramic package, which makes them very resistant to environmental stress as we observed throughout our tests. We numbered every device from 1 to 6 (six packages), A or B (two devices per enclosure); for instance, device 3-A would be the first device in package 3. Experiments took place over a period of 5 months. Environmental tests (Temperature and humidity) were applied to the devices in a climatic box for more than 1800 hours. The electrical characteristics of each device were measured before and after every test at an environment temperature of 20 °C (±5%). In addition, visual inspection was done to assess the degradation of the ceramic enclosure and metallic contacts.

TABLE 8 ENVIRONMENTAL TESTS

Test	Name	Description	
		Time, Hours	**Temperature, °C**
108A	**Humidity (steady state)**	**240 (*condition B*)**	**40**
	Humidity (steady state)	**504 (*condition C*)**	**40**
103B	**Life**	**96 (*condition A*)**	**70**
	Life	**504 (*condition C*)**	**70**
	Life	**504 (*condition C*)**	**150**

A set of measurements was done for every device, to verify if it failed, and to extract its electrical output characteristics. Using a power curve tracer, the device was characterized at six different gate voltages (*Uge* in Table 9). For every *Uge*, 40 measurements were taken for collector-emitter voltages (*Uce*) ranging from 2.5V to 63V, which rendered collector currents from 1A to 70A. Fig. 4 shows the measured output characteristics for device 1-A before any test was applied. The different curves correspond to several *Uge* values. Table 9 shows a summary of measurements for device 2-A before and after the second test (Test 103B condition C. See Table 8). The parameter *S* is defined as *Ic*/*Uge*.

After analyzing the collected date, we could realize of the excellent resistance of this devices to environmental stress. None of the devices failed, or even had a noticeable variation in its electrical characteristics. Therefore we could not conduct a more detailed analysis to obtain activation energy, mean time to failure, or degradation models, as it was our objective when we started this phase of our research. The devices result to be more reliable than expected, which changes our focus for the second phase of our research, where we are planning to conduct tests that stress the devices while in operation.

Another conclusion obtained from the data was related to the measurement process itself. The variation between the electrical characteristics of a device, measured before and after a test, is of the same order as the variation of the characteristics between two consecutive tests. This fact shows that the electrical characteristics of the devices were not affected by our environmental tests. It also surfaces a flaw in our measurement methodology. While we carefully planned the tests, characteristics to observe, and measurement conditions, we did not anticipate the small variations that the devices would show, therefore our measurement procedure was not precise enough to obtain accurate data. Fig. 5 shows an example of the variation between measurements. The figure shows the maximum variation of a measurement (*S*) between two consecutive tests, and within a particular test. Data for the figure is taken from device 4-A, tests 2 and 3.

TABLE 9 MEASUREMENTS FOR THE DEVICES BEFORE AND AFTER THE TEST

Voltages		After test		Before test		Distinction
U_{ge}, V	U_{ce}, V	I_c, A	S, Ω^{-1}	I_c, A	S, Ω^{-1}	ΔS
8,1	20,7	10,3	1,28	10,4	1,29	0,01
8,6	20,3	17,4	2,04	17,6	2,05	0,01
9,1	20,4	27,1	2,99	27,5	3,04	0,05
9,6	20,5	39,1	4,08	39,8	4,16	0,08
10,1	20,5	53,0	5,27	54,1	5,37	0,10
10,6	21,1	68,1	6,45	69,7	6,59	0,14

III. CONCLUSIONS

The maximum variation of the conductance is below 0.04 for any particular test, while the variation between the measurements after one test, and before the following, is also in the same range (0.025 in the example of Fig. 5). Because of this, we can not extract any conclusion about the possible degradation of the characteristics of the devices after applying the tests, however conductance seems to increase steadily for all devices.

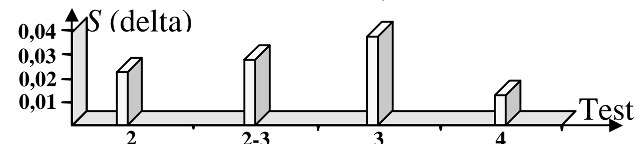

Fig. 5 Maximum variation of *S* within a test, and from test to test

Despite the aforementioned flaw in our methodology, we accomplished important objectives with our tests:

- Assess the resistance to environmental stress of the devices we selected. This is an important conclusion for our research in the design of reliable battery chargers.
- Establish and improve the flow for he second phase of our research, where we will be using the same equipment (climatic box, curve tracer, and analysis tools).

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