# Research and Implementation of Direct Digital Synthesis (DDS) in Programmable Logic Devices

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*Abstract* – **The flexibility of the Direct Digital Synthesis (DDS) makes it suitable for synthesis of generators for application in many areas of the electronics. It is a common practice to use PLL for transistor converter control. This function could be implemented in analog or digital way. The alternative representation of the analog function is done by digital logic blocks, implemented by specialized integrated circuits or inside programmable logic devices. This paper presents the use of DDS as numerically controlled oscillator (NCO), implemented inside a Complex Programmable Logic Device (CPLD).**

*Keywords* – **Direct digital synthesis, PLL, phase ripple, programmable logic device.**

## I. INTRODUCTION

The basic advantage of the digital synthesis is that the output frequency could be regulated fast and with high, a-priory stated accuracy of the value and the phase. This approach is spreading vastly in various fields of the digital electronics, and particularly in Digital Control Systems. With the development of new integrated circuits it becomes possible to implement the analog Phase-Locked Loop (PLL) function in alternative (digital) ways. The implementation of digital functional blocks inside an integrated circuit (programmable logic device) allows for operation at higher frequencies with smaller temperature error.

The union of algorithms and architectures for this purpose allows for the development of the necessary combinational and register structures, programmable generators, digital phase detectors, digital filters, etc. inside a single chip.

The goal of this research is to develop a possible application of DDS in control systems for transistor power converters. The application of DDS as Numerically Controlled Oscillator (NCO) is accompanied by the presence of a phase ripple (phase noise) [5] which must be compensated to certain extent.

## II. DIGITAL PLL

The control of transistor power converter devices widely uses Phase- Locked Loop function, which adapts the control system to the characteristics of the converter according to given algorithm.

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Fig.1 shows basic digital PLL, consisting of phase detector DPD, which converts the phase difference in a signal with certain duration, digital filter DLF, which converts the signal from the phase detector and digitally controlled oscillator DCO [1].

During the system operation the frequency fout of the output signal of the DCO aims to match the input frequency fin with certain accuracy. The change in the input frequency fin causes an increase or decrease of the phase difference between itself and the output fout, which leads to a tendency of frequency matching fin = fout.

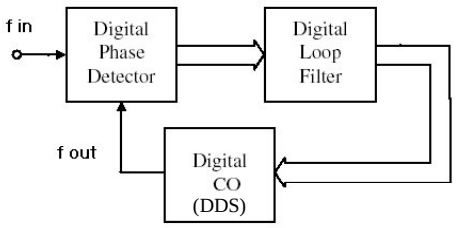


Fig.1. Digital PLL

It is essential that the output signal of the phase detector is processed. In this case the controlled oscillator DCO is based on DDS, thus it's necessary that the output signal of the detector is converted into a binary number.

It's possible to use filter- converter of time duration into digital code. The acquired code (word) N directly controls the oscillator, changing its frequency proportionally to the value of N – Fig.2. A requirement of the synthesis is that the clock frequency CLK is much greater than the frequency of the EVENT input – Fig.3 [2].

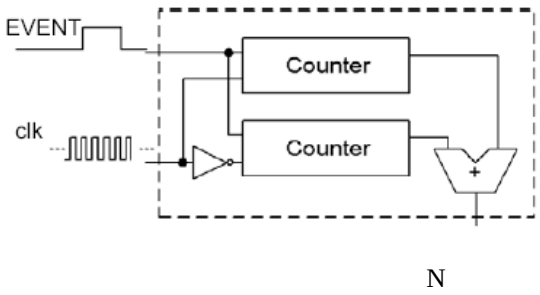


Fig. 2.Time-to-digital-code converter.

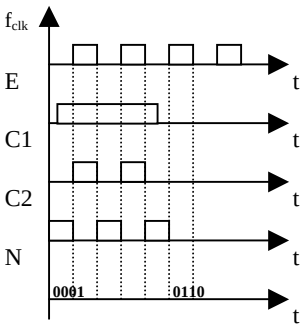


Fig. 3. Waveform of the time-to-digital-code converter.

## III. PULSED-OUTPUT DDS

A simplified diagram of a DDS is shown in Fig. 4. The basic building blocks are Phase accumulator, P2A – phase-to-amplitude converter (a sine waveform, stored in memory), Digital-to-analog converter and low-pass filter [3], [4].

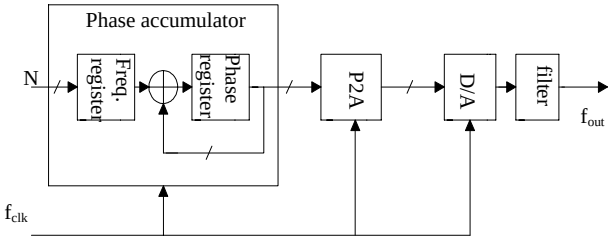


Fig.4. Block Diagram of a DDS.

DDS is normally carried out by specialized integrated circuits like the AD9830, manufactured by Analog Devices. Due to the fact that the transistor converters need only a pulse train only the phase accumulator can be used, which turns the DDS into so-called pulsed- output DDS.

The pulsed- output DDS is one of the application forms of DDS. It consists of only the phase accumulator, who's carry output (or the most- significant bit of the accumulator) is used as an output. The research and implementation of the DDS is carried out using PLD of the Xilinx Corporation, namely S10PC84 and the Xilinx Foundation software. An 8-bit accumulator is implemented (as shown in Fig.5), and the waveforms for its operation are shown in Fig. 6.

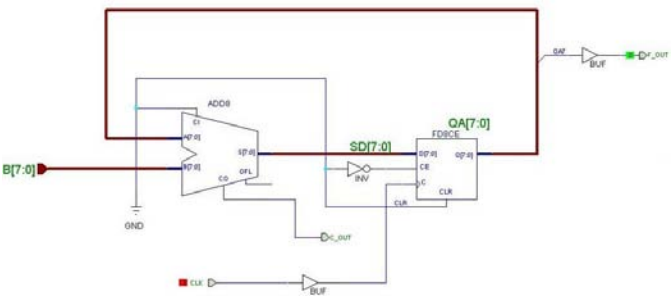


Fig.5. 8-bit wide phase accumulator.

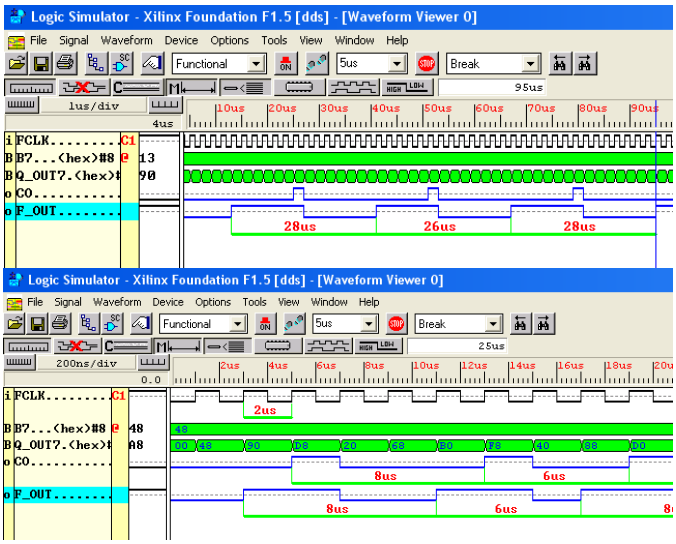


Fig.6. Waveforms of 8-bit wide phase accumulator operation.

The output frequency of the DDS is calculated from the equations:

$$f_{out} = \frac{N.f_{clk}}{2^k} \quad (1)$$

$$\frac{f_{out}}{f_{clk}} = \frac{N}{2^k} \quad (2)$$

Where the value of N determines the output frequency and k is the width of the adder and the register.

The frequency change step Δf is calculated according to:

$$\Delta f = \frac{f_{clk}}{2^k} \quad (3)$$

The maximal output frequency fout is fclk / 2, which will be acquired at 1/2N. The DDS operation is accompanied by a phase noise (phase jitter) of the output frequency with magnitude of 1/Tclk - Fig. 6. The presence of phase jitter is due to the fact that the accumulator can accomplish transitions only from integers, multiple to the clock period. Let us consider for example 4-bit wide phase accumulator (k=4) and an input word N=5. The ideal case should state that the accumulator must generate carry each 16/5 cycles, that is 3.2 clock periods, which is impossible. The real case introduces a phase jitter which will gradually decrease to zero and then increase to 1/Tclk. The first transition (Table. 1) must occur at 3.2 cycles, but it occurs after 4 cycles. The phase error is 4/5 of the period.

TABLE I.
N=5, k=4 (4-bit wide accumulator)

| Accumulator output | Carry output |
|---|---|
| 0000 (0) | 1 |
| 0101 (5) | 0 |
| 1010 (10) | 0 |
| 1111 (15) | 0 |
| 0100 (4) | 1 |
| 1001 (9) | 0 |
| 1110 (14) | 0 |
| 0011 (3) | 1 |
| 1000 (8) | 0 |
| 1101 (13) | 0 |
| 0010 (2) | 1 |
| 0111 (7) | 0 |
| 1100 (12) | 0 |
| 0001 (1) | 1 |
| 0110 (6) | 0 |
| 1011 (11) | 0 |
| 0000 (0) | 1 |

After the second transition the error is 3/5 from the period and the ideal case shows that the transition must occur after 6.4 clock periods, but it actually occurs after 7 periods. The relation between N and the carry C determines the phase error:

$$\varepsilon = \frac{C}{N} \tag{4}$$

The phase jitter reduction is normally done by output frequency division, for example by 4, which decreases the phase noise by a factor of 4, as it is a function of the output frequency [5].

An alternative is to use reset of the flip-flops at the end of the cycle using the carry output of the adder – Fig. 7.

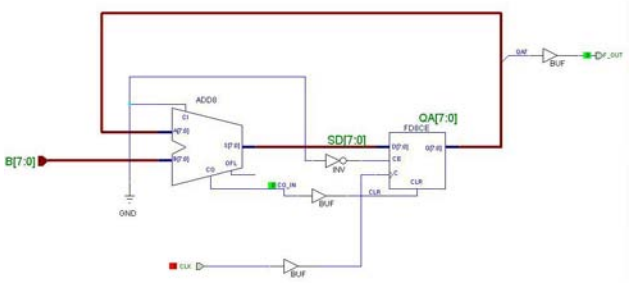


Fig.7. DDS with forced reset.

This approach changes the sensibility of the output frequency change. With the increase of the input word N the step with which the output frequency will rise will gradually increase. For example in Table 1 the first cycle begins with the value of 0 and ends with a remainder 4 after the carry, which happens on the fourth cycle i.e. after 4 Tclk periods. Forcing a reset actually causes the same cycle to be repeated each time by changing the value of the remainder, thus eliminating the phase noise, but also changing the step of the output frequency. Fig. 8 shows example waveforms of the clock frequency and output frequency of the DDS.

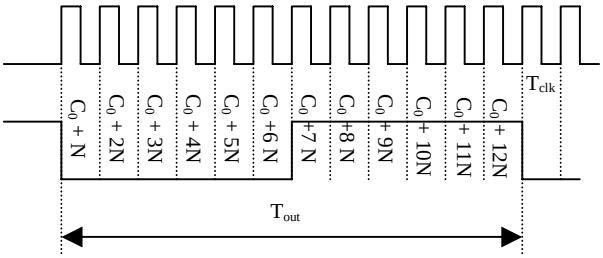


Fig.8. Output frequency and clock frequency

The value of the adder Sb depends on the count of the clock periods The count of the clock periods B is calculated according to:

$$B = \frac{T_{out}}{T_{clk}} = \left[\frac{2^k}{N}\right] \quad , \tag{5}$$

Where [x] is the round- down function, that returns the largest integer less than x. Thus, B is always an integer, and the adder value will be:

$$S_b = C_0 + B.N \tag{6}$$

Where C0 is the remainder value.

The overflow condition is $Sb \geq 2\kappa$ , so:

$$C_0 + B.N \geq 2^k \tag{7}$$

$$B \geq \left[\frac{2^k - C_0}{N}\right] \tag{8}$$

It is obvious that B depends on the remainder value C0, and since after reset C0=0, we come to:

$$B \geq \left[\frac{2^k}{N}\right] \tag{9}$$

The number of clock pulses B is always an integer (1, 2, 3, …) which determines the non-uniform change in the frequency step and the varying duty-cycle. To achieve 50% duty-cycle the output frequency must be divided in two by a T-flip-flop. The waveforms from the simulation of the schematic, depicted in Fig. 7 show clearly the non-symmetrical output and the absence of phase jitter – Fig. 8.

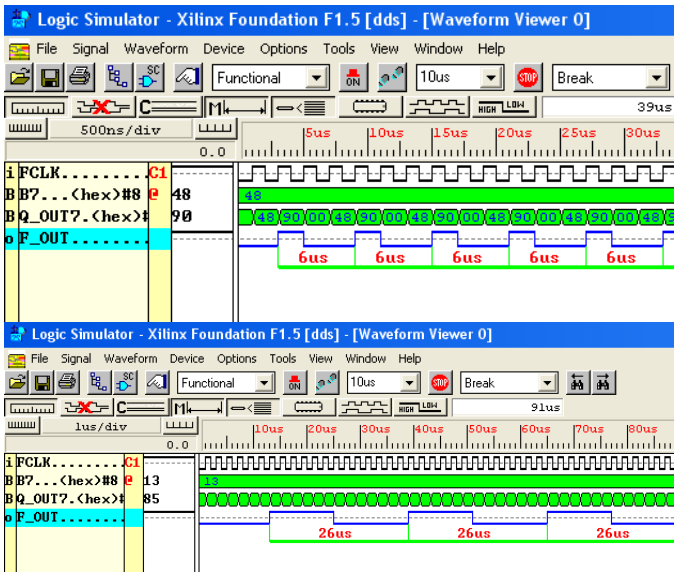


Fig.9. DDS with forced reminder zeroing..

The phase jitter elimination is on the price of the uniform output frequency change. In this case the change in output frequency is non- uniform and is given by the equation:

$$\Delta f = f_{clk} \frac{1}{B(B+1)} \qquad (10)$$

A small step is achieved with big values of the clock pulses B, i.e. smaller values of the input word N. The relation between Δf and N at different clock frequencies and the same phase accumulator architecture is shown on Fig. 9. It can be seen that a change in the output frequency for big N occurs only after serious increase in N, i.e. N being increased by more than 1. This effect follows directly from Eq. (9).

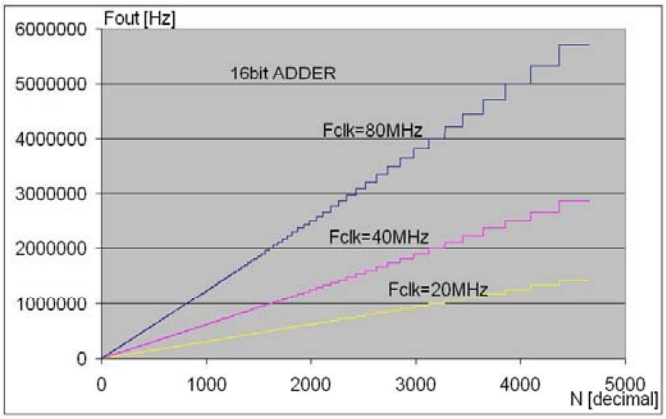


Fig.10. Relation between fout and N.

## IV. Conclusion

The developed and analyzed digital DDS generator with forced reset of the remainder has relatively low and non-linear sensibility with respect to the input word N.

In this case the DDS is applicable after limiting the actual range of values of N up to 5% of the maximal value of N, which in turn depends on the width of the phase accumulator.

## References


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