Results from Sampling, Reconstruction and Synthesis of Analog Signals with Microprocessor System

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Abstract: **There is a description of results from experiments with an analog input and output ports for a microprocessor-based system. The analog signal is sampled, converted into digital codes reconstructed and stored into the memory if necessarily. New ideas, theorems and rules for evaluation of the sampling and reconstruction process are proposed.**

Keywords: **sampling and reconstruction of analog signals**

I. INTRODUCTION

The conversion of analog signal (AS) into digital codes is one of the most important tasks during the data acquisition, measurement and digital signal processing. That is the reason to attempt to analyze and evaluate the errors during the analog to digital (A to D) conversions. Because the direct current (DC), the sinusoidal (SS), co-sinusoidal (CS) and multi-tone signals (MTS) are the basic test signals for the analog channels the results are given for them.

The paper resumes the results from sampling and reconstruction of AS with microprocessor system based on Motorola 6809 microprocessor unit (MPU) with additional hardware for possible synchronization of A to D conversions with the sampled AS. The approach described in [1] was developed and tested.

II. THE MICROPROCESSOR SYSTEM

The system based on the Motorola 6809 microprocessor is running at 1MHz+-0.01%. It is supported by the followings resources and was used as a principal controlling hardware: 4KB static RAM for the user program and data; 4KB EPROM with monitor program and constants; RS232C interface based on 6850; Motorola 6840 programmable timer module (PTM); six seven segments indicators; keyboard with 25 keys; expansion connectors for input output expansion boards and a power supply module for +-5V and +-12V. The block diagram of the system is shown on the Fig 1.

III. THE ANALOG PORTS

An additional board (called analog input and output port) was developed with an 8-bit analog to digital converter (ADC) and 8-bit digital to analog converter (DAC).

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The board is intended to convert synchronously or asynchronously (to a particular level crossing or point in the time) an AS into digital codes and digital codes into analog staircase function (step function). It is with one input for the AS and a possibility to test the analog port with on board reference voltage. The sample and hold circuit (SH) could be switched on and off in order to evaluate the influence of the SH to the accuracy and the maximal input frequency to be converted. The clock of the ADC is produced from the system clock E or by appropriate external TTL clock source.

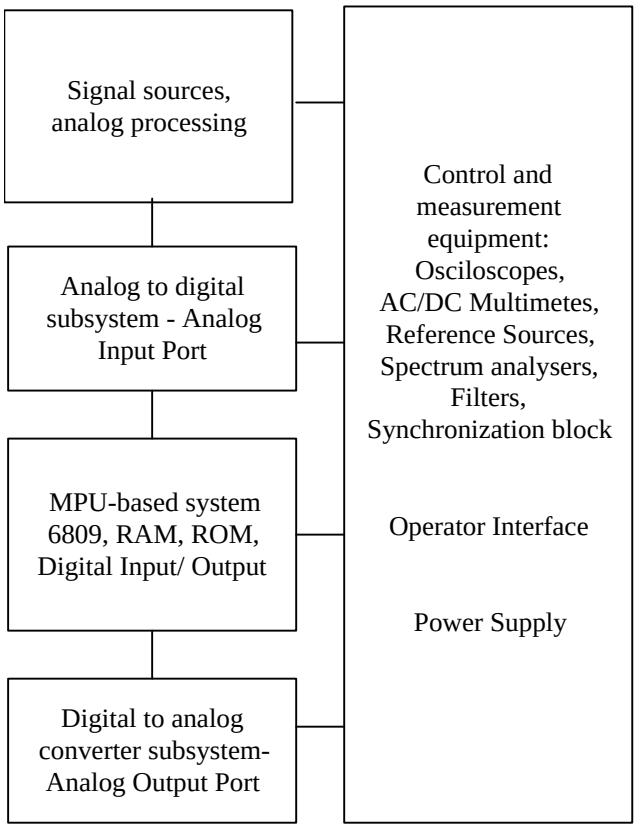

Fig. 1. Block diagram of Motorola 6809 MPU-based system with analog input/output ports for AS sampling and reconstruction.

The input analog port is build around the 8-bit ADC0801, a SH LF398 and source of reference voltage with TL431(A) normally adjusted to 5.120V. Under these conditions we have:

- reference voltage Vref=5.120V;
- minimum analog input voltage Vamin=0.00V;
- full scale analog input voltage Vfs=5.100V;
- one least significant bit (LSB) =Vref/2exp(8)=20mV.

A second analog port was tested with Analog Device AD570. ADC0801 and AD570 are not pin to pin compatible

but they have similar characteristics. AD570 has internal clock and internal reference voltage source.

The analog output port is build around the 8-bit DAC0808, operational amplifier LF356, 8-bit digital register 74HC273 and several resistors. DAC0808 is using the same source of reference voltage as ADC0801 or external voltage reference. In the first case the ADC and DAC has the same full-scale voltage Vfsadc and the same weight for the LSB (e.g. Vfsadc=Vfsdac=5.100V and LSB=20mV).

IV. Assembler Programs

The following programs in Assembler were developed:

1/ Converting the AS into digital codes with ADC and reconstructing it immediately with DAC. An example of such a program giving the maximum conversion speed of approximately 11KHz with name ADCDAC.ASM is given below. Since the time of the execution time is fixed and Fd = 1/Td =const the frequency of the sampled signal Fs should be changed in order to evaluate the influence of the different sampling factor N=Fd/Fs. The synchronization with a particular level of the sampled AS is not provided.

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* Name: ADCDAC.ASM (Motorola 6809 @ 1 MHz)
* Td =  91 us,  Fd =  10.989KHz,  Tadc = 64 us
                ORG     $200
ADC             EQU     $2000   ; ADC
DAC             EQU     $3000   ; DAC
* Sampling period Td = (5+72+14)us = 91 us
* Put SH in Hold Mode and START of the ADC
ADCDAC          STA     ADC     ; 5us;
* Wait (5*ACCA+2)us = 72 us; ACCA=14
                LDA     #14     ; 2 us
LOOP            DECA            ; 2 us
                BNE     LOOP    ; 3us
* Read ADC and put SH in Sample Mode
                LDA     ADC     ; 5 us ;
                STA     DAC     ; 5 us ; Write to DAC
                JMP     ADCDAC ; 4 us; Loop again.
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2/ Converting the AS with fixed number of bits n and variable SSF N (sampling frequency Fd).

3/ Converting the AS with variable number of bits n and fixed SSF N (sampling frequency Fd).

4/ Starting the analog conversion with programmable delay from the zero crossing of the signal in order to evaluate the influence of the ground noise and the amplitude of the samples to the quality of the reconstructed signal.

V. The Signal Sampling Factor

The term “signal sampling factor” (SSF) or encoding factor N is defined in [1] and is given by the Eq. 1:

$$N=Fd/Fs=Fd/Fmax>0 \quad (1)$$

where Fd is the sampling (encoding) frequency; Fmax is the maximal signal frequency to be converted (in case of band wide or multi-tone AS) and Fs is the frequency of sinusoidal signal (SS) or co-sinusoidal signal (CS) to be converted.

VI. The Factor of the Sample and Hold

In order to evaluate the role of the sample and hold circuit (SH) a parameter called “sample and hold factor” (SHF) Nsh was introduced and is defined by the Eq. 2

$$Nsh=Tadc/Tapsh \quad (2)$$

Where Tadc is the time of analog to digital conversion or the aperture time of the used A to D converter and Tap is the aperture time of the SH. In order to enlarged the band of the frequency converted with one ADC, normally we are in need of SH circuit with Nsh>>1.

VII. Basic Sampling Theorems

The equipment was intended primarily to test the new sampling theorem, discussed in [1] to evaluate the influence of the number of the converters bits n , the total harmonic distortion (THD) and intermodulation distortions (IMD).

The method of sampling and direct reconstruction of the AS was used and the analog “original” and its digital “copy” were compared. The signals before ADC and after the DAC were compared and processed. Several parameters (SSF, SHF), theorems and assumptions were formulated and are given below. They are applicable for a SSF N=Fd/Fs>=2. In some cases the reconstruction of the SS/CS is still possible with N<2 but we will not examine this case here.

Theorem 1: The maximum amplitude error Emax during the conversion of SS $A=Am*\sin(2*\pi*Fs*t)$ is given by the formula Emax = 1-sin(90-(180/N)), where N=Fd/Fs>=2 is the SSF and under the condition that the conversion error Econv is zero (Econv=0, the number of the converters bits $n=\infty$).

Theorem 2: If the maximal amplitude error Emax for a SS $A=Am*\sin(2*\pi*Fs*t)$ is given, the SSF N=Fd/Fs>=2 could be calculated with the formula N= 180/(90-arcsin(1-Emax)) and under the condition that the conversion error Econv is zero (Econv=0, the number of the converters bits $n=\infty$).

Theorem 3: The maximum amplitude error Emax during the CS $A=Am*\cos(2*\pi*Fs*t)$ conversion is given by the formula Emax=1-cos(180/N), where N=Fd/Fs>=2 is the SSF and under condition that the conversion error Econv is zero (Econv=0, the number of the converters bits $n=\infty$).

Theorem 4: If the maximal amplitude error Emax for a CS $A=Am*\cos(2*\pi*Fs*t)$ is given, the SSF N=Fd/Fs>=2 could be calculated with the formula N=180/arccos(1-Eamax) and under the condition that the conversion error Econv is zero (Econv=0, the number of the converters bits $n=\infty$).

The theorems 1, 2, 3 and 4 are giving the possibility to calculate the SSF N when the maximum amplitude error Eamax is known and vice versa. Once the SSF N is calculated it is easy to calculate the sampling frequency Fd using the formula given in [1] Fd = N*Fmax = N*Fs

Theorem 5: For a direct reconstruction of a sum of k SS and/or CS signals plus a direct current (DC) component at least N=3*k+1 samples are needed.

The Theorem 5 is based on the assumption that each of the signal components has at least thee independent parameters to

reconstruct : amplitude (Ak), frequency (Fk) and phase (φk) and one sample is needed to reconstruct the DC component. Assumption that the phases are zero (φk=0) and that the DC component is also zero (DC=0) does not reduce the number of the parameters to reconstruct.

A relation between the number of bits n in the digital word and the number of the frequency components k coded in the word was formulated and the following theorems are offered.

Theorem 6: The number of the SS and/or CS components k in a complex AS cannot exceed 2exp(n), where n is the number of bits n used to code this signal (k<= 2exp(n)).

Theorem 7: Every AS with limited slew rate (SR<∞) and limited peak to peak amplitude App (App<∞) could be approximated as a finite sum of SS and/or CS signals and a DC signal. Every SS and/or CS component in the sum has three basic parameters: amplitude, frequency and phase.

Definition: The simplest band wide signal (BWS) could be represented as a sum of a SS or CS and a direct current (DC) component and given with the formulas S=Asin(ωt+φ)+B or C=Acos(ωt+φ)+B. It has four basic parameters: amplitude A, frequency ω=2πFs or Fs, phase φ and a DC component B. Since four parameters should be transferred into digital form at least two bit will be needed to code them. In the paper for the signal frequency is used the abbreviation Fs.

Theorem 8: In order to reconstruct the simplest band wide signal given with the definition above at least four samples per period are needed or N=Fd/Fs>=4.

Theorem 9: In order to minimize the DC offset with direct signal reconstruction the SSF should be N=Fd/Fs = 4*p, where p is a positive integer number p=1, 2, 3…. Only the case with constant sampling intervals are concerned (Fd=const).

Table 1 is a resume of the amplitude and phase steps and resolutions during the A to D conversions of AS with an ideal converter. The phase resolution is important when the signal is containing more than one signal component with the same frequency but with a different phase (e.g. when a two or three phase 50/60Hz signals are summed and only one signal is produced and sampled).

VIII. LSB IN AMPLITUDE AND LSB IN PHASE

A parameter called "least significant bit in amplitude" (LSBa) defined with the formula LSBa=Vfs/(2exp(n)-1 or with the formula LSBa=Vref/2exp(n) is used in the sampling theory. Now, we could introduce the parameter "LSB in phase" with the Eq. 3

$$LSBph=360deg./N=360deg*Fs/Fd \quad (3)$$

Also parameters "Resolution in amplitude" (Ra) and "resolution in phase" (Rph) could be introduced with the corresponding Eq. 4 and Eq. 5

$$Ra=+-0.5*LSBa \quad (4)$$

$$Rph=+-0.5*LSBph=+-180deg/N \quad (5)$$

TABLE 1.
STEP AND RESOLUTION IN AMPLITUDE AND PHASE DURING THE ANALOG TO DIGITAL CONVERSION WITH AND AN IDEAL ADC

Parameter	Step (LSB) and resolution (R)
Amplitude (a)	LSBa=Vref/2exp(n) Ra=+-0.5*LSBa
Phase (ph)	LSBph=360/N Rph=+-0.5*LSBf=+-180/N

IX. CALCULATING THE NUMBER OF BITS

The discussed MPU equipment is offering the following possibilities:

1/ to transfer all of the bits between the ADC and DAC.

2 /to put some of the bits from the ADC in low state before writing them into the DAC.

3/ to put some of the bits from the ADC in high state before writing them into the DAC.

4/to delay the samples between the ADC and the DAC.

5/to generate AS from digital samples stored into memory.

The Eq. 6 for the minimum number of bits n is suggested in order the converter to be considered as an "ideal"

$$n>=lg(1/Emax)+D, [bit] \quad (6)$$

where lg is a logarithm in base 2 and D is a constant. In most of the cases D is chosen between 0 and 4 additional bits and depends on the application. The Eq. 6 is valid if Emax is equal to one step in the transfer characteristic of the converter.

In fact Eg 7 could be used as a quantity of information Qa which could be transferred from the analog to digital form of the signal.

$$Qa = lg (1/Emax) \quad (7)$$

X. CONCLUSIONS

Results were obtained and some of them are stated below:

1/ Theorem 1 to 4 are developed for evaluating the maximum amplitude error Eamax when sampling a SS or CS. The theorem 1 to 4 are valid for an ideal converter with infinity number of bits n (n=∞), e.g. in the case when the converters error could be neglected.

2/ It is found that SSF N=Fd/Fs=4 is guaranteeing a maximum difference between the amplitude of the "original" SS or CS and corresponding maximal digital code less than –29.3% or –3dB and this is valid for n=∞.

3/ The SSF N=Fd/Fs=2 and the frequency Fd=2*Fs (Nyquist frequency) is not very interesting. Nevertheless this is the frequency when the amplitude error Emax is changing from 0% to 100% when the phase of the SS/CS is changing from 0 do 90 deg. At this frequency the ADC is working as a "phase modulator", which normally is not his primary function. The frequency 2*Fs could be called "the frequency of full phase (or 90 deg.) to amplitude modulation".

4/ The usefulness of the new terms SSF and SHF was proven. The term SSF is giving a good idea about the error during the sampling process and about the methods of the signal reconstruction.

5/ The term SHF or Nsh is defining the ratio of enlarging the band of the AS to be converted into digital codes with one ADC with or without sample and hold circuit in from of it.
6/ The relations between the signal SSF N=Fd/Fs and the minimum number of bits n in the digital word was proven.
7/ It is suggested that the term " quantization noise" widely used in the publications is replaced with the term "error conversion function" during the SS/CS conversion or "conversion rounding function" because this error function is completely defined and determined by the characteristics of the signal and the transfer characteristics of the converter.

The method of sampling and direct signal reconstruction is described in [1]. Several practical circuits with ADC0801/2/3/4/5 and 6809 are published in [2]. The theorem of C.E. Shannon (1948) may be found in many sources, e.g.[3]. More information about the integrated circuit in the system is available from theirs manufacturers National Semiconductor Corp., Texas Instruments Inc., Analog Devices Inc. and Motorola Inc. in theirs respective catalogs [4, 5, 6, 7].

The equipment was used to evaluate the maximum amplitude, phase, frequency and function error between the "original" AS which was sampled under different conditions with different SSF N=Fd/Fs, amplitude, phase, spectrum with and without sample and hold and compared with the "digital copy". Table II is containing some of the obtained results.

TABLE II
MAXIMAL AMPLITUDE ERROR EMAX, MINIMAL NUMBER OF BITS N AND SIGNAL TO NOISE RATIO SNR FOR N FROM 2 TO 16.

N	Emax [%]	n(adc), [bit]	SNR , [dB]
2	100	0+2	1.76+12.04
3	50	1+2	7.78+12.04
4	29.3	1.77+2	12.4+12.04
5	19.1	2.39+2	16.14+12.04
6	13.4	2.9+2	19.22+12.04
7	9.9	3.33+2	21.84+12.04
8	7.61	3.72+2	24.13+12.04
9	6.09	4.05+2	26.15+12.04
10	4.89	4.32+2	27.96+12.04
11	4.05	4.63+2	29.61+12.04
12	3.40	4.86+2	31.11+12.04
13	2.91	5.1+2	32.49+12.04
14	2.51	5.32+2	33.77+12.04
15	2.18	5.52+2	34.97+12.04
16	1.92	5.7+2	36.08+12.04

It was proven t han the maximal amplitude errors during the sampling of a SS/CS depends on the SSF N=Fd/Fs. Table III is illustrating the maximal amplitude error E for the first sampled period of a SS/CS for SSF N from 2 to 16. It is clearly seen than the amplitude errors of two adjacent values (one pair and the other impair) could be quite different. Moreover for the positive and the negative period error (Epmax and Enmax) are equal for N pair and could be not equal for N impair. Concerning the direct current (DC) offset or the DC difference between the AS and the staircase approximation is minimal or zeroed when the N=4*k (k=1, 2, 3...)

TABLE III.
MAXIMAL AMPLITUDE ERRORS DURING THE FIRST PERIOD OF SS/CS, [%] FOR SAMPLING FACTOR N=FD/FS 2 TO 16

N	Amplitude errors E during the first period of SS/CS conversion with n=∞, [%]			
	Maximal	Positive and negative		Peak to peak
	Emax	Epmax	Enmax	Eppmax
2	100	100	100	100
3	50	50	0	25*
4	29.3	29.3	29.3	29.3
5	19.1	19.1	0	9.55*
6	13.4	13.4	13.4	13.4
7	9.9	9.9	0	4.95*
8	7.61	7.61	7.61	7.61
9	6.03	6.03	0	3.02*
10	4.89	4.89	4.89	4.89
11	4.05	4.05	0	2.02*
12	3.40	3.40	3.40	3.40
13	2.91	2.91	0	1.46*
14	2.51	2.51	2.51	2.51
15	2.19	2.19	0	1.09*
16	1.92	1.92	1.92	1.92

Note: (*) – With N= odd value Epp is never equal to zero. When En=0, Ep=Emax and vice versa.

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