Linear Current Starved Delay Element

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Abstract – **In this paper the instructions for preparing camera ready paper for the Conference ICEST 2005 are given. The recommended, but not limited text processor is Microsoft Word 97/2000/XP/2003. The global instructions for preparing paper with any text processor are given, too. For the LATEX users using the IEEEtran.sty is recommendable and it can be obtained from the IEEE web page http://www.ieee.org.**

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I. INTRODUCTION

Variable delay elements are inverter–based circuits used for fine, precise, and accurate pulse delay control in a high-speed digital integrated circuits. In order to achieve wide phase shift variable delay elements are realized as a chain of inverters. The chain of inverters is called delay line. In complex VLSI ICs, delay lines are constituents of DLLs (Delay Locked Loops) [1], TDCs (Time-to-Digital Converters) [4], VCOs (Voltage Controlled Oscillators) [5], Pulse-Width Control Loops (PWCLs) [3], etc.

In VLSI ICs, the DLL is routinely employed in order to obtain correct synchronization and elimination of clock skew among different digital blocks [1], such as CPU and SDRAM interface, etc. In addition, DLL is used for on-chip clock generation [1], and vernier delay patterns implemented in time-to-digital converter [4]. VCO for PLL application is realized when voltage controlled delay elements are connected in a ring [5]. Duty cycle converter (DCC) is another application, based on delay element that can independently adjust the delay of a rising/falling clock's edge [3]. In general, systems with feedback loop, which regulate pulse-width using delay elements, are referred as Pulse-Width Control Loop (PWCL). In all above–mentioned applications, variable delay elements are crucial building blocks, critical from aspect of design, since they determine precise and accurate pulse time reference.

This paper is organized as follows. Section 2 deals with an overview of existing types of voltage controlled delay elements. The modified bias circuit, with reciprocal current regulation, is described in Section 3. Hardware structure of the delay line and simulation results are considered in Section 4. Finally, Section 5 gives a conclusion.

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II. CLASSIFICATION OF DELAY LINE ELEMENTS

Variable delay line elements can be classified as digital- or voltage-controlled.

Digitally controlled delay line elements are realized as series of delay elements of variable length [7]. The number of elements in a chain determines the amount of the delay. Delay elements provide fixed and quantized time delays. These kinds of delay line elements are suitable for coarse-grain delay variation in a wide range of regulation.

Voltage controlled delay line elements, alternatively called analog voltage controlled delay line elements, are suitable for fine-grain delay variation. They are efficient in applications where small, accurate, and precise amount of delay is necessary to achieve. Usually, these types of delay lines are realized using shunt capacitor [2] or current starved delay elements [1].

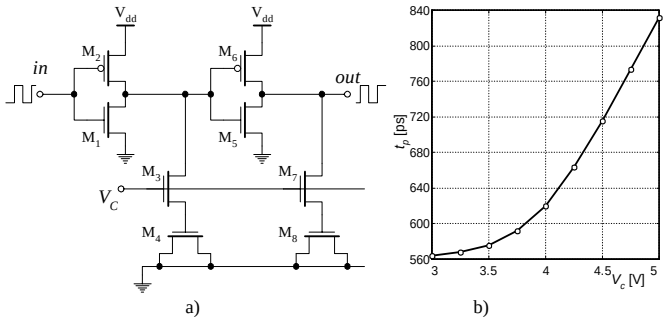

Fig.1. Shunt capacitor delay element a) scheme and b) typical characteristic delay in term of control voltage

Shunt capacitor delay element (see Fig. 1 a) is capacitive loaded inverter. In this case, the transistor (M_3 or M_7) acts as a linear resistor and defines the charging/discharging current of a load capacitor (transistor M_4 or M_8). Indirectly it changes the delay of output pulses. This type of delay element has the following disadvantages: a) the output capacitor occupies large silicon area; b) the amount of a delay and the active range of voltage regulation are small [2].

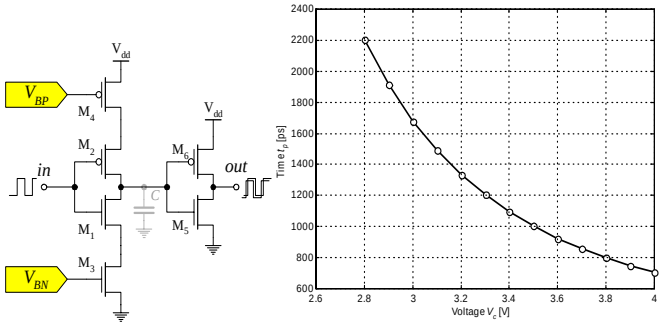

Fig. 2. Current starved delay element a) scheme and b) typical characteristic delay in term of control voltage

Current starved delay elements are implemented using current inverters (transistors M_4 and M_3 in Fig. 2 a). By controlling the charging/discharging current of the output parasitic capacitor C, we can regulate the propagation delay of this element [1].

A. Delay: Analytical model

Time delay in analog voltage controlled delay elements are defined by the following formula [6]:

$$t_{delay} = \frac{C}{I_{cp}} V_{sw} \qquad (1)$$

where: C is load output capacitance, I_{cp} corresponds to charging/discharging current of C, and V_{sw} is a clock buffer (inverter) swing voltage.

According to Eq. (1), linear delay variation, t_{delay}, is possible to achieve if either C or V_{sw} varies linearly. Let now analyze both cases:

a) **Capacitor, *C***: load capacitor can take one of the following two forms: parasitic or integrated. The parasitic capacitor depends of technological parameters (length of wiring, layout, etc.) and for a given hardware structure has constant value. Integrated capacitors can be realized as fixed and variable. MOS capacitor is usually realized with fixed value. Its value is defined by technological parameters and silicon area. Variable capacitor is realized as inversely polarized PN junction and its value dominantly depends of the inverse voltage. Its capacitance in function of inverse voltage is nonlinear. Time delay regulation, defined by Eq. (1), can be realized only with variable capacitor, by changing its inverse control voltage, V_{ctrl}, but the transfer function, $t_{delay}=F(V_{ctrl})$, will be nonlinear. We do not propose this solution.

b) **Swing voltage, V_{SW}**: it is an input voltage level at which the state at the output of the clock buffer (inverter) changes. In standard inverter's realization $V_{SW} = V_{dd}/2$, and cannot be variable. If we replace the inverter with comparator, as is described in [6], then it is possible to achieve linear regulation of the swing voltage, i.e. linear delay regulation. Critical design block of this solution [6], from aspect of high-speed operation, is a comparator. This solution meets our design goal but only for low frequency operation.

III. BIAS CIRCUIT WITH RECIPROCAL CURRENT REGULATION

The bias circuit is building block of a delay element. It determines the magnitude of current I_{cp}, defined be Eq. (1). At its input the bias circuit is driven by a single ended control voltage, V_{ctrl}, while at the outputs it generates symmetrical bias voltages, V_{BP} and V_{BN} (see Fig. 3). Directly, V_{BP} and V_{BN} provide DC operating conditions for inverter's current transistors, M_2 and M_3, while indirectly they determine the charging/discharging current, I_{cp}, of a parasitic inverter's load capacitor C_{load}.

In standard realizations [2], we have that $I_{cp}=k\cdot V_{ctrl}$, where the term k is a constant determined by a bias circuit structure. Analyzing Eq. (1), under condition that $I_{cp}=k\cdot V_{ctrl}$ is valid, we conclude that $t_{delay}=f(V_{ctrl})$ is a non-linear function. Our motivation now is to modify the structure of a standard bias circuit described in [2] in such a way that the transfer function $t_{delay}=F(V_{ctrl})$ is linear.

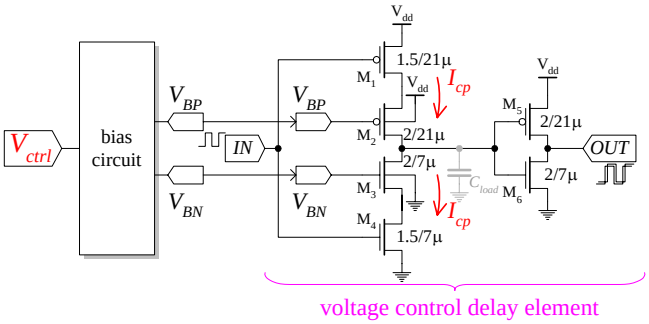

Fig. 3. Voltage control element and bias circuits

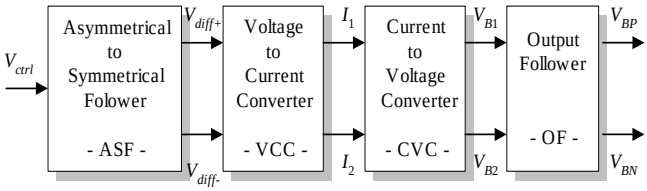

Fig. 4. Block scheme of bias circuit

Our proposal related to novel design of the bias circuit, at block schematic level, is sketched in Fig. 4. As can be seen from Fig. 4. the bias circuit is composed of four serially connected blocks. The first block in a chain, Asymmetrical-to-Symmetrical-Follower (ASF), converts the single ended control voltage V_{ctrl} into differential form represented by two output signals V_{diff+} and V_{diff-}, respectively. The second block, Voltage-to-Current-Converter (VCC), linearly converts the symmetrical input voltages, $+V_{diff}$ and $-V_{diff}$, into symmetrical outputs currents I_1 an I_2, respectively. The third block, Current-to-Voltage-Converter (CVC), converts the currents I_1 and I_2 into voltages V_{B1} and V_{B2}. The conversion process is non-linear and is based on the square route MOSFET transfer function [8]. Finally, the last block in a chain called Output-Follower (OF) converts the asymmetrical input voltage V_{B1} into two voltages V_{BP} and V_{BN}. These output voltages are used for polarization of the delay element stage (see Fig. 3).

Structures of blocks VCC, CVC and OF, at transistor level, are pictured in Fig. 5. Transistors M_{B1} (M_{B2}), M_{B3} (M_{B4}) and M_{B5} (M_{B6}) are constituents of VCC and form a band-gap current source I_0' (I_0")=12.5µA. Transistors M_{D1} and M_{D2} are parts of the VCC's differential input stage. Output currents I_1 and I_2, are defined by the following relations

$$I_1 = I_0^{'} + \frac{V_{diff}}{R} \quad \text{and} \quad I_2 = I_0^{''} - \frac{V_{diff}}{R} \qquad (2)$$

where R is a resistor connected between sources of transistors M_{D1} and M_{D2}, and $V_{diff} = V_{diff+} - V_{diff-}$. According to Eq. (2), we conclude that a linear dependence exists between the input voltage V_{diff} and output currents I_1 and I_2, respectively.

Transistors M_{A1} and M_{A2} are parts of CVC, and act as active load resistors. The CVC's output voltages V_{B1} and V_{B2} are defined as

$$V_{B1} = \sqrt{\frac{I_1}{k_n}} + V_{tn} \quad \text{and} \quad V_{B2} = \sqrt{\frac{I_2}{k_n}} + V_{tn} \qquad (3)$$

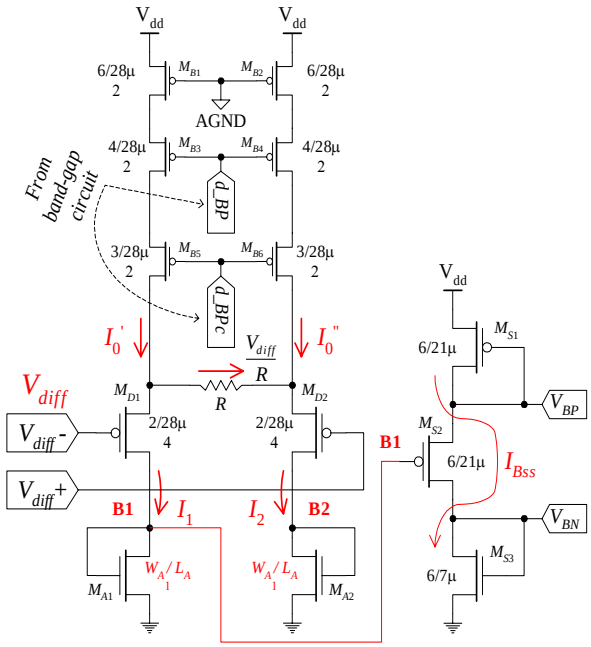

Fig. 5. Scheme of a bias circuit

The voltage V_{B1} drives the stage OF. At the outputs of OF two voltages, V_{BP} and V_{BN}, that are used for polarization of current starved delay elements, are generated.

The current I_{Bss} through transistors M_{s1}, M_{s2} and M_{s3}, see Fig. 5, is defined by the following formulas

$$I_{Bss} = k_p\left(V_{dd} - V_{BP} - V_{tp}\right)^2 \tag{4}$$

$$I_{Bss} = k_p\left(V_{BP} - V_{B1} - V_{tp}\right)^2 \tag{5}$$

from Eq. (4) we obtain

$$V_{BP} = V_{dd} - V_{tp} - \sqrt{\frac{I_{Bss}}{k_p}} \tag{6}$$

after substituting Eqs. (6) into (5) on obtain

$$I_{cp} = k_p\left(V_{dd} - 2V_{tp} - \sqrt{\frac{I_{cp}}{k_p}} - V_{B1}\right)^2 \tag{7}$$

where I_{Bss} is equal to I_{cp} since the composition of bias stage OF and a delay element forms two pairs of current mirrors (transistors M_{s1} (M_{s3}) and M_2 (M_3)) sketched in Fig. 5. By rearranging Eq. (7) we obtain

$$I_{cp} = \frac{k_p}{4}\left(V_{dd} - 2V_{tp} - V_{B1}\right)^2 \tag{8}$$

Finally, if we substitute V_{B1} from Eq. (3) we have

$$I_{cp} = \frac{k_p}{4}\left(V_{dd} - 2V_{tp} - V_{tn} - \sqrt{\frac{I_1}{k_n}}\right)^2 \tag{9}$$

Eq. (9) can be represented in the following form

$$I_{cp} = A + B\cdot\sqrt{I_1} + C\cdot I_1 \tag{10}$$

where constants A, B and C are equal to

$$A = \frac{k_p}{4}\left(V_{dd} - 2V_{tp} - V_{tn}\right)^2,\quad B = -\frac{k_p}{4}\frac{2\left(V_{dd} - 2V_{tp} - V_{tn}\right)}{\sqrt{k_n}},\quad C = \frac{1}{4}\cdot\frac{k_p}{k_n}.$$

Let note that Eq. (10) approximates a reciprocal relation between the current I_{cp} and control voltage V_{diff}.

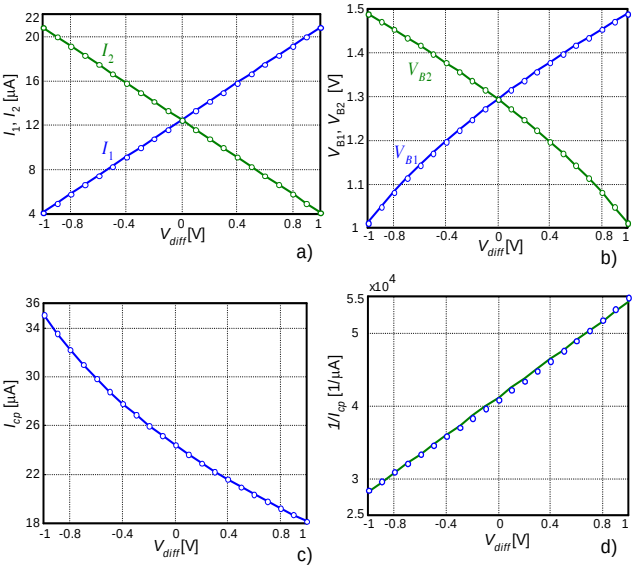

Fig. 6. Dependencies among output currents and input voltages of a bias circuit given in Fig. 5. according to the analytical model

In order to test the derived the analytical model, we will use the following technological and operating parameters for 1.2 µm CMOS technology:

C_{ox}=1.41e-3 F/m^2; μ_p=195E-4 m^2/V*s; μ_n=555E-4 m^2/V*s;
k_n=0.5*78.255 µA/V^2; k_p=0.5*27.495 µA/V^2;
V_{tn}=0.6259V; V_{tp}=1.14V; I_0=12.5µA; R=120kΩ; V_{dd}=5V;

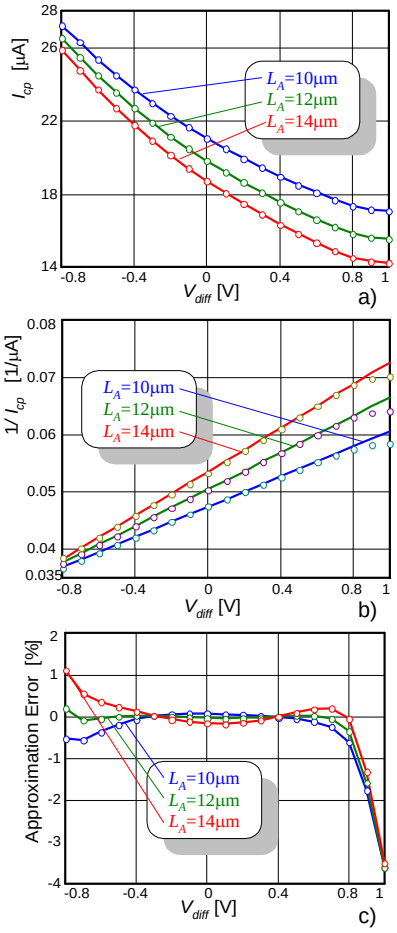

Fig. 7. HSpice simulation of biacircuits

By using the proposed analytical model, dependencies of currents (I_1, I_2 and I_{cp}) and voltages (V_{B1} and V_{B2}) in a bias circuit are calculated by a program Matlab in four steps (see Fig 6. According to Fig. 6 c) and d) we can conclude that the approximation is possible within a range I_{cp_max}:I_{cp_min} =36μA:18μA=2:1.

The design of bias circuit is verified using HSpice simulation. During simulation are used models of level 47 that correspond to 1.2μm double-metal double-poly CMOS technology. As simulation's parameter the channel length, L_A, of NMOS transistors, M_{A1} and M_{A2}, was used. Let note that M_{A1} and M_{A2} represent active loads for the CVC block. Active load NMOS transistors channel length L_A, of transitors M_{A1} and M_{A2}, defines the parameter $k_n=(\mu_n C_{ox}/2)*(W_A/L_A)$ in Eq. (10). During simulations, three different L_A values that correspond to 10, 12 and 14 μm, for supply voltage V_{dd}=5V and temperature T=27°C as constants, were used. The obtained simulation results are presented in Fig. 7.

As a conclusion, HSpice simulation of a bias circuit confirms that between the delay elements charge current I_{cp} and the control voltage V_{diff} a reciprocal relation exists. Relative approximation error is less then 1%, when the control voltage is in a range of ±0.8V.

IV. Current Starved Delay Line with Linear Delay Regulation

Our proposal concerning realization of the delay line consists of four delay element stages (see Fig. 8). As can be seen from Fig. 8, each stage is composed of voltage controlled delay element, VCDE$_i$, and an output buffer, OB$_i$, i = 1,..,4. VCDEs are of standard current starved delay elements sketched in Fig. 4, while OBs are realized with two large inverters connected in cascode. According to Fig. 8, the bias circuit is constituent of the delay line.

HSpice simulations results that relate to the delay line are presented in Fig 10. Models of level 47, for 1.2μm CMOS technology, during simulation, were used.

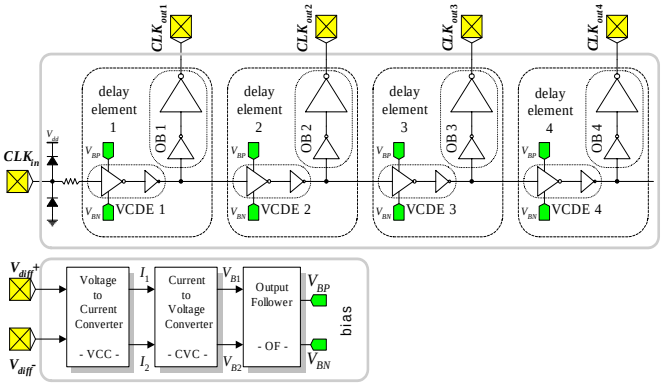

Fig. 8. Four stage delay line block scheme

During simulation, dimensions of bias circuit's active load transistors were selected to be W_A/L_A=14μm/14μm, the supply voltage was V_{dd}=5V and temperature T=27°C. Simulation results concerning delay line characteristics, for both leading and trailing clock edges, in term of control voltage, are pictured in Fig. 9 a). The appropriate absolute value of non-linearity error, in function of the control voltage, is given in Fig. 9 b). The delay line is operative within the frequency range from 20 to 33MHz. According to the obtained results, (see Fig. 9 b) we see that the linearity error is less then 500ps when the control voltage varies in the range of ±0.8V.

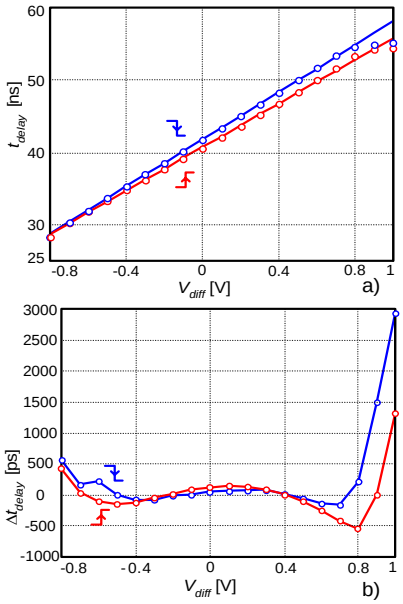

Fig. 9. HSpice simulation of time delay t_{delay} in term of control voltage V_{diff}

V. Conclusion

In this paper, we describe an implementation of a linear voltage controlled delay line. The delay line is constituent of the DLL circuit. HSpice simulation results points to the fact that for 1.2μm CMOS technology high delay linearity (< 500 ps) within the full range of regulation (from 30 to 60 ns) is achieved.

References

[1] Y.Moon, et al., "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance", *IEEE JSSC*, vol.35, No. 3, pp. 377-384, March 2000.

[2] M. Maymandi-Nejad, M. Sachdev, "A digitally Programmable Delay Element: Design and Analysis", *IEEE Trans. on VLSI Systems*, vol. 11, No. 5, October 2003.

[3] M. Fenghao, C. Svensson, "Pulsewidth Control Loop in High-Speed CMOS Clock Buffers", *IEEE JSSC*, vol. 35, No. 2, pp. 134-141, February 2000.

[4] P. Dudeck et al., "A high–resolution CMOS time–to–digital converter utilizing a vernier delay line", *IEEE JSSC*, vol. 35, No. 2, pp. 240–246, February 2000.

[5] J. Chiang and K. Chen, "The Design of an All-Digital Phase-Locked Loop with Small DCO Hardware and Fast Phase Lock", *IEEE Trans. on CAS–II*, vol. 46, No. 7, pp. 945-950, July 1999.

[6] G. Jovanović, M. Stojčev, "Voltage Controlled Delay Line for Digital Signal", *Facta Universitatis, Series: Electronics and Energetic*, vol. 16. No. 2, pp. 215-232, August 2003.

[7] A. Hatakeyama, et al., "A 256-Mb SDRAM Using a Register-Controlled Digital DLL", IEEE JSSC, vol. 32, No. 11, 1997.

[8] K. Bult, H.Wallinga, "A Class of Analog CMOS Circuits Based on the Square-Law Characteristic of an MOS Transistor in Saturation", IEEE JSSC, vol. 22, No.3, pp. 357-365, June 1987