A Behavior Macromodel of Closed-Loop Sample-and-Hold Amplifier with Active Integrator

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Abstract – **In this paper is proposed a behavior SPICE macromodel of Sample-and-Hold Amplifiers (SHAs) using closed-loop architecture. The circuit model is developed applying basic macromodeling technique: simplification and build-up. Computer models of linear dependent and independent voltage and current sources in the equivalent circuit are incorporated. The macromodel topologies comprise of three stages: input transconductance amplifier, low-leakage switch and output active integrator with hold capacitor. The model proposed here represents the full functional and logical behavior of the real devices. It reflects the two modes of operation (sample mode and hold mode) and the two transition between the modes (sample-to-hold and hold-to-sample) and the corresponding parameters: offset voltage and current, input resistance and capacitance, CMRR, acquisition time, slew rate, droop rate, etc. To confirm the validity of the SHA model, simulation results are compared with the data sheet parameters of the IC, where is found good agreement between simulations and performance of the actual devices.**

Keywords – **Sample-and-Hold, Behavior Modeling, Circuit simulations, SPICE, Verification.**

I. INTRODUCTION

The sample-and-hold function is one which is basic to the data acquisition and data distribution systems. Since the most leading companies of such type of analog circuits usually do not publish corresponding computer library models it is useful to have on one's disposed a macromodel of a concrete selected IC for preliminary analyses in the design process.

The SPICE simulator is actually the standard ECAD tool for the IC design. It contains intrinsic models for the most of the IC devices that give a good accuracy for the purely electrical simulations within the device safe operating area.

There are exits four methods to improve the accuracy of the SPICE models: the structural macromodeling, the C code modeling, AHDL modeling and Analog Behavior Macromodeling (ABM) [5]. In [2] a VHDL-AMS SHA macromodel is presented, which reflect the basic functionality and model some of the second-order effects of the real ICs. The drawbacks are the leak of portability to the SPICE like simulators. In [3] a structural macromodel of closed-loop sample-and-hold circuit is presented. This model allows one to simulate arbitrary user circuits with respect to the behavior in both the time and frequency domains including error parameters and the temperature dependence of several parameters. The main disadvantage of the structural macromodeling is the complexity of the equivalent circuit and the difficulty of obtaining all model parameters. This method is mainly used modeling the parasitic elements of an IC device.

The last generation of SPICE simulators has introduced a new and powerful modeling technique ABM that contains in building a sub-circuit description of the device, using linear and nonlinear voltage and current sources to implement the device's internal static and dynamic equations. The main advantages of the ABM method are the portability to all SPICE simulators and also the user's access to the macromodel's internal equations and variables.

In this paper is presented a behavior macromodel of closed-loop SHA, which can adequately represent the main electrical performances of the real ICs. Since the most manufactures of the SHAs usually do not publish information for the internal structure it is useful to develop equivalent circuit with behavior models from standard ABM SPICE compatible library. As well to keep the universality of the proposed macromodel some of the specific effects and elements of the actual ICs, which have not essential influence over the functionality (for example temperature dependence of the parameters, noise, internal feedback resistors, etc) are not presented in the equivalent circuit.

II. MACROMODEL DEVELOPMENT

The macromodel of a SHA is developed using the analog bloc modeling method introduced in [2]. This method is based on a Top-Down analysis approach and applying simplification and build-up macromodeling technique.

An interesting model structure is a closed-loop sample-and-hold amplifier with active integrator, as shown in Fig. 1 [1]. This architecture with a suitable choice of parameters and elements accurately represents a broad class of IC SHAs.

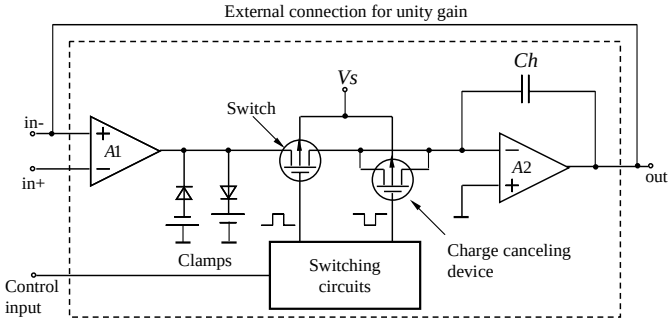

Fig. 1. Closed-loop Sample-and-Hold architecture.

The sample-and-hold ideal behavior macromodel is so defined using ideal internal elements and provides an ideal sample-hold behavior. In developing SHA model the transconductance amplifier A1 and output op amp A2 are

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replaced with ideal voltage controlled sources. For convenience, the transconductance of the amplifier A1 is selected to be less than unity and the value of A2 is chosen to be greater than unity. The analog FET switch and clamp diodes are replaced with ideal voltage controlled switches. The input and output waveforms of the ideal model predicted by OrCAD PSpice are shown in Fig. 2.

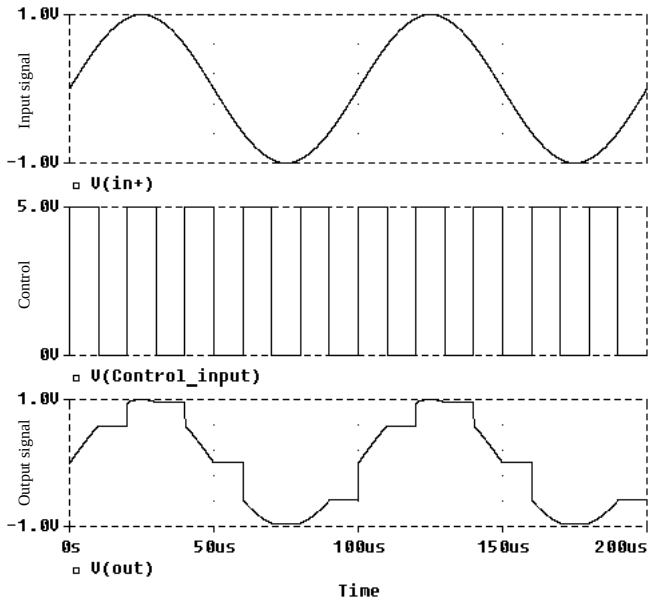

Fig. 2. Sample-and-Hold (S/H) Waveforms Showing the Input Sampled (Top), the S/H Control (Middle), and the S/H Output (Bottom)

However, ideal model not present several second-order effects, such as acquisition time, slew rate, feedthrough, etc. In response of these needs is developed improved macromodel with additional internal components. The equivalent circuit of this model is shown in Fig. 3, where the different elements are presented as hierarchical blocs.

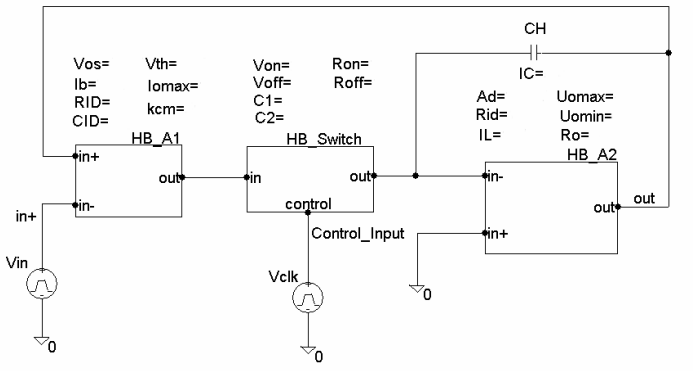

Fig. 3. Circuit diagram of the SHA macromodel.

The circuit of Fig. 3 is subdivided into tree stages: input stage – HB_A1, switch drive circuit (second stage) – HB_Switch, and output stage (third stage) – HB_A2. *The input stage*, shown in Fig. 4a consists of linear voltage controlled current source G1, passive elements and additional dependent and independent sources. This stage provides the necessary linear and nonlinear differential mode (DM) and common-mode (CM) input characteristics. The DM transconductance gain is provided by the elements consisting of maximum output current I_{omax} and threshold voltage *Uth* defined in the TABLE parameter of G1. The differential voltage gain is

$$A_{G1} = \frac{Io\,max}{Uth} \approx \frac{CH}{t_s(\varepsilon)} ln\left(\frac{1}{\varepsilon}\right), \quad (1)$$

where *CH* is the hold capacitance, $t_s(\varepsilon)$ is the settling (acquisition) time and ε is the error when settling occurs (for example 0,01 or 0,1 percent from the output voltage) [7].

The CM gain is produced by the elements *Gcm1*, *Gcm2*, *Ecm* and *Rcm*. Empirically, a value of *Rcm* is chosen equal to 1kΩ. The current sources *Gcm1* and *Gcm2* are chosen linear one-port generators having the following equations:

$$I_{G_{cm1}} = k_{cm} U(in+,0), \quad (2a)$$

$$I_{G_{cm2}} = k_{cm} U(in-,0), \quad (2b)$$

where $U(in+,0) = U(in-,0) = U_{cm}$ is the input common-mode voltage. The current thus generated $I_{G_{cm1}}$ and $I_{G_{cm2}}$, will flow through the resistor R_{cm}, towards the internal ground. In such a way the voltage $U(2,0) = (I_{G_{cm1}} + I_{G_{cm2}}) R_{cm} = 2k_{cm} U_{cm}$ will

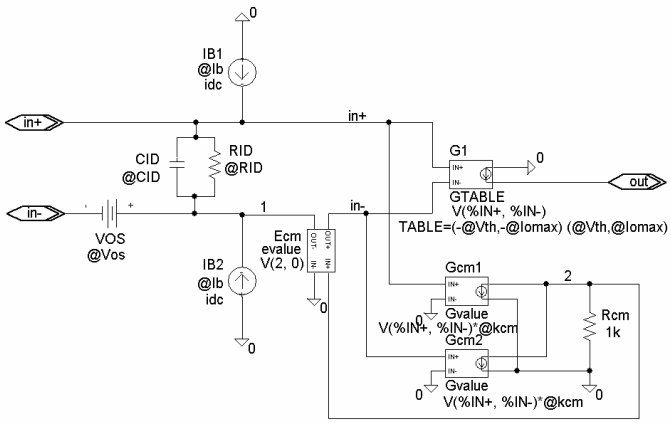

Fig. 4a. Equivalent circuit of the input stage (HB_A1).

depend upon the amplitude of the common-mode input voltage. The voltages generated at node 2 are used for forming the equation of input voltage-controlled voltage source E_{cm} as follows:

$$U_{E_{cm}} = k_{1,E_{cm}} U(2,0). \quad (3)$$

For convenience, the coefficient $k_{1,E_{cm}}$ of the polynomial source E_{cm} is selected equal to unity. Then the output current of the stage, predicted by the input common-mode voltage is

$$I_{out} = 2A_{G1} U_{Ecm} = 2A_{G1} k_{cm} R_{cm} U_{cm}. \quad (4)$$

The CM gain can be found with the following equation:

$$A_{cm} = \frac{I_{out}}{U_{cm}} = 2A_{G1} k_{cm} R_{cm}. \quad (5)$$

The CM rejection ratio (*CMRR*) is the ratio of the DM gain and CM gain [7], i.e.

$$CMRR = \frac{A_{G1}}{A_{cm}} = \frac{1}{2k_{cm} R_{cm}}. \quad (6)$$

The elements *RID* and *CID* produces the input resistance and capacitance. Offset voltage is modeled with the

combination of an ideal voltage source VOS and an initial condition voltage (*IC*) of the hold capacitor, while input bias/offset currents are modeled by properly setting the currents on the input sources *IB1* and *IB2*. The slew rate of the proposed macromodel is determined by the charging of the holding capacitor CH with the output current of source G1. The slew rate is given by

$$SR = Iomax/CH\ , \tag{7}$$

where *SR* is the slew rate of the SHA model in the sample mode. According to Eq. (1) the maximum output current of G1 is

$$Iomax = A_{G1}Uth\ . \tag{8}$$

Substituting into (7) gives

$$SR = \left(A_{G1}Uth\right)/CH\ . \tag{9}$$

The second stage (Fig. 4b) uses a two ideal voltage controlled switches S1 and S2 and several passive elements. In the sample mode S1 is closed and S2 is open, current source G1 provides charging current to the holding capacitor *CH*. When the S1 is open and S2 is closed, the circuit is in the hold mode

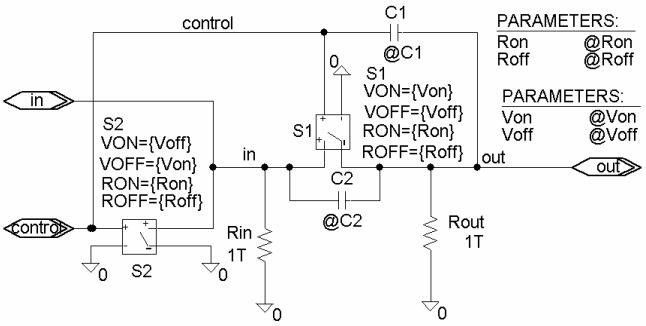

Fig. 4b. Equivalent circuit of the second stage (HB_Switch).

with the capacitor holding the value of the input voltage which was present at the instant the S1 was opened. Sample-and-hold offset is modeled with the capacitor C1, and the capacitor C2 produces the frequency dependence of the feedthrough attenuation ratio [4]. In the transition from sample mode to hold mode, the turn-off of the sampling switch S1 results in charge injection effects into C1 that introduce a sample-to-hold offset (jump) error ΔU_{SH} , which is dependent on the total clock voltage variation ΔU_C according to

$$\Delta U_{SH} = \Delta U_C.\left(C1/CH\right). \tag{10}$$

During the hold mode (S1 is turn off) there also is some penetration of the input ac signals through the capacitor *C*2. The feedthrough attenuation ratio (*FA*) of the macromodel can be calculated with

$$FA \approx 20lg\left(CH/C2\right). \tag{11}$$

The resistance in a sample and hold mode of the switch circuit are modeled with parameters *Ron* and *Roff*. The parameters *Von* and *Voff* provide the threshold voltages during the transitions between the modes of operations. The parameters *Ron, Roff, Von* and *Voff* of the switches S1 and S2 are defined in the equivalent circuit with additional elements 'param' (Special.lib). *The output stage* (Fig. 4c) provides the proper output resistance, operating voltage range of the SHA, etc. Droop rate is the rate at which the output voltage is changing due to the leakage from the hold capacitor. In the proposed macromodel the droop rate is presented with the combination of the I_{iB}^{+} , I_{iB}^{-} and *Rid*. The rate of voltage change is

$$DroopRate = I_L / CH\ . \tag{12}$$

The parameters U_{omax} and U_{omin} of the voltage source *Eo* produce the desired maximum voltage excursion. The output voltage range at higher frequencies is limited by the slew rate. The maximum output voltage range is given by

$$Uomax = \left|Uomin\right| = SR/\left(2\pi f\right), \tag{13}$$

where f is the power bandwidth. The input and output resistance of the stage is modeled with resistors R_{id} and R_o .

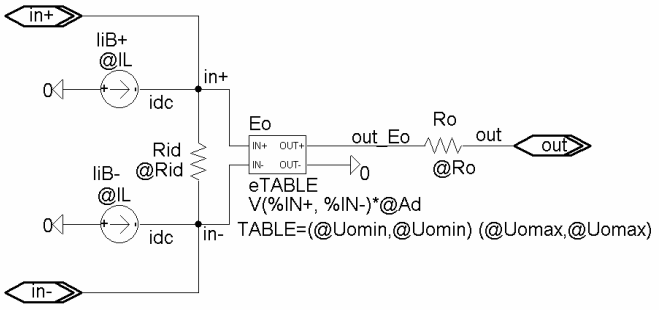

Fig. 4c. Equivalent circuit of the output stage (HB_A2).

III. Design Procedure

The design method of the SHA macromodel suggested in this section can be split into two basic steps. The first step consists of the model parameters selection using typical values of the IC data sheet.

TABLE I
DESIGN EQUATIONS FOR THE SHA MACROMODEL

$CH = C_h$	$V_{off} = V_{off-LowVoltage}$
$A_{G1} = \frac{CH}{t_s(\varepsilon)} ln\left(\frac{1}{\varepsilon}\right)$	$Ron = 1\Omega\ ,\ Roff = 1.10^{12}\,\Omega$
$U_{th} = \frac{CH}{A_{G1}} SR$	$C1 = CH\,\frac{\Delta U_{SH}}{\Delta U_C}$
$I_{omax} = SR.CH$	$C2 = 10^3 (CH/10^{\frac{FA}{20}})$
$k_{cm} = 1/(2R_{cm}CMRR)$	$A_d = A_{d-OpAmp}$
$VOS = IC(CH) =$ $= V_{OS\_OffsetVoltage}$	$R_{id} = R_{id-OpAmp}$
$I_b = I_{iB}$	$I_L = CH.(DroopRate)$
$RID = R_{id}$	$U_{omax} = U_{out}^{+}$
$CID = C_{id}$	$U_{omin} = U_{out}^{-}$
$V_{on} = V_{on-HighVoltage}$	$R_o = R_{o-dc}$

Expressions are developed to relate the performance of the SHA and the macromodel to the parameters and elements of

the macromodel. A summery of all design equations is presented in Table I. The determination of the element values of the macromodel proceeds from the input, transfer, and output characteristics of the SHA.

The second step of the proposed design method is macromodel verification and validation. The purpose of verification is to guarantee the correct behavior of each element or group of elements in the model. Verification is effectively a '*micro*' check of the model. During the verification process each element is tested in turn to ensure that, 1) they behave in the manner intended by the model code and, 2) that their behavior is representative in the real world. A valid model is both accurate and able to meet the objectives of the simulation project for witch it is being used. The purpose of validation is to guarantee the correct degree of accuracy by checking that the overall behavior of the model is representative in the real world. Model validation can be seen as a '*macro*' check of the simulation. During the validation it is particularly important to compare the performance of the model against the real system. For the goals of validation it is necessary to collect data that represents the average behavior of the real device [4].

IV. THE AD585 MACROMODEL

In this section, a numerical example is used to illustrate the development of the parameters of the SHA macromodel. For the example, the electrical characteristics and parameters of the AD585 closed-loop SHA are used [6]. The AD585 is a complete monolithic sample-and-hold circuit consisting of transconductance input amplifier in series with low leakage analog switch and JFET input integrating amplifier (Fig. 1). In fact AD585 is typical representative of the closed-loop topology using the most contemporary SHAs implementation.

The development procedure follows the sequence of expressions of Table I. The final results are presented in Table II.

TABLE II
MACROMODEL PARAMETERS

$CH = 100\,pF$	$V_{on} = 2V$
$A_{G1} = 307\mu S$	$V_{off} = 0{,}8V$
$U_{th} = 3{,}257V$	$C1 = 60\,fF$
$I_{omax} = 1mA$	$C2 = 7{,}5\,pF$
$k_{cm} = 50nS$	$A_d = 200.10^3$
$R_{cm} = 1k\Omega$	$R_{id} = 1T\Omega$
$VOS = IC(CH) = 5mV$	$I_L = 100\,pA$
$I_b = 2nA$	$U_{omax} = 10{,}8V$
$RID = 1T\Omega$	$U_{omin} = 10{,}8V$
$CID = 10\,pF$	$R_o = 1k\Omega$

Validation checks have been performed on the SHA macromodel developed through simulation modeling of the four modes of operation of the real device. In Table III is given comparison between macromodel parameters and data sheet parameters. Notice that the average error is not higher than 3%, which guarantee the correct degree of accuracy.

TABLE III
SHA PERFORMANCE CHARACTERISTICS

Parameter	Conditions	AD585 Macromodel	AD585 Data Sheet
Sample/Hold mode parameters			
Acquisition time	10V Step to 0,01%	3,19μs	3μs
Droop Rate	A=+1	1,001V/s	1V/s
Sample-to-Hold Offset	A=+1	2,93mV	3mV
Feedthrough	$20V_{p\text{-}p}$, 10kHz	0,51mV	0,5mV
Transfer parameters			
Open-Loop Gain	$20V_{p\text{-}p}$, A=+1	200,000	200,000
Common-Mode Rejection	V_{cm}=10V	80dB	80dB
Full Power Bandwidth	V_o=$20V_{p\text{-}p}$	159kHz	160kHz
Slew Rate	V_o=$20V_{p\text{-}p}$	9,84V/μs	10V/μs
Operating Voltage Range	-	10,8V	10,8V
Analog input parameters			
Offset voltage	-	5mV	5mV
Bias Current	-	2nA	2nA
Input Capacitance	f=1MHz	10pF	10pF
Input Resistance	V_o=$20V_{p\text{-}p}$	10TΩ	10TΩ
Digital input parameters			
Logic Low Voltage	-	0,8V	0,8V
Logic High Voltage	-	2V	2V

VI. CONCLUSIONS

In this paper, a behavior SPICE macromodel of a closed-loop SHAs has been presented. The proposed model accurately predicts the circuit behavior for nonlinear dc, ac, and large-signal transient responses. The macromodel is implemented as a hierarchical blocks and the structure of their netlist confirm to the standard SPICE format.

REFERENCES

[1] K. R. Stafford, P. R. Blanchard, "A Complete Monolithic Sample/Hold Amplifier," *IEEE J. Solid-State Circuits*, vol. 9, pp. 381-387, Dec. 1974.

[2] M. Cousineau, D. Stadarovski, M. Lescure, "Analog Circuit Modelling Method – Sample-and-Hold Development," *MIXDES 2003*, Poland, June 2003.

[3] U. Jörges, G. Jummel, G. Müller, M. Reinhold, "A Macromodel of Sample-and-Hold Circuits," *International J. of Circuit Theory and Applications*, vol. 25, pp. 483-502, Dec. 1998.

[4] E. D. Shoikova, I. M. Pandiev, "Commercial Sample/ Track-and-Hold Amplifier Macromodel Development," *ET'2003*, book 3, pp. 84-90, Bulgaria, September 2003.

[5] D. Andreu, D. Stepan, S. Josse, "Introduction to Behavioural Modelling and PLL Behavioural Modelling," *Newsletter www.spice-club.com*, 09/2001.

[6] AD585 High Speed, Precision SHA – Data sheet, *Norwood, Mass., Analog Devices*, 2003.

[7] K. Laker, W. Sansen, "*Design of Analog Integrated Circuits and Systems*," McGraw-Hill, 1994.