Statistical Optimization of Frequency Converter for Radiocommunication System

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Abstract - **The paper presents a specific methodology for a statistical optimization of a frequency converter in radiocommunication systems. The study is performed in the environment ORCAD/PSPICE 9.2. and IESD. Optimization steps and results from circuit simulations are presented. In order to implement the circuit for different channel conversions a parametric range for a set of sensible parameters is determined nominally and statistically.**

Keywords - **statistical optimization; frequency converter;**

I. Introduction

The paper continues the research on the development of specific methodologies for statistical optimization of different types of circuits for radiocommunication applications, presented in previous papers [2,3,6]. These papers develop the methodology for statistical optimization with IESD simulator described in [4,5] and improves existing methods as for example [9].

A specific methodology for statistical optimization of a frequency converter for radiocommunication system is proposed. The frequency converter permits to transmit TV signal from channels IV and V through S-channels for cable TV or to exploit TV retranslators of VHF range (I and II TV channels) on areas with cut relief where UHF signals are transmitted with big losses.

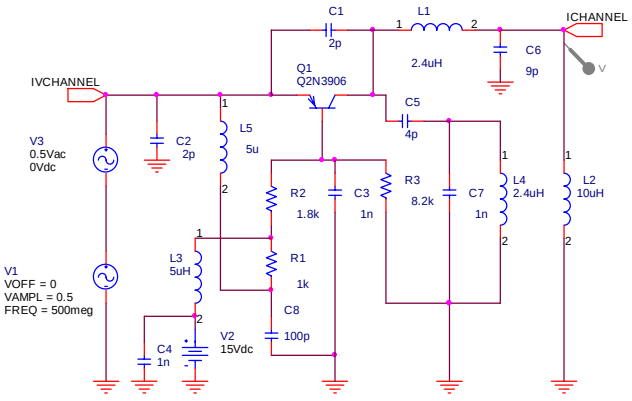

Figure 1. Frequency converter from 500MHz to 50MHz

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Figure 1 presents the circuit of a frequency converter from [1] which permits the conversion from UHF range (TV channel IV - 500MHz) in VHF range (TV channel I - 50MHz). A table is given in the paper for the necessary variations of a set of circuit element values in order to cover the different conversion options.

II. Steps of the Specific Methodology for Optimization of the Frequency Converter

The specific methodology for the statistical optimization of the frequency converter has the following steps:

- Specification and constraints definition;
- Nominal analysis and estimation for the conversion between two TV channels;
- Statistical analysis of the frequency converter in ORCAD/Pspice 9.2 and IESD;
- Definition of the Goal function for statistical optimization;
- Statistical optimization of the frequency converter through optimal tolerancing;
- Implementation of the frequency converter for different channel conversions.

The specific methodology steps are described in details..

III. Description of the Specific Methodology Steps for the Statistical Optimization of the Frequency Converter

A. *Specification and constraints definition*

The specification of the frequency converter is to convert the channels IV and V into channels I, II and S-channels [see 8]:

f (Vout, f(Vin)=500MHz) ∈{50MHz;175.25MHz; 182.25MHz; 189.25MHz; 196.25MHz; 203.25MHz; 217.25MHz; 224.25MHz}

f (Vout, f(Vin)=800MHz) ∈ {80MHz;175.25MHz; 182.25MHz; 189.25MHz; 196.25MHz; 203.25MHz; 217.25MHz; 224.25MHz},

where Vin and Vout are the input and output voltages of the frequency converter and f is frequency.

The constraints for the frequency converter are defined from the standards of Bulgarian telecommunications Company from [7]:

f(Vout)±5%, THD(Vout)<20%, SNR(f(Vout))>40dB,

where THD is the coefficient of total harmonic distortion when a sinusoidal signal is applied to the input and SNR is the signal to noise ratio.

B. Nominal analysis and estimation of the frequency converter

Figure 2 presents the results for the output voltage and the SNR from simulation of the frequency converter from figure 1 in frequency area with AC and NOISE analysis in ORCAD/PSPICE. The value for SNR in the output is:

SNR (50MHz)=109dB.

Figure 3 presents the results from the simulation in Time area for the input and output voltages of the frequency converter. The input voltage is sinusoidal with 500MHz frequency. The output voltage is sinusoidal with 50MHz frequency. A Fourier analysis is performed in order to estimate the total harmonic distortion of the output signal. The value of the THD is: THD(Vout) = 4.54%.

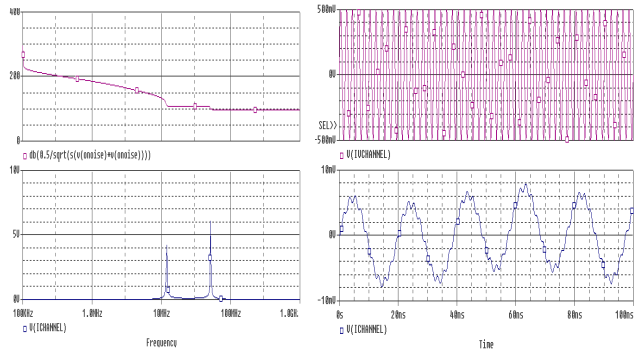

Figure 2. Gain and SNR from AC simulation in ORCAD/PSPICE

Figure 3.Input and output voltage converting 500MHz to 50MHz from Time area simulation in ORCAD/PSPICE

C. Statistical analysis of the frequency converter

The statistical analysis of the frequency converter is performed in ORCAD 9.2 and IESD simulators. The tolerances of all R,C,L elements in the circuit from figure 1 are 10%. Figure 4 presents the results for the output voltage of the frequency converter from Monte Carlo simulation with 100 runs in time domain. The histogram of output voltage period is built by the PSPICE option PERFORMANCE ANALYSIS, defined as:

XatNthY(V(ICHANNEL),0,2)

Figure 5 presents the results for the output voltage and the SNR of the frequency converter from a Monte Carlo simulation with 100 runs in frequency domain (AC sweep). A histogram is determined for the SNR value at the output for 50MHz. A Fourier analysis is performet at any MC run and the values of the THD coefficients are detrmined at any run. Statistical processing is performed with the simulator IESD for the circuit parameters determined from the 100 MC runs. Figure 6a presents the histograms of the THD coefficient and of the frequency values for the output voltage. Figure 6b presents the correlation between the THD and the frequency of the output voltage in the frequency converter. The value of the linear correlation coefficient r is:

R(THD(Vout), f(Vout))=0.9195

There is a strong linear correlation between the output voltage frequency and the output voltage total harmonic distortion in the frequency converter from figure 1.

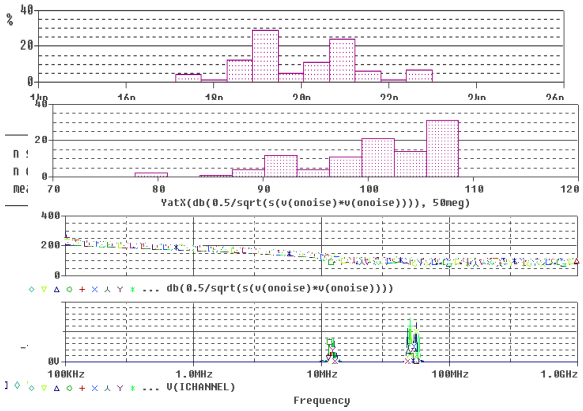

Figure 4. Statistical simulation in time area for the outcome voltage with 10% tolerances for all R,L,C elements

Histogram for the period of the outcome voltage

Figure 5. Statistical simulation with AC sweep for the outcome voltage and the SNR. Histogram of the SNR(50MHz)

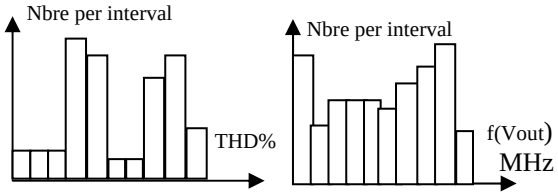

Figure 6a. Histograms of the output voltage frequency and total harmonic distortion built in the IESD simulator

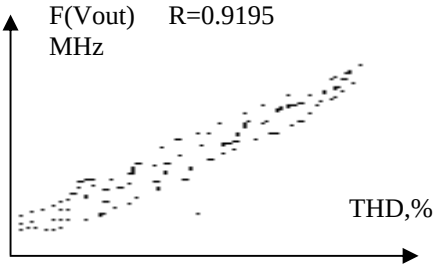

Figure 6b. Statistical correlation between the outcome voltage frequency and the total harmonic distortion estimated from IESD simulator

D. Definition of the Goal function for statistical optimization

Taking in consideration the results from the statistical analysis of the frequency converter described in previous paragraph, the statistical optimization task is defined as follows:

- The objective is to perform optimal tolerancing for the circuit from figure 1 with 100% Yield following the constraints defined in point A.
- Tolerancing is performed for the R,L,C elements.

The goal function for statistical optimization of the frequency converter is to determine the maximal tolerance values for all R,L,C elements in the circuit which guarantee

100% Yield (0% Fail) following the constraints for the output voltage: frequency f(Vout)=50MHz±5%, total harmonic distortion TDH(Vout)<20% and signal to noise ratio SNR<40dB. The goal function is formulated as follows:

Max tol{Ci, i=1,8, Lj, j=1,5; Rk, k=1,3}, f(Vout,f(Vin)=500MHz)=50MHz±5%, THD(Vout)<20%, SNR(Vout)>40dB}, Yield=100%, Fail=0%

E. Statistical optimization of the frequency converter

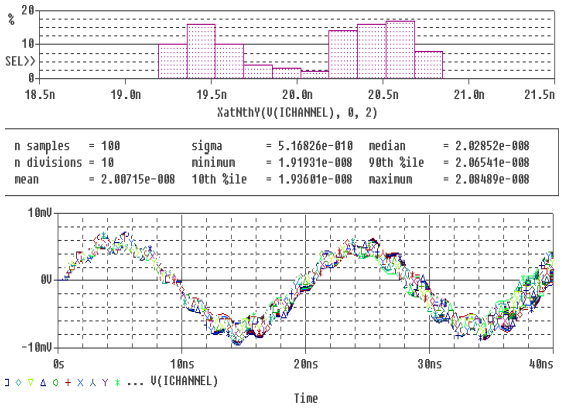

Figure7. Statistical simulation in time area for the outcome voltage of the statistically optimized frequency converter. Histogram for the period of the outcome voltage

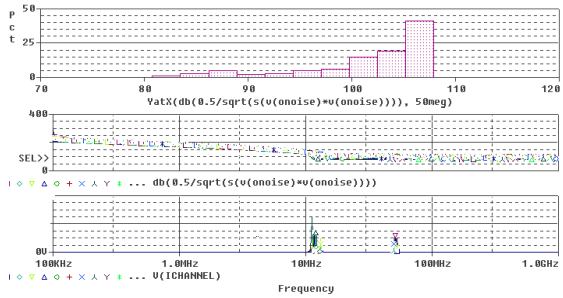

Figure 8. Statistical simulation with AC sweep for the outcome voltage and the SNR of the statistically optimized frequency converter. Histogram of the SNR(50MHz)

The statistical optimization which consists in optimal tolerancing is realized in IESD and ORCAD 9.2 environment. The initial values for the tolerances of all R,L,C elements in the circuit are 10%. Monte Carlo simulations in time and frequency areas are realized with 100 runs each. The values for the parameters f(Vout) - frequency of the output voltage, T(Vout) - period of the output voltage, k=f(Vout)/f(Vin) - frequency conversion coefficient, SNR (Vout,50MHz) - signal to noise ratio at 50MHz are extracted at any run. The Yield and Fail values are determined from the constraints from point A. The reason for the 30% fail is the output voltage frequency variation.

The circuit's elements which influence mostly the output voltage frequency are determined from the worst results between the 100 Monte Carlo runs and they are: C5, C6,C7,L1,R1. At the second step the tolerances of these elements are decreased: Tol(C5, C6,C7,L1,R1)=5%. Fail decreases to 10%. The last step brings Tol(C5, C6,C7,L1,R1)=2% and then 100% yield and 0% fail are obtained. Data for the optimal tolerancing steps are presented in Table 1.

Figures 7 and 8 present the results from the Monte Carlo simulation of the frequency converter after the optimal tolerancing in time and frequency areas. Histograms of the output voltage period and SNR(Vout,50MHz) are built for the statistically optimized circuit.

TABLE 1. OPTIMAL TOLERANCING STEPS FOR THE FREQUENCY CONVERTER

Element name and nominal value	Step 1	Step2	Step 3
C1, 1nF	10%	10%	10%
C2, 2pF	10%	10%	10%
C3, 1nF	10%	10%	10%
C4, 1nF	10%	10%	10%
C5, 4pF	10%	5%	2%
C6, 9pF	10%	5%	2%
C7, 1nF	10%	5%	2%
C8,100pF	10%	10%	10%
L1,2.4μH	10%	5%	2%
L2, 10μH	10%	10%	10%
L3, 5μH	10%	10%	10%
L4, 2.4μH	10%	5%	2%
L5, 5μH	10%	10%	10%
R1, 1k	10%	5%	2%
R2, 1.8k	10%	10%	10%
R3, 8.2k	10%	10%	10%
Fout	43-58MHz (50±7)MHz 50MHz±35%	46.9-52.9MHz (50±3)MHz 50MHz±6%	48.3-51.8MHz (50±1.8)MHz 50MHz±3.6%
Tout	17.3-23ns 20ns±35%	18.9ns-21.3ns 20ns±12%	19.3-20.7ns 20ns±3.5%
K= Fin/Fout	8.6-11.6 10±15%	9.34-10.66 10± 6%	9.65-10.35 10± 3.5%
Total Harmonic Distortion	0.%-19.3%	0.44%-19.4%	2.47% - 16.4%
SNR (50MHz)	79-109dB	80-109dB	82-108dB
Yield Fail	70% 30%	90% 10%	100% 0%

F. Implementation of the frequency converter for different channel conversions

The frequency converter from figure 1 is tuned to convert 500MHz input signal into 50MHz output signal. In order to perform the conversions between different channels as defined in the specification from point A, the circuit parameters the influence the output frequency, given the input frequency are determined and they are: L1,L4,C5 and C6.

Table 2a presents how the initial values for L1,L2,C5 and C6 can be modified in order to perform a conversion from channel V (800MHz) at the input to channel II (80MHz) at the output. Two ways are possible: modifications of L1 and L4 values or modifications of C5 and C5 values. The second option is more suitable for realization of the frequency converter as an integrated circuit. Then C5 and C6 can be realized as varicaps.

Table 2b presents how the initial values for L1, L4, C5 and C6 can be modified in order to perform the conversions from channels IV and V to S-channels for cable TV. The output frequency is most sensitive forward L1. For this purpose the value of L1 is modified for any conversion case. For some neighbor S-channels the values obtained for L1 are very close to each other, so 1% tolerance is determined for L1.
An additional optimization for this set of conversions could be performed in order to avoid mistakes in the channel conversions.

IV channel →I channel 500MHz →50MHz 2ns →20ns	V channel→ II channel 800MHz →80MHz 1.25ns→12.5ns
L1=2.4μH **L4=2.4μH** **C5=4pF** **C6=9pF**	Varying L1, L4
	L1=0.85uH L4=0.85uH **C5=4pF C6=9p**
	Varying C5, C6
	L1=2.4μH L4=2.4μH C5=2.8pF C6=2.1pF

TABLE 2A

TABLE 2B

V channel → S-channels	C5=1p, 1% C6=1p, 1% L4=1μH, 1% Varying L1	IV channel→ S-channels	C5=1p, 1% C6=1p, 1% L4=1μH, 1% Varying L1
800MHz → 175.25MHz 1.25ns → 5.7ns	L1=1.2μH, 1%	500MHz→ 175.25MHz 2ns → 5.7ns	L1=1.25μH, 1%
800MHz → 182.25MHz 1.25ns → 5.5ns	L1=1μH, 1%	500MHz→ 82.25MHz 2ns → 5.5ns	L1=1.2μH, 1%
800MHz → 189.25MHz 1.25ns → 5.3ns	L1=0.87μH, 1%	500MHz→ 189.25MHz 2ns → 5.3ns	L1=1.1μH, 1%
800MHz → 196.25MHz 1.25ns → 5.1ns	L1=0.83μH, 1%	500MHz→ 196.25MHz 2ns → 5.1ns	L1=0.93μH, 1%
800MHz → 203.25MHz 1.25ns → 4.9ns	L1=0.82μH, 1%	500MHz→ 203.25MHz 2ns → 4.9ns	L1=0.82μH, 1%
800MHz → 217.25MHz 1.25ns → 4.6ns	L1=0.77μH, 1%	500MHz→ 217.25MHz 2ns → 4.6ns	L1=0.62μH, 1%
800MHz → 224.25MHz 1.25ns → 4.5ns	L1=0.71μH, 1%	500MHz →224.25MHz 2ns → 4.5ns	L1=0.58μH, 1%

IV. CONCLUSION

The paper presents a specific methodology for statistical design of a frequency converter circuit. A strong linear statistical correlation between the THD and the output signal frequency were determined through the statistical estimations of the circuit behavior. The optimal design is determined for a set of channel conversions between IV and V channels to I, II and S-channels (for cable TV). The optimal design is oriented to realization of the frequency converter as an integrated circuit. An additional statistical optimization is planned in order to avoid mistaking the conversion to neighbor S-channels.

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