# Statistical Estimation of Multiple Realizations in Analog Synthesis

Galia I. Marinova[1], Dimitar I. Dimitrov[2]

*Abstract* - **The paper presents a method for statistical estimation of multiple realizations in analog circuit synthesis. The case study of a frequency converter with different power supply realizations is presented as an implementation of the method for combinatorial optimization of a design with multisolution synthesis in radiocommunications. The statistical estimation permits also to exanimate the influence between the different stages in a module.**

*Keywords:* - **statistical optimization, radiocommunications modules, analog circuit synthesis, switch mode power supply, frequency converter**

## I. Introduction

The paper presents a method for statistical estimation of multiple realizations of analog circuits. The method develops the statistical optimization methodology with the simulators IESD and ORCAD/PSpice 9.2 from [4] and it is based on the theory for statistical optimization of a design in case of multiple synthesis solutions, presented in [5]. More theoretical aspects for statistical optimization are presented in [7]. The method permits to compare different synthesis solutions for a circuit, with given specifications and constraints, through the statistical estimation for each solution. It permits also to estimate statistically the mutual influences between the different stages integrated in a module. A case study is proposed for different power supply solutions of a frequency converter for radiocommunications. Two synthesis solutions are studied for the 15VDC power supply of the frequency converter - realization of the output voltage stabilization with a voltage regulator (VR) circuit and another realization with a switch mode power supply (SMPS) circuit. The voltage regulator and the switch mode power supply are studied and optimized nominally and statistically. The frequency converter is first studied with an ideal power supply of 15Vdc and then it is integrated with the VR and SMPS circuits. A goal function is defined for the determination of the optimal solution for the synthesis of the frequency converter module with a power supply circuit. The different synthesis solutions are simulated and estimated statistically and the optimal design solution is determined. The mutual influences between the frequency converter and the two power supply circuits are estimated and some conclusions are draft for their performances.

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## II. Multisolution Synthesis of a Module for Radiocommunications

Multiple synthesis solutions for the power supply of a frequency converter module are studied. It is an implementation of the method proposed, in radiocommunications.

### *A. Multisolution synthesis of a frequency converter realized with different power supply circuits*

Figure 1 presents the frequency converter (FC) from [3] and three synthesis solutions: figure 1a, whit an ideal 15Vdc voltage power supply; figure 1b, where the stabilized voltage comes from a voltage regulator circuit; figure 1c, where the stabilized voltage comes from a switch mode power supply.

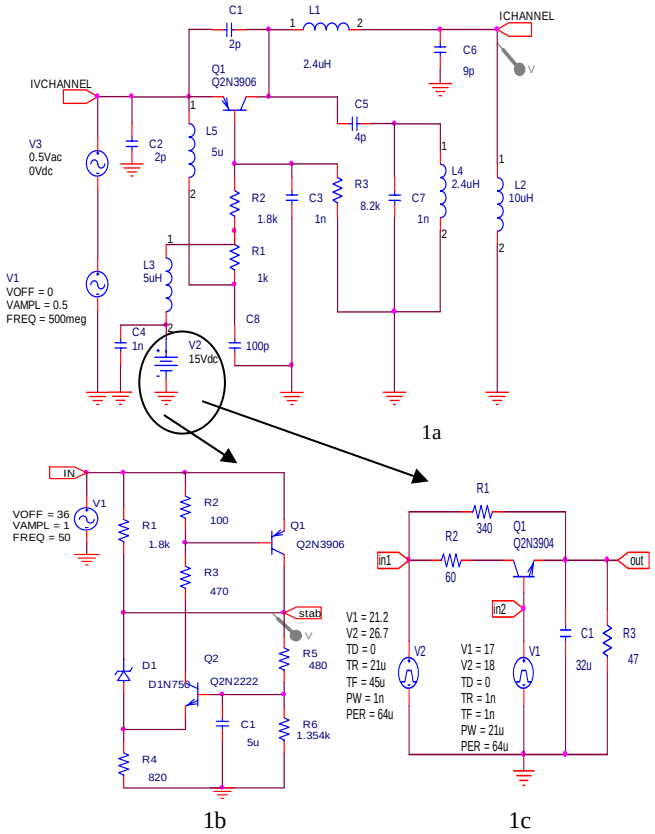



Figure 1. Multisolution synthesis of a frequency converter with different power supplies a)frequency converter with ideal power supply of 15dc b) voltage regulator circuit c) switch mode power supply circuit

The circuits from figures 1a,1b and 1c are studied nominally and statistically. The statistical optimization of FC is studied in [3].

*B. Nominal and statistical estimations of the power supply circuits*

The specification of the power supply circuit is to provide a 15V stabilized output voltage with less than 1% pulsation. The constraints on the DC voltage statistical variations are defined for each circuit.

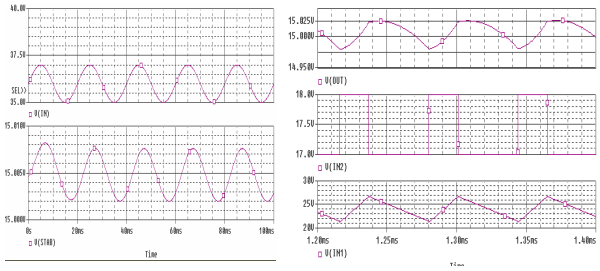
- **Voltage regulator circuit**

The voltage regulator (VR) circuit from figure 1b is studied and optimized nominally and statistically in [2]. There the circuit is specified for 24V stabilized voltage. In order to integrate VR with the frequency converter module, the stabilized voltage is specified to 15V and the design is parameterized through a new value for R6=1.354kΩ. The input and output voltages obtained from nominal simulation with ORCAD/PSpice 9.2 in time area for the VR are presented on Figure 2a. Figure 3a presents the 100 Monte Carlo simulation runs in Time area for the stabilized voltage, of the VR with the optimal tolerance values defined from [2]. The VR elements have the following parameters:

VR={1.8kΩ,15%; R2=100Ω,15%;R3=470Ω,15%;
R4=820Ω,10%; R5=480Ω,1%; R6=1.354k Ω,1%;
C1=5μF,15%}

- **Switch mode power supply**

The circuit of the switch mode power supply is presented on figure 1c. It is studied analytically in [1].



2a 2b

Figure 2. Nominal response in time domain a) input and output stabilized voltages of the voltage regulator b) iput pulses and output stabilized voltages of the switch mode power supply

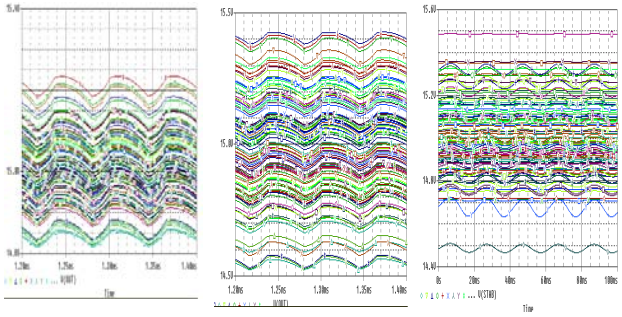


Figure 3. Statistical simulation of the voltage regulator and the switch mode power supply a) stabilized voltage of the voltage regulator b) stabilized voltage of the initial design of the SMPS c) stabilized voltage of the statistically optimized SMPS design

The nominal design from [1] was for 195V stabilized voltage and it is modified for 15V stabilized voltage through the parameter definition of the pulse voltages V1 and V2, which control the stabilized voltage value. Figure 2b presents the nominal response in time domain for the input pulses and the output stabilized voltage for the SMPS.
The goal function for optimal tolerancing of the SMPS circuit is to obtain the maximal tolerance values that guarantee 100% yield following the circuit constraints for VDC=15V±1%, and for output voltage pulsation amplitude inferior than 0.15V. As for all runs the pulsation is inferior than 0.15V, the goal function takes in consideration only the constraints on the output voltage. The goal function is defined as follows:

Max tol(R1,R2,R3,C1)
[V1pulse(21.2V, 26.7V,0.21μs,45μs, 1ns, 64μs),
V2pulse(17V, 18V,0,1ns, 1ns, 64μs),
Vdc=15V±0.15V, VMpulsatios<0.15V]

The statistical design steps for the optimal tolerancing of the SMPS are presented in table 2.

TABLE 1. OPTIMAL TOLERANCING STEPS FOR THE SMPS CIRCUIT

| SMPS elements | Step1 | Step2 | Step3 |
|---|---|---|---|
| R1 | 15% | 5% | 5% |
| R2 | 15% | 15% | 15% |
| C1 | 15% | 15% | 15% |
| R3 | 15% | 5% | 2% |
| Stabilized voltage Vdc | 14.56-15.42V | 14.79-15.27V | 14.852-15.15V |
| Yield<br>Fail | 60%<br>40% | 85%<br>15% | 100%<br>0% |

The optimal design of the SMPS circuit is determined as:

SMPS={R1=340Ω,5%; R2=60Ω,15%; R3=47Ω,2%,
C1=32μF,15%}

Figure 2b presents the statistical simulation results in time area for the output voltage of the initial SMPS circuit from step 1 in Table 1. Figure 2c presents the output voltage for the statistically optimized SMPS circuit from step 3 in Table1.

## III. STATISTICAL ESTIMATION OF THE MULTIPLE REALIZATIONS OF THE FREQUENCY CONVERTER MODULE WITH DIFFERENT POWER SUPPLIES

A goal function is defined for the statistical optimization of the synthesized modules integrating FC with a power supply. The different synthesized solutions are analyzed nominally and statistically and then they are estimated statistically. The influence of the FC circuit on the power supply circuits is determined.

*A. Goal function for combinatorial optimization of the frequency converter module with different power supplies*

The constraints for the frequency converter parameters are defined from the telecommunication standards in [6]. The three circuit realizations are:

C1=C(FC,Vdc=15V) - FC with ideal 15VDC power supply
C2=C(FC,Vdc(VR)) - FC with VR
C3=C(FC,Vdc(SMPS)) - FC with SMPS

The results from the Monte Carlo simulations in time and frequency area, for each realization, are defined as follows:

MC(C1)={T±ΔT(C1),F±ΔF(C1),SNR(50MHz) ±ΔSNR(C1), THD±ΔTHD(C1)}
MC(C2)={T±ΔT(C2),F±ΔF(C2),SNR(50MHz) ±ΔSNR(C2), THD±ΔTHD(C2)}
MC(C3)={T±ΔT(C3),F±ΔF(C3),SNR(50MHz) ±ΔSNR(C3), THD±ΔTHD(C3)}

The yield and the fail, for each circuit realization, are defined as:
m-number of MC runs for a circuit

$$Yield(C)=\frac{\sum_{k=1}^{m} Yk \cdot 100\%}{m},$$

$$Fail(C)=100\%-Yield(C)$$

k=1,m
Tk∈20ns±5% (Fk∈50MHz±5%)
& THDk<20%
&SNRk(50MHz)>40dB
=> Yk=1
Tk∉20ns±5% (Fk∈ 50MHz±5%)
& THDk>20%
&SNRk(50MHz)<40dB
=> Yk=1

The goal function for the optimal circuit design from the multiple synthesis solutions is defined as follows:

Copt = C1, Yield(ci)=100%(Fail=0%),
Min(T(Ci)-20ns) & Min ΔT(Ci),
[Min(F(Ci)-50MHz) & Min ΔF(Ci)]
& Min THD(Ci) & Min$THD_H$(Ci)
& Max SNR(Ci) & Max$SNR_L$(Ci)

where $THD_H$(Ci) is the higher value for the THD coefficient for all the Monte Carlo runs of the circuit Ci
Max$SNR_L$(Ci) is the lower value for the SNR for all the Monte Carlo runs of the circuit Ci.

As the goal function includes several criteria it could occur different circuit realizations to be optimal for different criteria. In order to define the optimal solution, a priority of the different criteria in the goal function should be defined.

*B. Statistical simulation of the multiple realizations of the frequency converter module*

Figure 4a presents the realization of the frequency converter module with a voltage regulator and figure 4b presents the realization of the FC with a switch mode power supply circuit.

Figure 5a and 5b present the results from the Monte Carlo simulations in time and AC area for the stabilized voltage, the output voltage and the SNR, of the circuits C2 and C3.

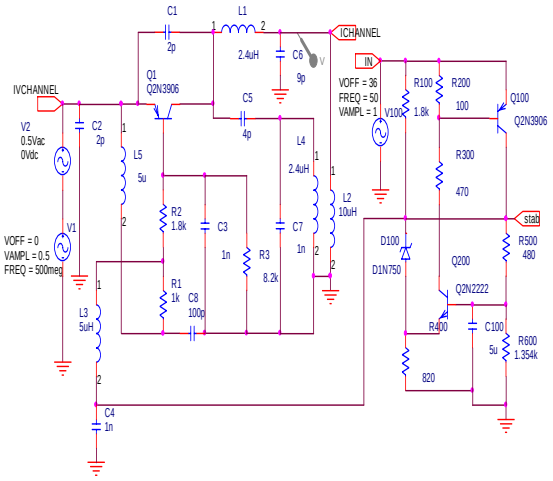



Figure 4a. Frequency converter with voltage regulator

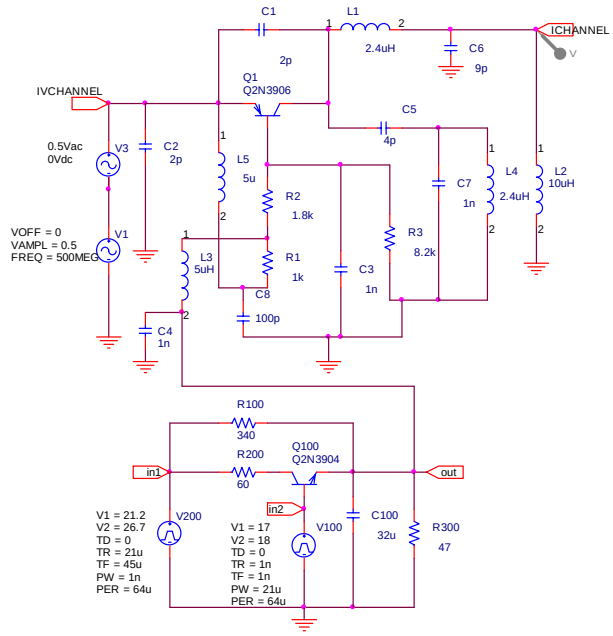
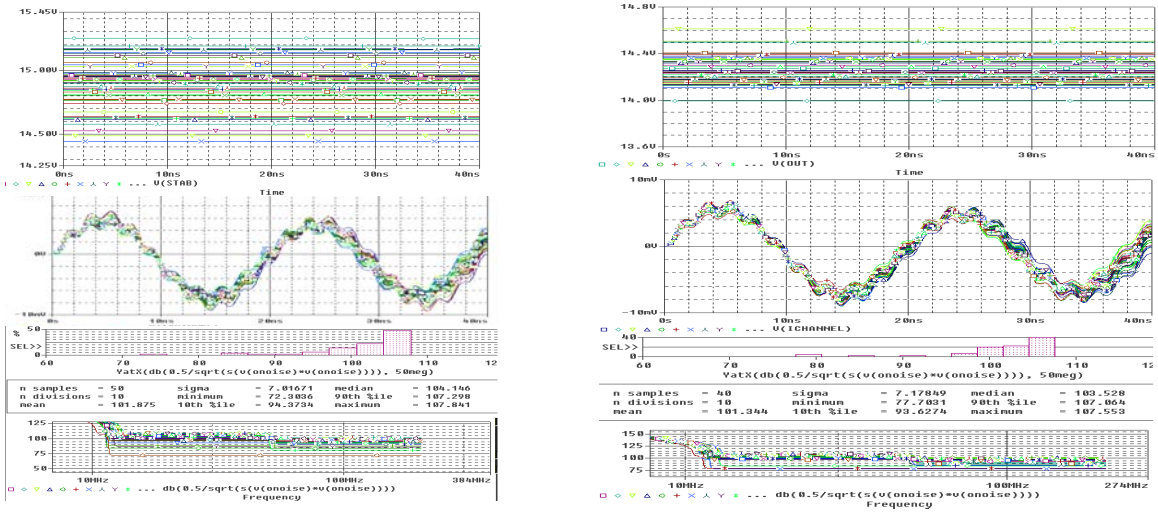



Figure 4b. Frequency converter with switch mode power supply

Table 2 presents the estimations of the different synthesis solutions for the frequency converter module. These estimations will serve the application of the criteria from the goal function.

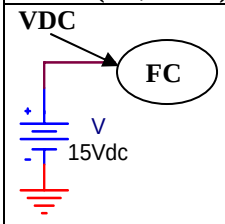
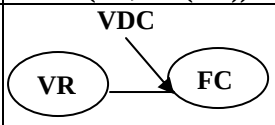
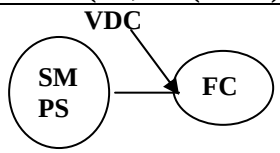
Table 2 permits to determine the influence of the statistical variations of the power supply circuits on the FC behavior, and to define the influence of the statistical variations of the FC on the different power supplies. It permits also to compare the different power supply realizations with the case of ideal 15VDC power supply of the FC.



5a 5b

Figure 5. Results from Monte Carlo simulations in time and AC area for the stabilized voltage, the output volatge and the signal to noise ratio a) for the FC and VR b) for the FC and SMPS

TABLE 2. NOMINAL AND STATISTICAL ESTIMATIONS OF THE DIFFERENT SYNTHESIS SOLUTIONS FOR THE FREQUENCY CONVERTER MODULE

| **Multiple realizations of the FC module with different power supplies** / **Nominal and statistical simulation of the different synthesis solutions for the FC module** | **C1(FC,15Vdc)** | **C2(FC,Vdc(VR))** | **C3(FC, Vdc(SMPS))** |
|---|---|---|---|
| |   |   |   |
| Nominal design of the frequency converter | Vdc=15V<br>T=20ns<br>F=50MHz<br>THD=4.54%<br>SNR(50MHz)=109dB | Nominal design of the voltage regulator | Nominal design of the switch controlled power supply |
| | | Vdc=14.961V<br>T=20.222ns<br>F=49.45MHz<br>TDH=10.45%<br>SNR=106.489dB | Vdc = 14.274V<br>T= 20.453ns<br>F=48.9MHz<br>TDH=9%<br>SNR=86dB |
| | | Optimal design of the voltage regulator | Optimal design of the switch controlled power supply |
| | | Vdc =14-15.34V<br>T=19.61-20.70-21.05ns<br>F=48.3-51MHz<br>TDH=6.4-12.16%<br>SNR=105.77-106.343dB | Vdc = 14.127-14.651V<br>T=20.2-20.57ns<br>F=48.61-49.5<br>TDH=8.6-11%<br>SNR=106.4-106.7dB |
| Optimal design of the frequency converter obtained by optimal tolerancing | Vdc=15V<br>T=19.3-20.7ns<br>F=48.3-51.84MHz<br>THD=2.47-16.4%<br>SNR=82-108dB | Nominal design of the voltage regulator | Nominal design of the voltage regulator |
| | | Vdc = 14.96-14.962V | Vdc =14.2702-14.2784V |
| | | Optimal design of the voltage regulator | Optimal design of the switch controlled power supply |
| | | Vdc = 14-15.24V<br>T=19.14-20.77ns<br>F=48.14-52.25MHz<br>TDH=4.91-16.78%<br>SNR=72.3-107.8dB | Vdc = 13.99-14.65V<br>T=19.24-20.9ns<br>F=47.85-51.97MHz<br>TDH=0.344-12.61%<br>SNR=77.7-107.55dB |

The comparison between the results in Table 2 for the realizations of the FC module with VR and with SMPS circuits and the results for the FC module with an ideal 15V dc power supply, show that both synthesis solutions are slightly different from the ideal case and they don't deteriorate considerably the FC module performance. The results for the nominal designs of the FC (with 0% tolerances) and the statistically optimized VR and SMPS circuits (with optimal tolerances) show the impact of the power supply variations on the FC module parameters. The variations of the power supply value influence considerably the FC parameters.

### *C. Statistical estimation of the influence the frequency converter has on the different power supply circuits*

The influence of the FC on the stabilized voltage pulsation of the VR and of the SMPS circuits is estimated. The nominal and statistical simulation with ORCAD/PSpice 9.2 of the FC with SMPS shows that there are not pulsation from the FC induced to the stabilized SMPS voltage. But the simulations of the FC with the VR circuit show that the FC induces pulsation into the stabilized voltage. The results from the nominal simulations in time area for the stabilized voltage of the FC with VR circuit, which are presented on figure 6a show that the pulsation induced from the FC to the stabilized voltage is:

Vstab(pulsation)= {-14.892V,+0.047V}
ΔVstab(pulsation)= {-0.108V,+0.047V}
freq(Vstab(pulsation))=38MHz

The stabilized output voltage with the pulsation induced from the FC covers still the constraints for the VR circuit: Vstab=15V±0.15V.

Figures 6b and 6c present the results from statistical simulation of the pulsation induced in the stabilized voltage from the FC. The response on figure 6b is from a simulation of a nominal VR circuit (with 0% tolerances) and statistically optimized FC (with optimal tolerances). The response from figure 6c is from a simulation of the statistically optimized FC and the statistically optimized VR (both with optimal tolerances). In both cases the constraints are not broken and the yield remains 100%. These data allow to conclude that the SMPS circuit is less sensible to influences from the FC than the VR circuit is. Tables 3a and 3b present data for the variations of the stabilized voltage values for the VR and for the SMPS circuits in nominal designs and in designs where they are integrated with the FC circuit.

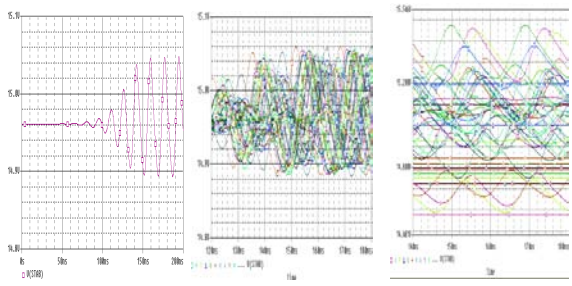


Figure 6. Pulsation of the stabilized voltage in the voltage regulator induced by the frequency converter a) nominal design FC+VR b) nominal design of the VR and optimal tolerances of the FC c) design with optimal tolerances of the FC and VR

TABLE 3A. ESTIMATIONS FOR THE VR

| Voltage regulator -VR | Stabilized voltage Vdc |
|---|---|
| VR, nominal design | 15V |
| VR, optimal tolerances | 14.7-15.4V |
| VR nominal design<br>FC nominal design | 14.961V |
| VR, nominal design<br>FC, optimal tolerances | 14.96-14.962V |
| VR, optimal tolerances<br>FC, optimal tolerances | 14-15.24V |

TABLE 3B. ESTIMATIONS FOR THE SMPS

| SMPS | Stabilized voltage Vdc |
|---|---|
| SMPS, nominal design | 15V |
| SMPS, optimal tolerances | 14.85-15.15V |
| SMPS, nominal design<br>FC, nominal design | 14.274V |
| SMPS, nominal design<br>FC, optimal tolerances | 14.2702-14.2784V |
| SMPS, optimal tolerances<br>FC, optimal tolerances | 13.99-14.65V |

The examination of these data shows that the stabilized voltage value of the SMPS circuit is less sensible to element tolerances than the stabilized voltage value of the VR circuit is. But the value of the stabilized voltage of the SMPS falls down with 720mV when it is integrated with the FC circuit. In that case the value of the stabilized voltage in VR decreases with 39mV.

## IV. OPTIMAL SOLUTION FOR THE FREQUENCY CONVERTER MODULE

The two module realizations C2 and C3 are estimated following the definition of the goal function from point IIIA and results are given in table 4.

TABLE 4. ESTIMATION OF THE GOAL FUNCTION CRITERIA FOR THE TWO REALIZATIONS

| Realization parameter | C2 | C3 | Criteria application | Optimal circuit |
|---|---|---|---|---|
| T-20ns | 0.222ns | 0.453ns | (T-20ns)(C2)< (T-20ns)(C3) | C2 |
| ΔT | 1.09ns | 1.66ns | ΔT(C2)< ΔT(C3) | C2 |
| F-50Hz | 0.55MHz | 1.1MHz | (F-50MHz)(C2)< (F-50MHz)(C3) | C2 |
| ΔF | 4.11MHz | 4.12MHz | ΔF(C2)< ΔF(C3) | C2 |
| THD | 10.45% | 9% | THD(C3)< THD(C2) | C3 |
| $THD_H$ | 16.7% | 12.61% | $THD_H$ (C3)< $THD_H$(C2) | C3 |
| SNR | 106.48dB | 86dB | SNR(C2)> SNR(C3) | C2 |
| $SNR_L$ | 72.3dB | 77.7dB | $SNR_L$ (C2)< $SNR_L$ (C3) | C3 |
| Yield<br>Fail | 100%<br>0% | 100%<br>0% | Yield(C2)= Yield(C3)<br>Fail=(C2)= Fail(C1) | C2,C3 |

A general conclusion is that both solutions are suitable for FC converter module realizations Anyway depending of the priority criteria definition in the goal function an optimal solution for the frequency module with a 15V dc power supply is determined as follows:

- If the priority in the optimization criteria is given to the constraints on the period and frequency and the SNR of the output voltage, the optimal solution is the one realized with the FC and the VR:
  Copt(T(F),SNR)=C2
- If the priority in the optimization criteria is given to the THD or to the $SNR_L$, then the optimal solution is the one realized with the FC and the SMPS:
  Copt(THD, $SNR_L$)=C3.

## V. CONCLUSION

The method for statistical estimation of multiple synthesis solutions, proposed in this paper was implemented for a radiocommunications example consisting in the optimal synthesis of a frequency converter module with a power supply. Two different power supply solutions (one with a voltage regulator circuit and another with a switch mode power supply circuit) were estimated and then compared following the criteria from a goal function. The optimal solution was determined depending on priorities of the criteria in the goal function. Besides this the influences between the FC,VR and SMPS circuits were studied and it was proven that the FC induces pulsation in the VR and it doesn't induce pulsation in the SMPS circuit. Although the SMPS circuit proves to be less sensitive than the VR circuit, the optimal realization of the FC module estimated on the higher priority of the constraints, on the output voltage frequency, is the module realized with the VR circuit.

The study described in this paper proves the large possibilities for implementation of the statistical estimates in optimal synthesis of analog circuits and more precisely for radiocommunication modules. Additional case studies in radiocommunications would enlarge the optimal synthesis know-how in this area.

## ACKNOWLEDGEMENT

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