Method and Example of Errors Evaluation During the Conversion of a Band Wide Signal

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Abstract - **There is a possible solution of the classical problem for calculating the sampling frequency Fd when sampling analog signal with several components (a band wide signal). The example has five frequency components. For each frequency component Fs a sampling factor N=Fd/Fs and an amplitude error Emax is calculated.**

Keywords - **sampling frequency, errors, band wide signal**

I. INTRODUCTION

Sampling a band wade signal (BWS) is a common task in the signal processing electronic equipment. During this process a lot of parameters should be evaluated in order to have knowledge about the differences between the analog signal (AS) or the "analog original" and its digital representation (the "digital copy" or the approximation of the AS). Normally, as a result of this evaluation the following parameters should be calculated:

- Signal sampling factor (SSF) N=Fd/Fs where Fd is the sampling frequency and Fs is the maximal frequency of interest in the BWS. The SSF was discussed in [1,2]. Most frequently (but not always) the SSF N is greater or equal to 2 (N>=2).
- Calculating the minimum number of the converters bits (MNCB) n in order to neglect the converters error.
- Calculating the differences (e.g. amplitude errors, peak to peak amplitude errors, etc) between the AS and its digital approximation .

The purpose of this paper is to apply the method developed by the author in [1, 2, 3] and to give an example of amplitude errors evaluation during the sampling of a band wide signal (BWS) (AS build by several sinusoidal and cosinusoidal (SS and CS) components.

II. THE TASK

Definition: The simplest BWS which contains two line in its spectrum (one of them is the Direct Current (DC) component with amplitude B and the other is a SS with frequency Fs, amplitude Am and phase B), has four basic parameters (Am, Fs, φ, B) and could be defined with Eq. 1

$$A=Am*\sin(2*\pi*Fs+\varphi)+B \quad (1)$$

Assuming B=0 and φ=0 in (1) simplifies the Eq. (1) of AS but does not reduce the number of the parameter to reconstruct to two. It is just giving the value of zero to two of them. Consequently in order to reconstruct this AS in a simple way we are in need of sampling factor N>=4 [1, 3] or one sample per parameter to reconstruct.

It was proven in [3] that the maximum amplitude error Emax during sampling the SS A=Am*sin(2*π*Fs) is calculated with Eq. 2

$$Emax= (1- \sin(90- (180/N)) \quad (2)$$

where N=Fd/Fs is the SSF (in this case N>=2) and the number of the converter bits n should be infinity (n→∞).

In this paper we will examine an example of sampling a BWS with five spectrum components with different amplitudes. The signal is defined by Table 1. The phase relations are defined in one particular moment and could vary in time due to instability of the parameters of the sources and the circuits. The components of the AS could exists in any combinations (some or all of the components could disappear temporarily).

The task consist of calculating the SSF N, the sampling frequency Fd and the number of the converters bits n in order to satisfy the following conditions:

- Maximal amplitude error Eamax (assuming Eamax equal to resolution of the converter in amplitude) for every frequency component should be less than +-5%;
- Maximal amplitude error Eamax should be distributed between the amplitude error EN from the SSF N and error Eadc from the limited number of the converters bits n.
- We will chose an appropriate analog to digital converter (ADC) with the calculated number of bits n and conversion time Tc.

III. THE SOLUTION

The problem will be solved in several steps (common for most of the similar applications).

Step 1: Evaluation of the maximal signal amplitude Asmax and calculating the full scale voltage Vfs of the converter.

Since the phase of each of the signal components is unknown and could be variable the evaluation of the maximal signal amplitude (Asmax) and the maximal signal peak-to-peak amplitude (Asppmax) could be made accordingly to the worst case scenario principle "The maximal signal amplitude could be as high as the sum of the amplitudes of its components". In this case the sum of the amplitude of all

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components is Asmax<= 4.9V and Asppmax=2*Asmax<= 9.8V.

The full scale (FS) voltage of the converters Vfs should be higher or equal to Appmax. We are chousing Vfs approximately 10V because this is one of the industry standard voltage ranges. Also we could select and industry standard voltage reference source withVref=10.240V.

Vref, Vfs, the minimal (Vinmin) and maximal (Vinmax) input voltage of the converter should be appropriately selected in order not to have underflow or overflow of the input range. It is desirable that the maximum of the input signal to use at least the half of the input range of the ADC (to be higher that Vfs/2 and to activate all of the ADC bits. For this purpose the maximum amplitude and peak to peak amplitude of the AS should de exaluated. This could be done in a theoretical or in practical way or in both way. The minimal value of AS should be at least 10*LSB (LSB= Least Significant Bit) in order to maintain at least 10% relative accuracy. The "underflow" and the "overflow" should be avoided because there will be irreversible lost of information. In most of the cases selecting and industry standard input range is making easier the practical implementation.

In this example the sum of the amplitude of frequency components Amax is

Amax = A1+A2+A3+A4+A5=4.9V

We could admit that the maximal amplitude of the AS is not higher than 4.9V and the maximal peak-to-peak amplitude of the signal is not greater than 2*4.9V=9.8V. Vfs and the Vref of the ADC could be chosen at industry standard 10.240V. With Vref=10.240V, the minimal output voltage will be 0.0V and the maximal will depend of the number of the converter bits and should be higher than 9.8V calculated above or Vfs>9.8V. From the other side normally we are having Vfs =Vref-1*Vlsb, where Vlsb is the voltage step for one LSB.

TABLE I
AN EXAMPLE OF BAND WIDE SIGNAL WITH FIVE COMPONENTS

Input test signal				
# (I)	Compo-nent	Am= App/2	App	Fsi
1	DC	2.5V*	5V	0Hz*
2	SS	0.6V	1.2V	2.5Hz
3	CS	0.8V	1.6V	22Hz
4	SS	0.3V	0.6V	150Hz
5	CS	0.7V	1.4V	460Hz
Obtained results after the sampling (n=10 bit)				
# (I)	+-5%*Am	Number of LSB	Ni = Fd/Fs	Emax, [%]
1	+-125mV	+-12.5	∞	0.0
2	+-30mV	+-3	1840	0.000146
3	+-40mV	+-4	209.1	0.0113
4	+-15mV	+-1.5	30.7	0.523
5	+-35mV	+-3.5	10	4.83

Notes: (*) – conditional value; (#) the index is changing from 1 to 5 because the signal has five frequency components; SS/CS – sinusoidal/cosinusoidal signal; The results are for Fd=4600Hz, n=10 bit, LSB=10mV and Eadc=+-0.0488%.

Step 2:. Calculating the number of the converters bits

We have to estimate the effective resolution for each signal component and especially the case with the component with the smallest amplitude (component #4 in this case). The resolution for the component #4 or Resmin4 should be less than +-15mV (+-5% from 0.3V) or

Rezmin4=+-5%*Am4=+-3%*0.3V=+-15mV<=+-0.5*LSB

Now we could calculate the maximal value of one LSB.

If +-0.5*LSB<=+-15mV, then 1*LSB<=30mV

It is possible to calculate the minimal number of the equally spaced step in the transition characteristic of he converter Lvmin in order to have Rezmin4 equal to one level

Lvmin = Vfs/Rezmin4=10V/30mV=333.3 levels.

The minimal number of the ADC bits is

nmin=lg(Lvmin)=lg(333.3)= 8.38 bits

We could choose a 9-bit converter. But a good idea is to use a converter with from 1 to 4 bits more that the calculated value due to the additional sources of errors. With n=10 bits the levels are

Lv(n)=Lv(10)=2*exp(10)=1024 levels

This is satisfying our solution because

Lv(10)=1024 levels >Lvmin=333.3 levels

In case of 10-bit converter one LSB will correspond to 10mV because

Vlsb=Vref/2exp(n) = 10240mV/1024=10mV<30mV

The maximal input voltage for the ADC is

Vfs=Vref-1*LSB=10240mV-10mV=10230mV

The resolution of the ADC is

Res(n)=Res(10)=+-0.5*Vlsb=+-10mV/2=+-5mV

And correspond to the task because

Rezmin4<=+-15mV.

The error of the ideal 10-bit ADC Eadc is

Eadc(10)=(+-1/2)*Vlsb=+-(1/2)*100%/2exp(n)=

= +-(1/2)*100%/2exp(10)= +-0.0488%

It is important to note two results:

- Usually, the sampling error (SE) of the components with highest frequency depends mainly from the SSF N.
- Usually, the SE of the components with the lowest frequencies depends mainly on the number of the converters bits n.

As we could see from the Table I that for the components 1, 2 and 3 the error EN is less than Eadc, and for the components 4 and 5 EN is greater than Eadc.

Step 3: Calculating N=Fd/Fs and Fd

Accordingly to the theorem of Kotelnikov-Shannon-Whitaker the sampling frequency Fd should be chosen according to the Eq. 3

$$Fd=2*Fsmax= 2*Fs5=2*460Hz=920Hz \quad (3)$$

Here will apply a the approach discussed in [1, 2, 3]. We will calculate the SSF N=Fd/Fs for each frequency component. A special attention should be paid to the component with the highest frequency because it will be with the smallest SSF and with the highest possible amplitude error. In this example the component #5 with amplitude Am5=0.7V and with frequency

Fs5=460Hz has the maximal signal frequency. The amplitude resolution for this component is +-35mV or +-5%*Am.

The amplitude error of +-5% should be distributed between: 1/ The amplitude error AN5 due to the finite SSF N5=Fd/Fs5; 2/ The error of the converter Eadc (In the ideal case Eadc is the same for all frequency components).

We could apply the model of the maximal or root-mean-square (rms) error or any other appropriate model. The second is given with the formulae:

Ea5rms= sqr(EN5rms*EN5rms+Eadcrms*Eadcrms),

Where Ea5rms is the rms error for the component #5,

Eadcrms is the rms error for an ideal 10-bit ADC.

If we apply the model for the maximal error for he component #5 we will obtain.

EN5max=EN - Eadc=5%-0.0488%=4.95%.

Usually for he highest frequency component the difference between EN5rms and EN5max is small. Also, for the highest frequency components Eadc is smaller that EN. (The error of the finite number of bits n is lower then the amplitude error from the possible not sampling the SS/CS in its maximum which depend on the SSF N=Fd/Fs)

We are calculating the SSF for the component #5:

N5=180/(90-arcsin(1-EN5max))=

=180/(90-arcsin(1-0.0495))=9.94

We are accepting N5=10 and the sampling frequency Fd is

Fd=N5*Fs5=10*460Hz=4600Hz

The sampling period Td is

Td=1/Fd=1/4600Hz=217.39us

Now with sampling frequency Fd=4.6kHz we have the guarantee that with 10-bit ADC all components of the AS will be converted (transferred into digital codes) with amplitude error less than required Eamax=+-5%.

The Eq. 2 could be used in order to calculate the maximal possible amplitude error for each component for Fd=4600Hz. The results are given in Table 1 (EN1max=0.0, EN2max=0.000146%, EN3max=0.0113%, EN4max=0.523%, EN5max=4.83%).

It should be noted that the following equation n=lg(1/Emax), [bit] could be considered *as the quantity of information in amplitude* transferred from the AS to its digital "copy" (if Emax is considered equal to one step of the transfer characteristic of the conveter).

IV. SELECTING AN APPROPRIATE ADC

There are a lot of ADC with accuracy of 10 or more bits, with serial or parallel output interface and with conversion time Tc less than 200 us which are suitable candidates for that task. The solution will be tested on a 8-bit 6809 microprocessor and the ADCs with parallel interface were selected:

- 10-bits ADCs: AD571K (Tc=25us), AD573K (Tc<20us) and AD579 (Tc<1.8us).
- 12-bits ADCs: AD572 (Tc<25us), AD574AK(Tc<35us), AD674A(Tc=15us) and ADADC80 (Tc=25us).

Also, there are several micro-controllers with 10-bit internal ADC which could be used as an intelligent peripheral ADC to the testing system (e.g. PIC 18F876, 68HC12 etc.). The internal source of errors and code distribution of ADC should be evaluated before taking the final decision.

If we are using the 10-bit ADC with parallel outputs AD574AK (Tc<35us, LSB=10mV) without S/H we could sample AS with peak to peak amplitude App=10Vpp and frequency Fsmax(adc), calculated with the formula:

Fsmax(adc) = 0.5*LSB/(π*App*Tadc)=

=5mV/(π*35us*10Vpp)=4.5Hz.

If we choose ADC AD574AK together with SH AD585 we could sample AS with peak to peak amplitude up to 10Vpp and frequency up to 10 kHz. In most of the cases the AS at the ADC input should not change more than +-0.5*LSB (sometimes even less than that value) for the time of one conversion (in this case Tcmax=35us). From the practical point of view the ADC with internal SH are interesting, e.g.:

- 10-bit ADC AD7579/AD7580 with up to 50000 conversions/sec and "band wide" up to 25KHz;
- 12-bit AD678 with up to 200000 conversion/sec and "band wide" up to 500 KHz

We will chose the model AD571K (Tc=25us, n=10) because the its parameters are satisfying and the price is acceptable.

V. SELECTING A SAMPLE AND HOLD CIRCUIT

We should select an appropriate SH circuit in order to sample and hold the AS during the conversion time of the ADC. During the selection process the following should be taken into the consideration:

- The aperture time Tap(sh) of the SH should be low enough for the selected ADC (n=10 bits in this case), maximal signal frequency (Fsmax=460Hz) and sampling frequency Fd= 4.6KHz (Td=217.4us);
- The "sample time" Ts should be much lower than Td in order not increase the conversion time Tc of the ADC. For example with Td=217.4us we should select Ts<10 us in order to have accuracy less than +-0.5*LSB=+-0.0488%.

We will use SH model SHC298AM of Burr-Brown. It has 12-bit accuracy, band wide for large signal (+-10V) up to 16 kHz (with hold capacitor Ch=10nF), SR of the output voltage typically 2V/us, maximal aperture time Tapmax= 200ns and sample time with accuracy of 0.01% when the input voltage is changed with step 10V less than 10us. In order not to increase the conversion error of the ADC the signal of the SH input should not change during the conversion more than the value Ea(S/H) calculated below

Ea(S/H) <=+-0.5*LSB=+-0.0488%=+-5mV

The maximal frequency of the SS with peak to peak amplitude App=Vfs=10.230V, which could be processed with SH with aperture time error less than +-0.5*LSB is

Fsmax(S/H)=Ea(S/H)/π*Tapmax*App=

=5mV/(3.14*200ns*10.23V)=779Hz>460Hz

The frequency calculated above is higher than the maximal frequency component (Fs5=Fmax=460Hz) and consequently the choice of the SH is appropriate.

If the peak to peak amplitude is App=10V and the resolution of ADC is Eadc=+-5mV and the maximal signal

frequency is Fsmax=460Hz we could calculate the maximal allowed aperture time Tapmax for SH

$$Tapmax = Eadc/(\pi*App*Fsmax) = 5mV/(\pi*460Hz*10.23V) = 338ns.$$

The sample and hold factor (SHF) Nsh is defined with the Eq. 4 in [1]:

$$Nsh = Tapadc/Tapsh \quad (4)$$

Where Tapadc is the aperture time of the ADC (or the conversion time of the ADC) and Tapsh is the aperture time of SH. In fact the aperture time of SH (Tapsh) is replacing the aperture time of ADC (Tapadc).

In fact SH is useful only if Tapsh<<Tapadc. This is the reason of introducing the parameter "sample and hold factor" (SHF) given with the Eq. (4) which is measuring the effectiveness of the addition of the SH in front of ADC. Normally SHF Nsh>>1 and is guaranteeing then the band with of the ADC will be enlarged with the addition of SH and not reduced. More information about the ADC and SH could be found in [4, 5].

VI. The importance of the relative accuracy and the amplitude error

When the amplitude of the AS to be sampled is changing the number of bits activated is changing also. Lets us compare the cases of two samples from two different signals sampled with 10-bit ADC with codes from 0 to 1023:
Case 1: The samples are in the range from 0 to 10*LSB.
Case 2: The samples are in the range from 0 to 600*LSB.
In both cases the absolute rounding error is +-0.5*LSB or +-0.0488% (for n=10bit) from the full scale (FS). The relative rounding error is quite different in both cases. In the first case the relative error E1 is

$$E1=100\%*(+-0.5*LSB/10*LSB) = +-5\%$$

In the second case the relative error E2 is

$$E2=100\%*(+-0.5*LSB/600*LSB) = +-0.083\%$$

If the samples are processed digitally (for example in the same filter section) the results from the processing the second signal will be much more accurate.

In conclusion there is a need of formula guaranteeing the maximal amplitude error (the maximal difference between the amplitude value of the signal and the maximal sample) which in fact is guaranteeing that at least one sample per period will have at least the guaranteed amplitude. The Eq. (2) is guaranteeing the maximal amplitude error Eamx during the sampling a SS with amplitude A and the maximal value Amax of the samples after the ADC or Amax=A-Emax.

VII. Control of the solution

The AS coming from most the signal sources is band limited (Fsmax << ∞) and with limited peak-to- peak amplitude (Aspp<<∞). That means that it has a limited maximal slew rate (SRmax << ∞) and could de represented as a finite sum of SS and CS and a direct current (DC) component. These AS could be modeled successfully with a set of analog or digital sinusoidal generators.

The control of the solution is made with modeling the example given before with set of SS and CS signal generators and comparing the signal before ADC with signal after the reconstructing DAC. Moreover the samples are stored in the memory and sorted in order to find the maximal and minimal value and errors are searched. Five signal sources were used and a five input precision summing stage with TL071 or LF356 operational amplifier was used.

The amplitude, frequency, phase and a DC component of each signal component were evaluated and compared with the input signals. The test was made for any signal component and for any combination of them. When two or more signal components are added and processed the inter-modulation distortions (IMD) were discarded in order to simplify the task. The hardware is described in [2].

VIII. Conclusions

A method and example of errors evaluation during the sampling of a BWS was given. The SSF N=Fd/Fs, the sampling frequency Fd, the maximal amplitude error Emax, the number of the converters bits n and the SHF Nsh were calculated in order to satisfy previously done amplitude error for each signal component. Electronic components for a practical realization were selected.

The method is simple and effective and is applicable for any analog to digital conversion system. It is applicable to system with microprocessor, micro-controllers and a free running ADC+DAC system and is useful for testing analog channels including analog to digital conversion.

This example is an application of the method of evaluation of the amplitude errors during A to D conversion of single or multi-tone signal. It is important because due to he phase changes and/or instability of some frequency component could be lost or and adverse interference could be produced.

Work should de done in order to build much more representative and comprehensive models and equipment of the sampling and signal reconstruction process.

References

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