Advanced Current mode CMOS OTA Based Band Pass Filters for Detector Readout Front Ends

T. Noulis¹, C. Deradonis² and S. Siskos³

Abstract - CMOS current mode band pass filters for front end electronics are proposed. Three semi Gaussian shaper topologies based on operational transcondactunce amplifiers (OTA) are designed using advanced filter design techniques which provide full integration. The implementations are compared in terms of noise performance, power consumption, total harmonic distortion (THD) and dynamic range (DR) in order to examine which is the most preferable in readout applications. Analysis is supported by simulations results in a 0.6µm process by Austria Mikro Systeme (AMS).

Keywords — operational transconductance amplifier, readout system, shaper, leapfrog, LC ladder.

I. INTRODUCTION

Nuclear radiation detection has been developed in the last few years in various fields of radioactivity control, high energy physics, space science, medical applications and so on. Solid state detectors are gaining importance in a variety of Xrays detection applications that demand excellent resolution. These detectors require compact, low cost and low noise electronics with a high number of channels. Several motivations suggest that the most of these applications can benefit from the use of ASIC (single application specified integration circuit) readouts instead of discrete solutions. Continuous efforts were performed in order to implement readout systems in monolithic form. CMOS technologies have been chosen due to the high integration density, relatively low power consumption and capability to combine analog and digital circuits on the same chip [1]-[3].

The preamplifier - shaper structure is commonly adopted in the design of the above systems. Semi-Gaussian (S-G) shapers are the most common pulse shapers employed in readout electronics [4], [5]. The above typical voltage mode architecture was sufficiently studied (mainly in terms of the CSA input transistor for noise reduction [6]-[9]) but few studies have been performed on pulse shapers and especially

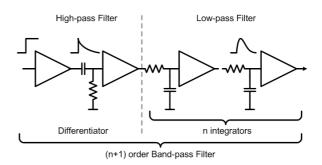


Fig. 1. Principal diagram of an n order voltage mode Semi-Gaussian shaper.

on current mode designs. After all, many current mode preamplifiers were so far suggested [10], [11]. This is due to the fact that a current mode structure could be an attractive alternative to the more typical voltage mode one, since the signal is processed in the current domain, avoiding charging and discharging of the parasitic capacitance to high voltage levels and keeping the internal nodes of the circuit at low impedance values.

In this work, current mode S-G shaper designs based on operational transconductance amplifiers (OTA) are proposed. Advanced filter design techniques [12], [13] which provide full integration, are used and novel CR-RC² implementations are suggested. All the implementations are compared in terms of noise performance, power consumption, total harmonic distortion (THD) and dynamic range in order to conclude which the optimum one is.

II. DESIGN OF OTA BASED SHAPERS

A semi-Gaussian shaper principal schema is shown in Fig.1. A high-pass filter (HPF) sets the duration of the pulse by introducing a decay time constant. The low-pass filter (LPF), which follows, increases the rise time to limit the noise bandwidth. Although pulse shapers are often more sophisticated and complicated, the CR-RCⁿ shaper contains the essential features of all pulse shapers, a lower frequency bound and an upper frequency bound and it is basically a (n+1) order band pass filter (BPF), where *n* is the integrators number (n is called shaper order). The transfer function of an S-G pulse shaper consisting of one CR differentiator and nintegrators is given by:

¹T. Noulis is with Electronics Laboratory of Physics Department, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece, e-mail: tnoul@physics.auth.gr.

C. Deradonis is with Electronics Laboratory of Physics Department, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece.

³S. Siskos is with Electronics Laboratory of Physics Department, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece, e-mail: siskos@physics.auth.gr.

$$H(s) = \left(\frac{s\tau_d}{1+s\tau_d}\right) \left(\frac{A}{1+s\tau_i}\right)^n = H(s)_{BPF}$$
(1)

where τ_d is the time constant of the differentiator, τ_i of the integrators, and *A* is the integrators dc gain. The number *n* of the integrators is called shaper order. Peaking time is the time that shaper output signal reaches the peak amplitude and is defined by $\tau_s = n\tau_i$. The order *n* and peaking time τ_s , depending on the application, can be predefined by the design specifications or not.

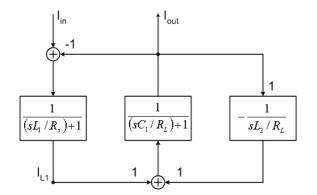


Fig. 2. Signal flow graph of a current mode 3rd order RLC filter.

 TABLE I

 Shapers Passive Elements and Transconductances

LC Ladder		Leapfrog		Cascade	
Rs	100 kΩ	C_1	11.8 pF	R_1	11 kΩ
R _L	100 kΩ	C ₂	13.3 pF	C_1	4.2 pF
C ₁	11.7 pF	C ₃	3.7 pF	R_2	100 kΩ
C ₂	11.7 pF	g _{m1}	11.4 µA/V	C_2	5 pF
C ₃	11.7 pF	g _{m2}	24 µA/V	R ₃	100 kΩ
g _{m1}	24 µA/V	g _{m3}	500.4 nF	C ₃	5 pF
g _{m2}	500.4 nA/V			g _{m1}	37.8 μA/V
				g_{m2}	500.4 nF

Using the above shaper model and the respective passive RLC equivalent two port circuit, the signal flow graph (SFG) of a 2^{nd} order current mode S-G shaper is extracted (Fig. 2). From the above SFG and using the Leapfrog (LF), the Ladder simulation method by element replacement and the typical cascade filter technique, three 2^{nd} order shapers are designed. The basic circuit block of all three shapers is an operational transconductance amplifier (OTA). Figs. 3, 4 and 5 show the LC ladder shaper with simulation by element replacement, the leapfrog shaper and the OTA based cascade method shaper

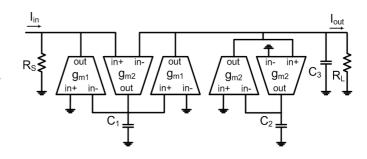


Fig. 3. OTA based LC ladder shaper using simulation by element replacement.

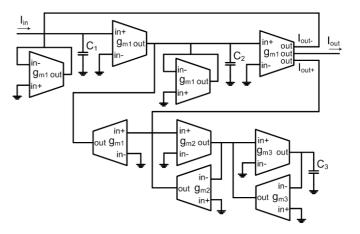


Fig. 4. OTA based leapfrog shaper with capacitance simulator.

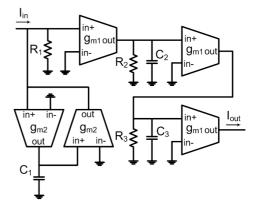


Fig. 5. OTA cascade method shaper with inductor simulator.

respectively. An OTA based inductance and a capacitor simulator are used in the cascade OTA shaper and the LF shaper respectively, in order to implement fully integrated systems [14].

The passive elements and the OTA transconductances of all the above configurations are given in Table I.

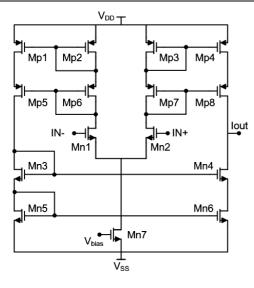


Fig. 6. CMOS operational transconductance amplifier.

III. SIMULATION RESULTS

A typical CMOS operational transconductance amplifier was designed in order to implement the above shaper structures. The respective OTA schematic is shown in Fig. 6. This OTA is implemented using a CMOS configuration with a cascode structure [15].

The OTA based shapers were designed in order to provide the same operating bandwidth (BW) at 230 kHz. Their frequency response is given in Fig. 7. The difference of the output current amplitude signal and in particular the lower gain of the LC Ladder and the Leapfrog structures is caused by the fact that the specific filter design methods reduce the output signal amplitude by half.

The total performance characteristics of each shaper system are listed in Table II.

The higher maximum bias current is observed in the OTA cascade shaper and the lower minimum in almost the same in all three configurations. All the shapers appear to be low power, but the LC Ladder shaper provide the optimum power consumption performance. Additionally, the cascade and the LF structure provide a dynamic range equal to 22 dB, far lower to the 32 dB value of the LC Ladder topology. Concerning the noise performance, all the structures appear to have low rms output noise, with the cascade shaper being slightly worse in comparison to the other two. The above characteristics, and in relation to the fact that the LC Ladder architecture is the optimum in terms of the total harmonic distortion, render it suitable for applications where the DR is required to be very high, and the noise and power consumption limits are the main factors that determine the application as in the readout front ends.

Fig. 8 shows the signal to noise ratio of the three OTA based shapers.

 TABLE II

 OTA Based Shapers Performance Characteristics

	Cascade	Leapfrog	LC Ladder
Maximum bias current	35.8 µA	4.7 μΑ	2.2 μΑ
Minimum bias current	83.6 nA	83 nA	83.5 nA
Power consumption	787 µWatt	648 µWatt	133 µWatt
$i_{in,peak-40dB}$ (THD = 1%)	1.3 µA	1.6 µA	8.4 μΑ
Output noise (rms)	77 nA	71 nA	71 nA
Dynamic Range (DR)	22 dB	22 dB	32 dB

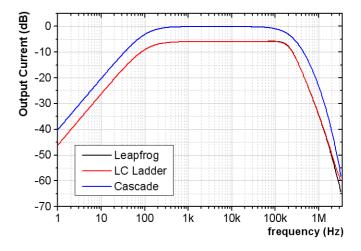


Fig. 7. Shapers frequency response.

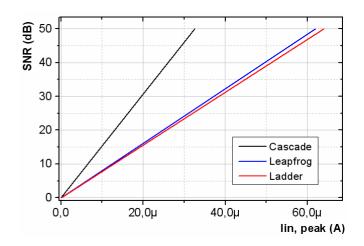


Fig. 8. Shapers signal to noise ratio.

IV. CONCLUSION

In this paper, a detailed examination of OTA based semi-Gaussian shapers suitable for readout applications is performed. Specifically, three different current mode shaper structures are designed using advanced filter design methods such as the Leapfrog and the Ladder LC technique by element replacement. All the methods used in this work provide fully integrated configurations and not discrete systems. An OTA was designed in order to be used in the implementation of the above shapers. The filter configurations are analytically compared in relation to power consumption, total harmonic distortion, dynamic range and noise performance. The OTA LC Ladder architecture is proved to be the optimum in low energy radiation detection applications, according mainly to its output noise and power consumption. Consequently, the LC Ladder method is the most suitable in order to design the shaper of an integrated readout front end system in which a current mode preamplifier is used.

REFERENCES

- B. Kriger, I. Kipnis, B. A. Ludewigt, "XPS: A multi-channel preamplifier-shaper IC for X-ray spectroscopy", *IEEE Transactions on Nuclear Science*, vol. 45, no. 3, pp. 732-734, June 1998.
- [2] M. Pedrali-Noy et al., "PETRIC a positron emission tomography readout integrated circuit", *IEEE Transactions on Nuclear Science*, vol. 48, no. 3, pp. 479-483, June 2001.
- [3] B. Krieger et al., "An 8x8 pixel IC for X-ray spectroscopy", *IEEE Transactions on Nuclear Science*, vol. 48, no. 3, pp. 493-497, June 2001.
- [4] Erik H. M. Heijne, Pirre Jarron, "A low noise CMOS integrated signal processor for multi-element particle detectors", *Digest of Papers ESSCIRC*, pp. 68-69, 1988.

- [5] F. S. Goulding, D. A. Landis, "Signal processing for semiconductor detectors", *IEEE Transactions on Nuclear Science*, vol. NS-29, pp. 1125-1141, June 1982.
- [6] W. Sansen, Z. Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology", *IEEE Transactions on Circuits and Systems*, vol. 37, no. 11, pp. 1375-1382, November 1990.
- [7] Z. Y. Chang, W. Sansen, "Effect of 1/f noise on the resolution of CMOS analog readout systems for microstrip and pixel detectors", *Nuclear Instruments and Methods in Physics Research*, vol. 305, pp. 553-560, 1991.
- [8] T. Noulis, S. Siskos, G. Sarrabayrouse, "Analysis of input and feedback capacitances effect on low noise preamplifier performance for X rays silicon stripe detectors", 19th Conference on Design of integrated circuits and systems, Bordeaux, France, November 24-26, 2004.
- [9] T. Noulis, S. Siskos, G. Sarrabayrouse, "Effect of technology on the input transistor selection criteria of a low noise preamplifier", *IEEE Mediterranean Electrotechnical Conference*, Dubrovnik, Croatia, May 12-15, 2004.
- [10] J. Wulleman, "Current mode charge pulse amplifier in CMOS technology for use with particle detectors", *Electronics Letters*, vol. 32, No. 6, pp. 515-516, March 1996.
- [11] Fei Yuan, "Low voltage CMOS current-mode preamplifier: Analysis and design", *IEEE Transactions on Circuits and Systems*, vol. 53, no. 1, pp. 26-39, January 2006.
- [12] T. L. Deliyannis, Yichuang Sun, Kel Fidler, Continuous-time Active Filter Design, Florida, CRC Press LLC, 1999.
- [13] R. Schaumann, Mac.E van Valkenburg, *Design of Analog Filters*, New York, Oxford, Oxford University Press, 2001.
- [14] R. Senani, "Novel lossless synthetic floating inductor employing a ground capacitor", *Electronics Letters*, vol. 18, no. 10, pp. 413-414, May 1982.
- [15] T. Noulis, C.Deradonis, S. Siskos, G. Sarrabayrouse, "Novel fully integrated OTA based front end analog processor for X – rays silicon strip detectors", accepted for publication to 13th *IEEE Mediterranean Electrotechnical Conference*, Malaga, Spain, May 16-19, 2006.