A Space Application Current Mode CMOS Low Noise Preamplifier for X-rays Detection System

T. Noulis[1] and S. Siskos[2]

Abstract — **A systematic design guideline is presented for the noise optimization of a current mode CMOS preamplifier suitable for space applications X-rays silicon strip detectors. A novel current architecture preamplifier is implemented using a third generation current conveyor. The preamplifier implementtation is designed in AMS 0.35 μm process. Analysis is supported by simulation results, which confirm its great performance mainly in terms of the total output noise and the power consumption. This current structure appears to be preferable to the typical voltage one due to its lower noise performance and its noise independence on the detector capacitance variations.**

Keywords — **current mode, low noise preamplifier, X-rays detection system.**

I. Introduction

Radiation detection has been increasingly developed in various fields of radioactivity control, medical imaging and space science. In X-rays detection front-end systems CMOS technologies are widely used since they ensure the required integration density and seem very promising in terms of radiation hardness. A block diagram of such a detection system is shown in Fig. 1. A reversely biased diode (Si or Ge) detects radiation events by generating electron–hole pairs proportional to the absorbed energies. A low noise charge sensitive preamplifier (CSA) is widely used at the front end due to its low noise configuration and insensitivity of the gain to the detector capacitance variations. The generated charge Q is integrated onto a feedback capacitance. This is fed to a bandpass filter (shaper) where pulse shaping is performed to optimize the signal to noise (S/N) system ratio. The resulting output signal is a narrow pulse suitable for further processing [1], [2].

The noise performance of the amplification stage determines the overall system noise and should be therefore optimized. A voltage mode folded cascode architecture is commonly used because of its low input capacitance [1]-[5]. However, a current mode structure could be an attractive alternative to the more typical voltage mode ones, since the signal is processed in the current domain, avoiding charging and discharging of the parasitic capacitance to high voltage levels and keeping the internal nodes of the circuit at low impedance values.

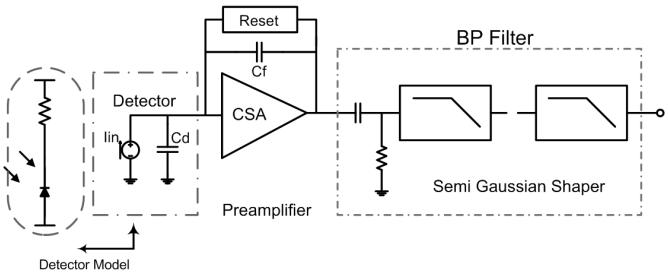

Fig. 1. Block diagram of a front-end readout system.

In this work, a current mode preamplifier configuration is proposed. A CMOS third generation current conveyor (high gain current conveyor CCII∞) is designed and noise minimization techniques are presented in order to achieve optimum noise performance.

II. Noise Minimization Techniques

A current mode preamplifier can be implemented using a current conveyor and particularly a high gain one (CCII∞). The input stage of almost all current mode feedback amplifiers is either a positive or a negative second generation current conveyor [6], [7]. Therefore, a conveyor noise model (Fig. 2) can be used to simplify noise calculations. The noise sources in a dual output MOS CCII∞ are shown in Fig. 3, where the only MOSFETs not included in the conveyor noise model are the output stage transistors (M1, M2, MSS1 and MSS2).

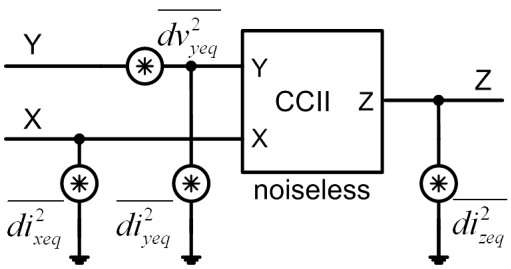

Fig. 2. Equivalent noise sources of a second generation current conveyor.

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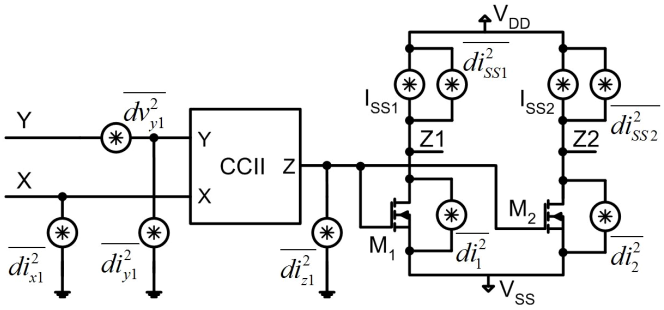

Fig. 3. Noise sources in a dual output MOS high gain current conveyor.

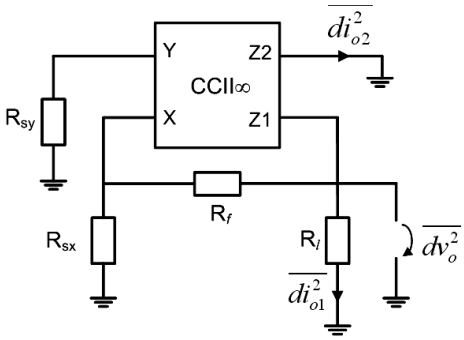

Fig. 4. Noise test set-up for a dual output high gain current conveyor.

By using the circuit configuration of Fig. 4, the noise of most high gain current conveyor applications can be evaluated. Since the closed loop input impedance at the X-terminal is in most cases significantly lower than R_{sx}, the output noise voltage $\overline{dv_o^2}$ at the Z1-output can be approximated at low frequencies as:

$$\overline{dv_o^2} \approx \left(1+\frac{R_f}{R_s}\right)^2\left(\overline{dv_{y1}^2}+R_{sy}^2\,\overline{di_{y1}^2}+4kTR_{sy}df\right) + R_f^2\left(\overline{di_{x1}^2}+\overline{di_{z1}^2}+\frac{4kT}{R_{sx}\|R_f}df\right) + \frac{R_f^2}{\left(1+G_i+\frac{R_f}{R_l}\right)^2}\left(\overline{di_1^2}+\overline{di_{SS1}^2}+\frac{4kT}{R_f\|R_l}df\right) \quad (1)$$

where k is the Boltzmann constant and T is the temperature.

In high gain current conveyors the open-loop current gain G_i is high and therefore noise contribution of output transistors (M1 and MSS1) can be neglected unless very high frequencies are considered. If the output current noise is required, it can be obtained by letting:

$$\overline{di_{o1}^2}=\frac{\overline{dv_o^2}}{R_l^2} \quad (2)$$

Contrary, the replica output is outside the feedback loop and transistors M2 and MSS2 noise contribution can not be neglected, and thus the output current noise is:

$$\overline{di_{o2}^2}=\frac{\overline{dv_o^2}}{\left(R_f\|R_l\right)^2}+\overline{di_2^2}+\overline{di_{SS2}^2} \quad (3)$$

Because the replica output is typically used in the closed loop current conveyor configuration without resistive feedback, the output noise current is given by:

$$\overline{di_{o2}^2}=G_{icl}^2\left(\overline{di_{x1}^2}+\overline{di_{z1}^2}+\overline{di_1^2}+\overline{di_{SS1}^2}\right)+\overline{di_2^2}+\overline{di_{SS2}^2} \quad (4)$$

where G_{icl} is the closed loop current gain depending on the aspect ratios of the output transistors. As a result, the output transistors (M2 and MSS2) noise contribution is more significant whereas the conveyor input voltage noise is omitted. This situation differs from the normal one with high gain voltage mode opamps where normally only input transistors noise needs to be considered. Consequently, the noise model for a high gain current conveyor should also include output current noise sources, as depicted in Fig. 5 [7]. In this model, the equivalent noise sources at Y-terminal are identical to the noise sources of the input CCII-. However, the remaining noise sources are divided between the X-terminal and the two Z-outputs accordiong to the following equations:

$$\overline{di_{xeq}^2}=\overline{di_{x1}^2}+\overline{di_{z1}^2} \quad (5)$$

$$\overline{di_{zeq1}^2}=\overline{di_1^2}+\overline{di_{SS1}^2} \quad (6)$$

$$\overline{di_{zeq2}^2}=\overline{di_2^2}+\overline{di_{SS2}^2} \quad (7)$$

A simple optimization technique in order to design a low noise current conveyor implies the use of conveyors with a current gain from node X to node Z, since this reduces the ouput transistors noise contribution and can be controlled in current mode opamps. It would also be essential to design low g_m current mirror structures, high g_m structures for the X input stage and the Y to X level shifter stage.

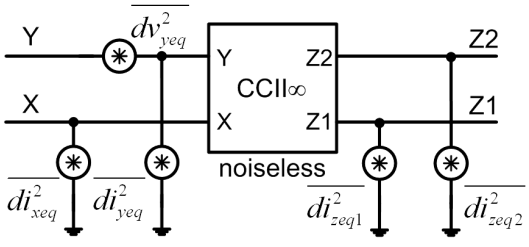

Fig. 5. The equivalent noise sources of a multi-input high gain current conveyor.

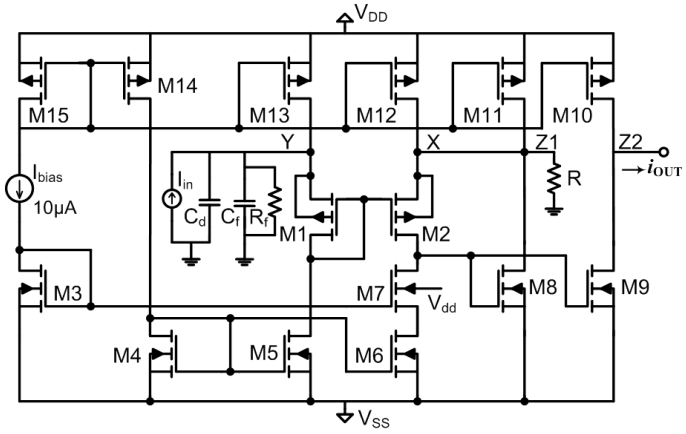

Fig. 6. Preamplifier current mode implementation with a high gain current conveyor.

III. Design of Low Noise Preamplifier

The preamplifier integrates the input signal from a silicon strip detector. The circuit has to be designed to work with current (dc) couple detectors and should be able to supply a current in the range from a few picoamperes to a few nanoamperes through the feedback loop in order to match the detector leakage current.

The current mode preamplifier using a CCII∞ implementation with an n-well CMOS process is shown in Fig.6. This conveyor uses an input voltage follower structure typical to class-A second generation positive current conveyors [8], [9]. The input voltage follower is implemented with PMOS transistors M1, M2 and the input voltage swing can be maximized by using floating n-wells for these transistors. Since the offset voltage between Y- and X-terminals remains minimal, this high gain conveyor can be used as a drop-in replacement for voltage mode operational amplifier [7]. In certain applications, the input impedance may be too low. Its performance can be improved by using cascode current sources rather than the transistors M5, M13 and M12. This high-gain conveyor has two current outputs Z1 and Z2. A CCII+ structure is implemented from this amplifier by connecting the Z1 output to X-terminal. When only one current output is needed, the output current swing can be doubled by joining the two outputs together. In order the circuit to operate as a non-inverting loss integrator a feedback capacitor C_f is connected in parallel with a resistor R_f in node Y and a resistor R is connected between node X and the ground. This circuit design was based on the respective noise optimization criteria described above.

The above preamplifier circuits have been designed for a low energy X-rays strip detector for space applications. The design specifications are listed in Table I.

TABLE I
Design Specifications

Detector Diode PIN (Si) – Preamplifier	
Detector capacitance	C_d =2 - 5 pF
Leakage current	I_{leak} = 10 pA
Q collected per event	$Q_{typical}$=28000e$^-$ Q_{max}=300000e$^-$
Time needed for 90% of total Q	300 nsec
Temperature	-40^0 C
Power consumption per channel	< 8 mW

IV. Simulation Results

The preamplifier configuration was simulated using HSPICE (BSIM3V3.2 Level 49) and designed in 0.35 μm process by Austria Micro Systeme (AMS). Voltages V_{DD} and V_{SS} are 2.5 V and -2.5 V respectively, feedback capacitance C_f was 10 pF, R_f and R were 5 kΩ and 25 Ω. The bias current I_{bias} was selected to be 10 μA in order to achieve lower noise performance. The current output signal of the CCII∞ preamplifier implementation is shown in Fig. 7. The fact that the current CSA output signal is not inverted does not complicate the signal processing, since the use of a respective CCII current mode shaper structure (with inverting Z- and non-inverting Z+ outputs) would provide a more flexible system design. Table II summarizes the performance of the circuit.

TABLE II
Performance Characteristics

	Current Preamplifier
Charge time	200 ns
Discharge time	0.46 μs
Power consumption	2.5 mW
Gain	45 dB
fp	1.92 MHz
enc_{total}/τ_s =10μs C_d = 2pF	28 e$^-$
Charge time	200 ns

As it seems from Fig. 7 the preamplifier output increases to a maximum value when the charge of the feedback capacitance ends. Charge time (collection of input signal by CSA) is very low, which proves that the circuit is fast enough to perceive signals of 300 ns. The discharge time is also relatively very low since in this application, two successive events have a time distance of about 1 ms. The requested power consumption limits are also satisfied since the current mode preamplifier consumes 2.5 mW, providing the shaper the capability to consume 5.5 mW. The CCII∞ opamp, appears to have lower gain performance in relation to typical voltage configurations but in a much more wider bandwidth. Moreover the current mode CSA has very low *enc*. Fig. 8 shows the noise spectral density of the current configuration.

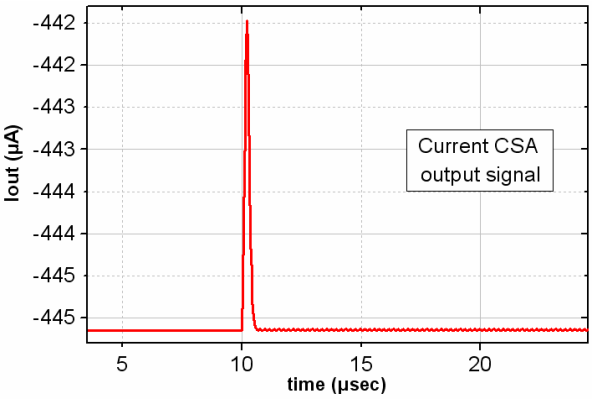

Fig. 7. Current mode preamplifier output signal.

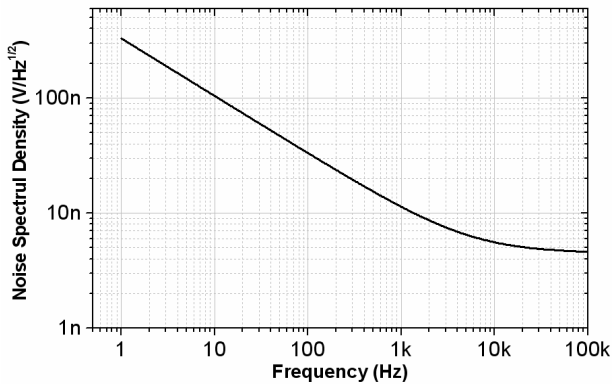

Fig. 8. Preamplifier noise spectral density.

Furthermore, a study was made as to examine and contrast the dependence of noise performance on the detector capacitance. It was calculated that in a current mode CSA the total *enc* (detector readout system noise performance is expressed as the equivalent noise charge (*enc*) [1], [2]) is constant with C_d. Specifically, this corresponds to a constant equivalent noise charge of 28 e^- at a detector with a capacitance of 2 pF.

V. Conclusion

In this paper, a noise optimization technique for a current mode preamplifier was presented. In particular, low noise design criteria were applied for the first time in a current mode structure suitable for X-rays detection systems. It is confirmed by simulations that with a current mode preamplifier very low *enc* levels can be provided. Moreover, a great advantage of the current mode configuration is the opportunity to implement analog systems with high speed and wider frequency bandwidth. It is also noticeable that the detector capacitance increase does not result to higher noise performance, as it happens with the typical voltage mode architecture. However, it should not be neglected that the amplification gain performance appears to be worse in relation to the typical folded cascode architecture. The above factor renders the current mode preamplifier optimum especially for large capacitance detection applications.

References

[1] Z. Y. Chang, W. Sansen, "Effect of 1/f noise on the resolution of CMOS analog readout systems for microstrip and pixel detectors," *Nuclear Instruments and Methods in Physics Research*, vol. 305, pp.553-560, 1991.

[2] W. Sansen, Z. Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology", *IEEE Transactions on Circuits and Systems*, vol. 37, no. 11, pp.1375-1382, November 1990.

[3] T. Noulis, S. Siskos, G. Sarrabayrouse, "Analysis of input and feedback capacitances effect on low noise preamplifier performance for X rays silicon stripe detectors", *19th Conference on Design of Integrated Circuits and Systems*, Bordeaux, France, November 24-26, 2004.

[4] E. F. Tsakas, A. N. Birbas, "Noise optimisation for the design of a reliable high speed X-rays readout integrated circuit", *Microelectronics Reliability*, vol. 40, pp. 1937-1942, February 2000.

[5] T. Noulis, S. Siskos, G. Sarrabayrouse, "Effect of technology on the input transistor selection criteria of a low noise preamplifier", *IEEE Mediterranean Electrotechnical Conference*, Dubrovnik, Croatia, May 12-15, 2004.

[6] E. Bruun, "Analysis of the noise characteristics of CMOS current conveyors", *Analog Integrated Circuits and Signal Processing*, vol.12, pp. 71-78, 1997.

[7] K. Koli, *CMOS Current Amplifiers: Speed Versus Nonlinearity*, Finland, Helsinki University of Technology, 2000.

[8] D. Johns, K. Martins, *Analog Integrated Circuit Design*, New York, Wiley Interscience Publications, 1997.

[9] K. Koli, K. Halonen, "Inverting transimpendence amplifier for current- and voltage-mode applications", *Proceedings of the 11th European Conference on Circuit Theory and Design*, Davos, August 1993.