

R-2R Digital-to-Analog Converter: Analysis and Practical Design Considerations

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Abstract – The following article is an attempt to describe the rudiments of R-2R structures in reverse connection and their application in D/A converters.

Analysis of R-2R ladders is made simple and intuitive by using Thevenin equivalent circuits. Formulae expressing all the basic properties of R-2R structures are derived using this approach. Practical design considerations are also discussed in great detail. To prove the theoretical analysis, test structures are designed and fabricated in 1.0 μm and 0.6μm double-poly, double-metal CMOS processes. Experimental results are then analyzed.

Keywords – ADC, R-2R, mixed-signal, CMOS

I. INTRODUCTION

R-2R structures of digital-to-analog converters (DAC) are very popular for their simplicity. For a DAC with a resolution of N bits 2N+1 resistors and 2N switches are necessary. In addition, only two resistor values are needed: R and 2R. Moreover, since 2R=R+R (and vice versa: R=2R//2R), only one resistor value is actually required. Thus the entire R-2R ladder is implemented as an array of equal resistors.

There are two basic types of R-2R DACs [1] [2] [3]:

- current mode (current steering).
- voltage mode (R-2R ladder in inverse connection).

The current mode DAC has been considered as the traditional approach. In this approach, the R-2R ladder is used to produce a set of binary-weighted currents whose sum is then converted to voltage (Fig. 1)

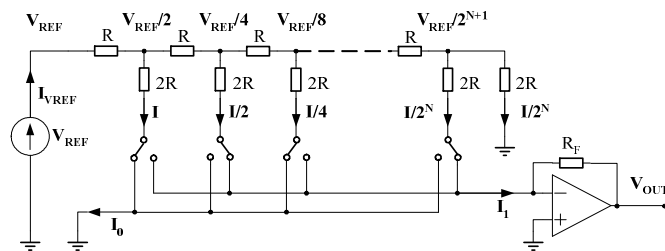


Fig. 1. Current mode R-2R DAC

The voltage at the output of the current-mode DAC is Eq. 1:

$$V_{OUT} = -R_F \times \sum_{k=0}^{2^n-1} I_k = -V_{REF} \times \frac{R_F}{2R} \times D \quad (1)$$

Where D is the digital word applied to the converter:

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$$D = (b_{N-1} \times 2^{N-1}; b_{N-2} \times 2^{N-2}; \dots; b_1 \times 2^1; b_0 \times 2^0)$$

An important disadvantage of the current mode R-2R structures is the need for an operational amplifier that performs the current-to-voltage conversion.

The opamp itself introduces errors such as offset voltage, limited slew rate, limited output swing, etc.

The output of the voltage-mode R-2R DAC is voltage, so no opamp is needed provided the load impedance is high enough, which is usually the case in CMOS circuits.

In this article, the long-neglected voltage-mode R-2R DAC is discussed in some more detail. Expressions are derived for all the basic properties of the R-2R ladders by means of Thevenin equivalent circuits. The emphasis is on the practical design considerations and design methodology.

The rudiments of R-2R ladder in voltage mode are discussed in Section II.

Errors and error sources are dealt with in Section III. Experimental results are given in Section IV.

II. THE VOLTAGE-MODE R-2R DAC

Fig. 2 shows a network of N cascaded R-2R links, numbered from 0 to N-1.

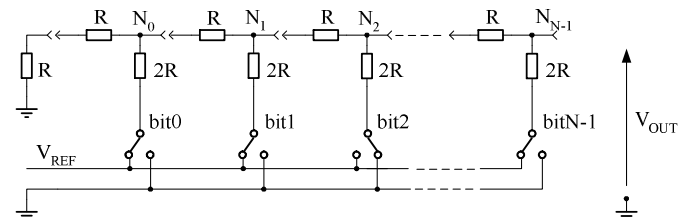


Fig. 2. The voltage mode R-2R DAC

Note that in contrast to the current-steering ladder, the basic R-2R links are connected in reverse order.

A terminating resistor of value R is connected to the leftmost link (numbered 0), so that the equivalent impedance seen to the left each link is exactly R and the equivalent impedance seen at the output node V_{N-1} is also R.

The Thevenin equivalent circuit for an arbitrary R-2R link is shown in Fig. 3

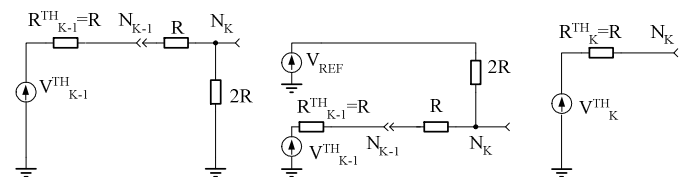


Fig. 3. Thevenin equivalent circuit of the voltage mode R-2R DAC

For an arbitrary link K , the following expression holds:

$$V_K^{th} = \frac{V_{N-1}^{th}}{2} + bit_K \times \frac{V_{REF}}{2} \rightarrow \text{for...} bit_K \in (0,1) \quad (2)$$

The index “th” stands for “Thevenin” equivalent circuit. Applying this recurrent formula to the entire chain of N basic links, numbered from 0 to $N-1$, yields the voltage at the last node (the output of the DAC) Eq. 3

$$\begin{aligned} V_{OUT} &= V_{N-1} = b_{N-1} \times \frac{V_{REF}}{2^1} + b_{N-2} \times \frac{V_{REF}}{2^2} + \dots + b_0 \times \frac{V_{REF}}{2^N} \\ &= \frac{V_{REF}}{2^N} \times D \end{aligned} \quad (3)$$

where D is the digital code applied:

$$D = (b_{N-1} \times 2^{N-1}; b_{N-2} \times 2^{N-2}; \dots; b_1 \times 2^1; b_0 \times 2^0).$$

In summary, the entire R-2R ladder can be replaced with a Thevenin equivalent circuit with equivalent open-circuit voltage V_{OUT} and output impedance Z_{OUT} , Eq (4):

$$\begin{aligned} V_{OUT} &= \frac{V_{REF}}{2^N} \times D \\ Z_{OUT} &= R \end{aligned} \quad (4)$$

Power consumption

A point worth mentioning is that in contrast to the current-mode R-2R ladder, the power consumption of the voltage-mode R-2R ladder is not constant but varies with the code applied.

For all bits = “0” power consumption is also zero (all 2R resistors are connected to GND). When only one bit is “1” the consumption is $V_{REF}/3R$. Maximum consumption occurs at codes 010101...01 and 101010...11 (Fig. 4)

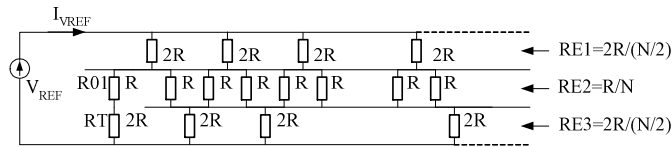


Fig. 4. The load applied to the reference source

If the number of R-2R links (i.e. number of bits) is large enough, the problem can be simplified by assuming that the contribution of the resistors R_{01} and R_T is negligible in comparison to all the other resistors. Then all nodes across lines A-A and B-B would be at potentials V_A and V_B respectively. Thus the impedance seen by the reference is:

$$R_E = \frac{2R \times 2}{N} + \frac{R}{N} + \frac{2R \times 2}{N} = \frac{9R}{N} \quad (5)$$

And the current flowing out of the reference is:

$$I_{VREF} = \frac{V_{REF}}{R_E} = V_{REF} \times \frac{N}{9R} \quad (6)$$

This formula is accurate if the number of bits is large enough. For N more than or equal to 8 bits the error is less than 10%.

The power consumed from the digital supply is actually zero, since no current flows through the switch gates.

III. ERROR SOURCES IN VOLTAGE-MODE R-2R DAC

Effects of tolerances and device mismatch

Device mismatch is the major source of error in any DAC. The stochastic matching between two identically designed resistors is defined as the standard deviation of the normal distribution for the relative difference δ_R .

$$\delta_R = \frac{\Delta R}{R} \quad (7)$$

The matching of two identically designed resistors with size $W \times L$ is described by the following model [4]:

$$\delta_R = \frac{A_R}{\sqrt{W \times L}} \quad (8)$$

where A_R is a process-dependent matching parameter.

The influence of device mismatch of each R-2R link increases as its rank in the ladder increases. The Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL) are likely to reach their maximum around the major carry points that involve the most significant bit (i.e transitions like 0111...111 \rightarrow 1000...000). The worst case occurs when all resistors are at their minimum (maximum) values and only the 2R resistor of the most significant bit (b_{N-1}) is at its maximum (minimum) value.

$$\begin{aligned} R &= R - \Delta R = R(1 - \delta_R) \\ 2R_{BITN-1} &= 2(R + \Delta R) = 2R(1 + \delta_R) \end{aligned} \quad (9)$$

The equivalent Thevenin circuit is shown in Fig. 5

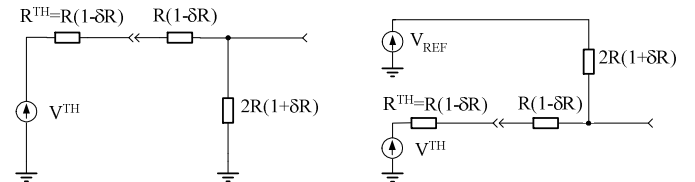


Fig. 5. The effect of device mismatch

Using this circuit the absolute values of DNL and INL can be expressed in terms of least-significant bits:

$$DNL = 2^N \times \delta_R \quad (10)$$

$$INL = 2^{N-1} \times \delta_R \quad (11)$$

Switch imperfection

a) On-resistance of closed switches. The on-resistance of a closed switch adds to the resistance of the corresponding 2R resistor. That is, its actual value becomes $R_a = 2R + R_{ON}$. Since the value of R resistors is not affected by switches, the actual division ratio of the basic R-2R link changes, resulting in integral and differential nonlinearity.

The equivalent Thevenin circuit with R_{ON} included is shown in Fig. 6.

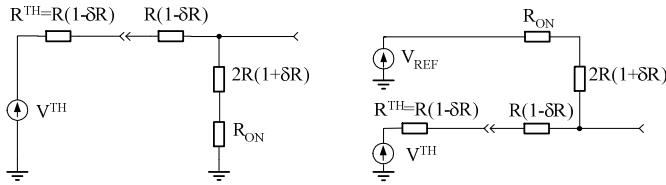


Fig. 6 – The influence of the switches

With R_{ON} included, the expressions for DNL and INL are (in terms of LSB):

$$DNL = 2^N \times \left(-\delta_R - \frac{R_{ON}}{4R} \right) \quad (11)$$

$$INL = 2^N \times \left(\frac{4R \times \delta_R - R_{ON}}{8R + 2R_{ON}} \right) \quad (12)$$

Note that since δ_R can be either positive or negative, the first term in the brackets in Eq. (11) and (12) can also be either positive or negative. However, R_{ON} is always positive.

b) Switch leakage. Since every $2R$ resistor is connected either to V_{REF} or to GND, which are both low impedance nodes, the leakage currents flow into V_{REF} or into GND rather than into the resistor array. That is why switch leakage currents do not affect DAC performance provided the reference source is low ohmic. Tests of real devices show that the effect of switch leakage is negligible.

Poor layout

Poor layout can significantly spoil device matching, thus leading to INL and DNL. Straight-forward layout (devices in a row) is the simplest and most compact way to place a set of resistors. However, it is prone to process deviations along the wafer. A layout with one axis of symmetry can significantly compensate for process deviations along this axis. A layout which is symmetrical in respect to two axes of symmetry (common-centroid layout) can effectively compensate for the process deviations along both the horizontal and the vertical axes at the price of an increased die area and an elaborate interconnection scheme.

Influence of the reference source

As mentioned above, the current flowing out of the reference source varies with the digital code applied. The changes in the current consumed cause changes in the voltage drop across the output impedance R_I of the reference. These code-dependent voltage drops result in integral nonlinearity. The error caused by this parasitic voltage drop is:

$$\delta_{V_{REF}} = \frac{\Delta V_{REF}}{V_{REF}} = \frac{R_I(N-3)}{9R} \quad (13)$$

A fact which is often neglected at the layout phase is that the wires connecting the converter to the reference source and to ground also have parasitic resistance, which adds to the output impedance of the reference source.

Influence of the load impedance

As shown in Fig. 3 and Eq. 3, the voltage mode R-2R DAC can be represented by its equivalent Thevenin circuit, which has an open-circuit ideal voltage source and output impedance Z_O . When a finite load impedance Z_L is applied, the actual output voltage is:

$$V_{OUT} = V_{REF} \times D \times \frac{Z_L}{Z_L + Z_O} \quad (14)$$

All codes are attenuated by the same factor. That is, the finite load impedance causes an additional gain error expressed in Eq. 12

IV. EXPERIMENTAL RESULTS

The voltage-mode DAC shown in Fig. 2 was fabricated in $1.0 \mu\text{m}$ and $0.6 \mu\text{m}$ double-poly, double-metal CMOS processes. Several R-2R structures were prepared for a resolution of 12, 10 and 8 bits. To check the influence of the layout, three different layout schemes were employed for the 8-bit DAC. Every effort was made at the layout phase to ensure good device matching and to keep the lengths of the interconnecting wires equal. Tests were performed by means of a special test kit and a KEITHLY 2000 digital voltmeter. The test results are given in Fig. 7 – Fig. 10. The minimum measured values are in blue, the maximum measured values are in red. The increase of both INL and DNL at the major carry point is easily seen. Device mismatch is the major source of error in voltage-mode R-2R DAC. The errors of the converters are actually determined by the mismatch of the two most significant bits. As predicted by Eq. 10 and Eq. 11, for the same device mismatch, the DNL is (in terms of LSB) twice as big as INL. If DNL is higher than 1 LSB the conversion monotonicity is not guaranteed. The improvement of conversion linearity (both INL and DNL) for the symmetrical layouts (one axis of symmetry and common-centroid) as compared to the straightforward layout is partially due to the fact that in symmetrical layout schemes devices are split into several unit devices whose total area is larger than the area of the straight-forward layout. Test results are summarized in Table I:

TABLE I
MEASURED R-2R DAC NONLINEARITY

DAC type: process and layout scheme	INL [LSB]	DNL [LSB]
12-bit; $1 \mu\text{m}$ CMOS common-centroid layout	1,5	2,6
10-bit; $1 \mu\text{m}$ CMOS one axis of symmetry	0,6	1,1
8-bit; $1 \mu\text{m}$ CMOS one axis of symmetry	0,18	0,32
8-bit; $0,6 \mu\text{m}$ CMOS straightforward layout	0,11	0,22
8-bit; $0,6 \mu\text{m}$ CMOS one axis of symmetry	0,09	0,17
8-bit; $0,6 \mu\text{m}$ CMOS common-centroid layout	0,05	0,09

V. CONCLUSIONS

The voltage-mode R-2R DAC (R-2R in reverse connection) has been discussed in this article as an effective way to circumvent the problems associated with the opamp in current-mode R-2R DACs. Theoretical analysis using Thevenin equivalent circuits has been proposed that gives insight into the voltage-mode R-2R DAC operation. The derived expressions have been proved by means of design experiment. Experimental results agree with the formulae derived in Section II. Ways to reduce the INL and DNL by means of proper layout techniques have also been discussed in brief.

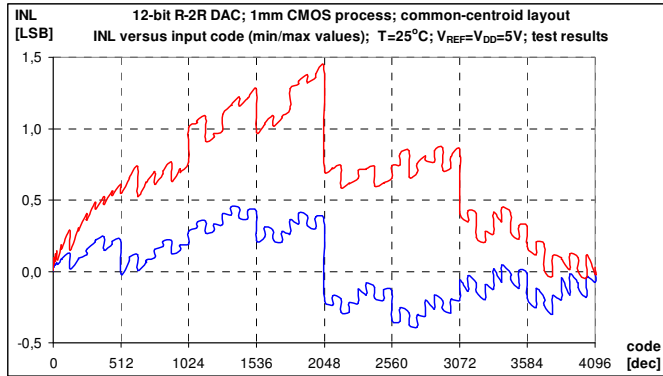


Fig. 7. INL of 12-bit R-2R DAC

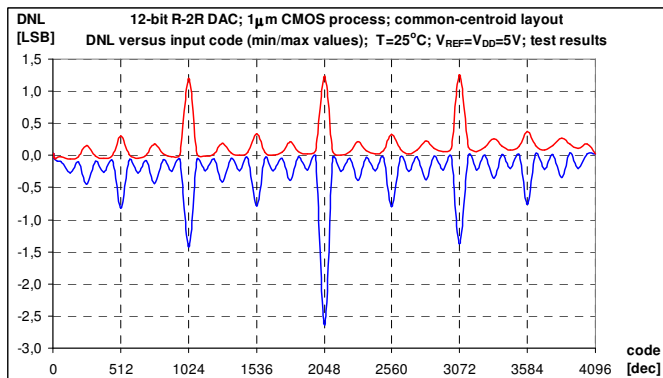


Fig. 8. DNL of 12-bit R-2R DAC

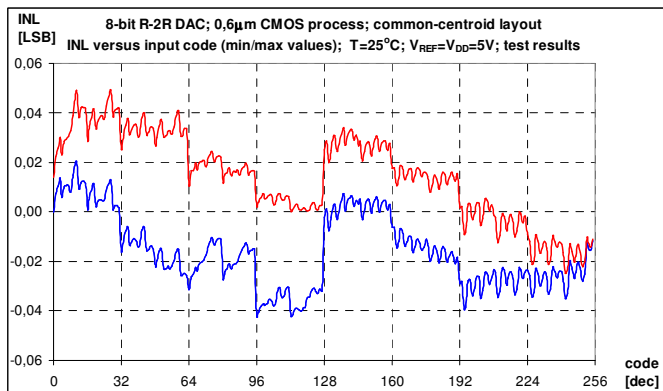


Fig. 9. INL of 8-bit R-2R DAC; Common-centroid layout

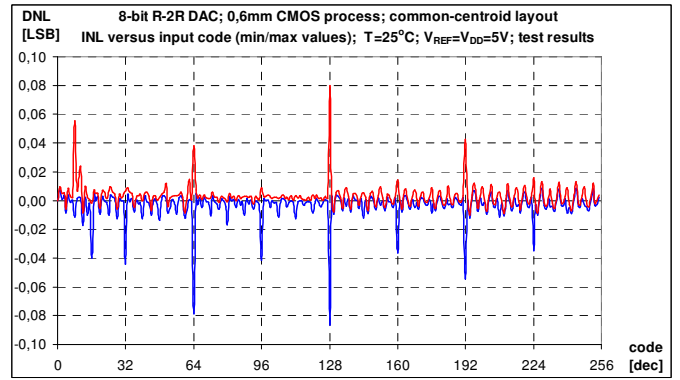


Fig. 10. INL of 8-bit R-2R DAC; Common-centroid layout

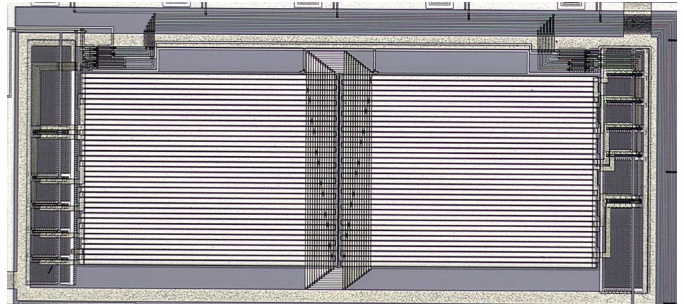


Fig. 11. Die photograph of 12-Bit DAC, 1µm CMOS process

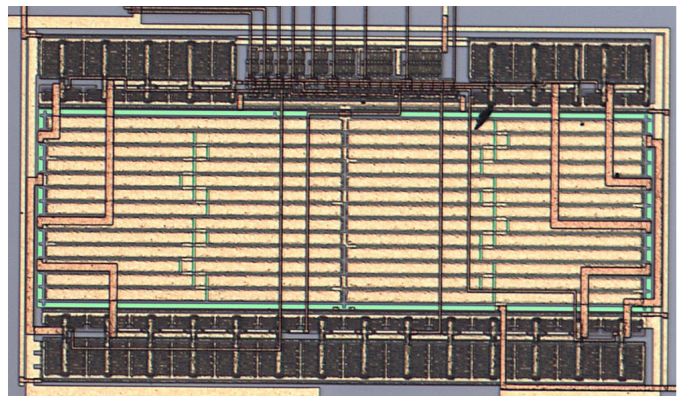


Fig. 12. Die photograph of 8-Bit DAC, 0.6µm CMOS process; Straight-forward layout

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