Model building and testing procedure – An analogue multiplexer SPICE macromodel improved with temperature effects

Ivailo M. Pandiev[1]

Abstract – **A systematic procedure to design a behaviour SPICE macromodels is described in this paper. The proposed modelling procedure can be split into three basic steps: 1) structuring the model; 2) build the model; 3) validate the model. Using this method, an improved SPICE macromodel of a CMOS analogue multiplexer is presented in which the temperature effect of a switch on-resistance is modelled. Also, for creating the simulation model, techniques known from modelling operational amplifiers have been adapted. The proposed macromodel allows the simulation of circuits with respect to the behaviour in both the time and frequency domains, including error parameters and the temperature dependence of switch on-resistance. Model parameters for the integrated circuit ADG408 from Analog Devices are extracted as an example. The simulation results are compared with manufacturer's data and good correspondence is reported.**

Keywords – **Analogue circuits, Temperature effects, CMOS analogue multiplexers, SPICE, Modelling.**

I. INTRODUCTION

The CMOS analogue multiplexers have become an essential component in the design of electronic systems which require the ability to control and select a specified transition path for the analogue signal. These analogue devices are widely used for implementing multi-channel amplifiers, sample-and-hold circuits and PGAs. [1-3].

The switch on-resistance (R_{ON}) is an important consideration in applying analogue multiplexers. When one of the switches is closed, DC-performance is affected mainly by on-resistance and leakage current. Also R_{ON} changes as a function of the temperature and from switch-to-switch. However, temperature variation of the switch on-resistance is not presented in the available behaviour SPICE macromodels of analogue multiplexers [4, 5]. The majority of published SPICE macromodels only attempt to model R_{ON} , usually by a fixed on-resistance model parameter, defined into the ideal model with voltage-controlled switches. They therefore cannot be used to simulate the dynamic variations in R_{ON} due to changing temperature. To solve this problem, here is proposed a design procedure for modelling temperature dependence of the on-resistance in the CMOS analogue multiplexer macromodels. Also, techniques described in [6-8] have been adapted for macromodelling the temperature effects.

[1]Ivailo M. Pandiev is with the Faculty of Electronics from Technical University of Sofia, Kliment Ohridski 8, 1000 Sofia, Bulgaria. E-mail: ipandiev@tu-sofia.bg

II. MACROMODEL BUILDING PROCEDURE

The macromodel building and testing procedure presented in this section is based on a Top-Down analysis approach and by applying simplification and build-up technique, known from modelling operational amplifiers [9-12].

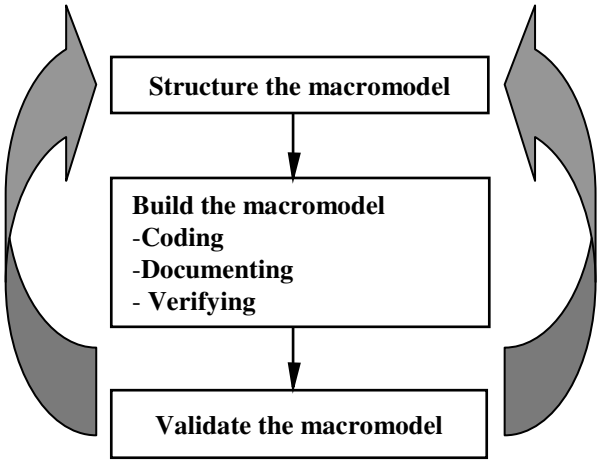

Fig. 1. Model building and testing procedure.

The process of model building and testing, as shown in Fig. 1, can be broken down into three steps: 1) structure the model; 2) build the model; 3) validate the model. Despite the fact that the process of model building is shown in a linear fashion, moving between structuring, building and validation of the model is a process that has iterative nature.

Each step of the procedure can be split into smaller steps which follow a similar iterative pattern. An outline of these steps can be resumed as follows.

1) The first step is to choose an internal structure for the model. The structure can be different from the actual structure of the IC. Also, the structure should consist of the elements that need to be defined and the data and logic, required to drive the model. It effectively is a paper version of the computer model.

2) The second step is the building of the model with the simulation software. This process consists of three distinct activities: coding, entering the model into the computer; documenting, explaining the model structure using software facilities and other techniques; verifying, ensuring that the code is correct. Each of these activities is performed in small steps, iteratively building and improving the model.

3) The last step is the validation of the macromodel. Validation is the process of determining whether a simulation model

is an accurate representation of the real system, for the particular objectives of the study. If a model is "valid", then it can be used to make decisions about the system similar to those that would be made if it were feasible and cost-effective to experiment with the system itself.

Validation is achieved by comparing the model predictions with actual experimental results or with data sheet parameters. For the goals of validation it is necessary to collect data that represents the average behavior of the real IC. It is important to check not only the average levels of those data, but also to compare their spread, applying the methods of statistical analysis and calculus probability.

III. BUILDING THE MACROMODELS SENSING TEMPERATURE EFFECTS OF THE SWITCH ON-RESISTANCE

The design procedure described in the previous section can be used to model second-order effects of the analogue multiplexers.

The analysis of switch on-resistance R_{ON} versus temperature at specified input signal level for different analogue multiplexers has shown that in most cases this electrical characteristic could be approximated by quadratic or exponential transfer function. Normally, semiconductor data books provided by IC-manufacturers contain electrical diagrams regarding the temperature dependence of the switch on-resistance that could be used in modelling the real devices.

The schematic diagram of the proposed macromodel is shown in Fig. 2. It's based on a previous analogue multiplexer macromodel [4] from standard SPICE library, with the additional capability to model the temperature effects of the switch on-resistance. The input switch section, decoder section and supply current section are implemented as behavioural models using ABM (Analogue Behaviour Modelling) technique and are represented in Fig. 2 as black-boxes marked 'demuxsw', 'scl' and 'pscc' respectively. The temperature dependence of the R_{ON} has been modelled by adding new elements into existing behaviour SPICE macromodels for analogue multiplexers as follows.

As it is shown in Fig. 2, a linear two-port voltage-controlled current source (VCCS) G_T is connected to the output section of the existing SPICE macromodel, creating a new node 88. The current through G_T will have to follow the change in the temperature. The temperature-dependent controlled voltage of the VCCS G_T comes from a separate stage in Fig. 2. This additionally defined temperature stage consists of an ideal current source I_T and a SPICE temperature-dependent resistor R_T, which is controlled with equation [13]:

$$R_T(T) = R_T(T_0)\left[1 + TC1(T - T_0) + TC2(T - T_0)^2\right] \qquad (1)$$

where $R_T(T_0)$ is the value of the resistor at $T_0 = 27°C$ (SPICE-Option TNOM), T is the temperature in $°C$, $TC1$ is the linear temperature coefficient and $TC2$ is the quadratic temperature coefficient. The equation (1) will fit a quadratic curve through three points in a temperature graph by solving three equations with three arguments.

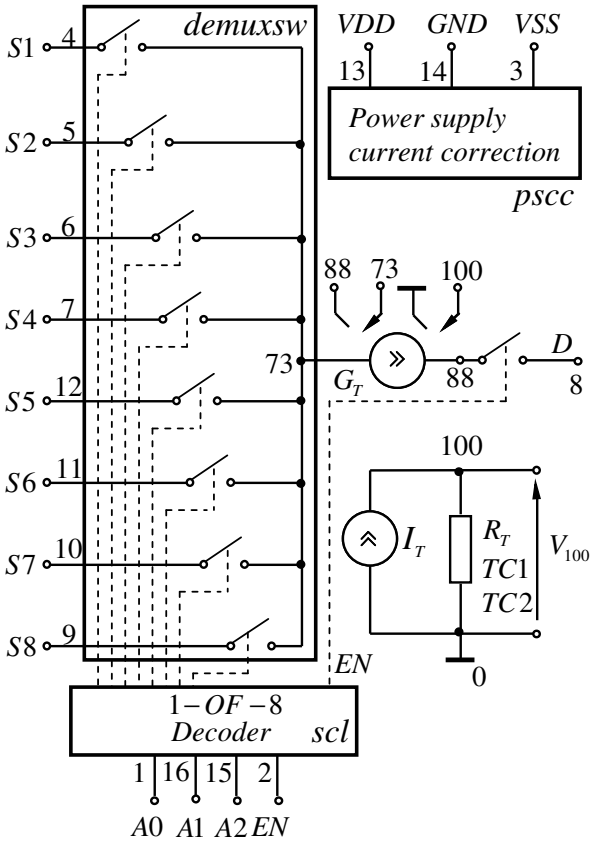

Fig. 2. Conceptual schematic of the proposed analogue multiplexer macromodel improved with temperature

The current I_T will flow through the resistor R_T, towards the internal ground. In such a way the voltage $V_{100,0}$ will depend upon the temperature.

$$V_{100,0} = I_T R_T(T_0)\left[1 + TC1(T - T_0) + TC2(T - T_0)^2\right] \qquad (2)$$

The current source I_T is fixed at $1A$ such that to simplify the calculations for the other components in the macromodel.

The controlling voltage $V_{100,0}$ is a quadratic temperature-dependent input value for the VCCS G_T in the model. The current generated by the G_T will have the following form:

$$I(G_T) = k_{G_T} V_{73,88} V_{100,0} = k_{G_T} V_{73,88} I_T R_T(T) \qquad (3)$$

where $k_{G_T}\ [S/V]$ is a linear coefficient. For convenience, it is chosen to be equal to one.

Since the current source G_T is controlled by two voltages $V_{73,88}$ and $V_{100,0}$, the relation between the on-resistance value at a certain temperature $R_{ON}(T)$ and the value at nominal temperature $R_T(T_0)$ is

$$R_{ON}(T) = R_{ON}(T_0) + \frac{V_{73,88}}{I(G_T)} = R_{ON}(T_0) + \frac{1}{k_{G_T} I_T R_T(T)} \qquad (4)$$

where $R_{ON}(T_0)$ is the switch on-resistance at a temperature $T_0 = 27°C$.

The temperature coefficients $TC1$ and $TC2$, and the resistance $R_T(T_0)$ from Eq. (2) are calculated by employing the least squares sense technique.

The main advantage of this approach is that parameter extraction can be performed only from manufacturer's data, even for integrated circuits whose internal structure is unknown.

Another temperature stage with an exponential behaviour is shown in Fig. 3. Its consists of the voltage source V_{TE}, the diode D_{TE} and the correction current source I_{TE}. The exponential temperature dependence of saturation current $I_S(T)$ in the SPICE diode model [13] is determined by

$$I_S(T) = I_{So} e^{(T/T_0 - 1)E_G/(NV_T)} (T/T_0)^{XTI/N} \quad (5)$$

where I_{So} is the saturation current at T_o, T is the temperature in K (Kelvin), XTI is the saturation current temperature exponent, N is the emission coefficient, V_T is the thermal voltage, and E_G is the energy gap. The parameter extraction can be done for the desired temperature behaviour. The voltage source V_{TE} is fixed at -10V to provide a reverse voltage drop across D_{TE}. The resistor R_{TE} is set to 1Ω in order to minimize the generated thermal noise and to simplify the calculations for the other components in the stage.

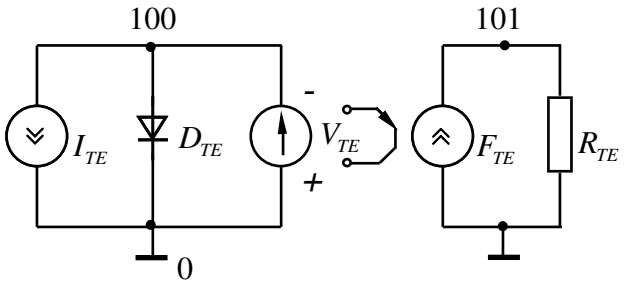

Fig. 3. Stage for generating exponential temperature dependence of the R_{ON}.

The current $I_S(T)$, generated from D_{TE}, will flow through the voltage source V_{TE} towards the ground. The current $I_S(T)$ is an exponential temperature-controlled input value for current-controlled current source (CCCS) F_{TE}, defined in the macromodel. The current generated by the F_{TE} will have the following form:

$$I(F_{TE}) = k_{1,TE} I_{VTE}(T) \quad (6)$$

The leakage current thus generated, $I(F_{TE})$ is routed through the resistor R_{TE}. The linear coefficient $k_{1,TE}$ of the CCCS is selected to be equal to one. The voltage V_{101} works as a linear temperature-controlled input value for VCCS G_T in the model.

III. MACROMODEL PERFORMANCE

The performance of the macromodel has been compared with data sheet parameters of the integrated analogue multiplexer ADG408 [14]. The existing macromodel for the ADG408 was used, with additional elements modelling a quadratic temperature function of the switch on-resistance (Fig. 2), inserted between the node 73 and the output terminal.

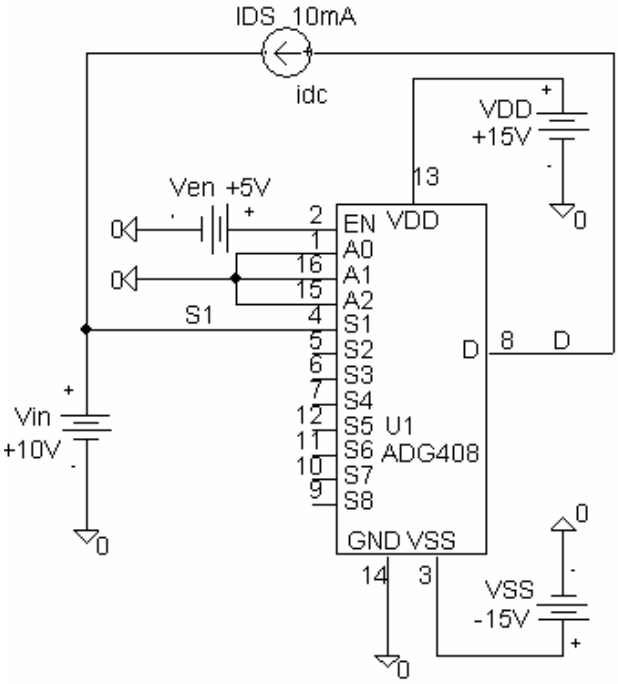

Fig. 4. Test circuit for simulation.

The test circuit for simulation shown in Fig. 4 is created following the test conditions, given in the semiconductor data book of the corresponding IC. The power supply voltages of the circuit are chosen ±15V and logic supply voltage is set to +5V. The DC input signal level V_{in}, applied to node S1 (pin 4), is set to +10V. The ideal current sources $I_{DS} = 10mA$ is connected between nodes S1 and D. For the simulation testing a parametric DC analysis is performed with the sweep parameters within the range from V_{in}=-15V to V_{in}=+15V. The enabling input voltage source $V_{EN} = +5V$ is applied to node EN (pin 2). The computer simulations are implemented for three values of the temperature, namely $25°C$, $85°C$ and $125°C$. Figure 5 and 6 shows the on-resistance versus input voltage for different temperature of the real device ADG408 and the simulation output, using the values in the netlist of Table 1. In Table 1 only additional elements to the existing model [4] are represented. Notice that the simulated response compares quite closely with the actual response. The maximum error between simulation results and manufacturer's data are not higher than 10%, which guarantees the sufficient degree of accuracy.

Table 1. SPICE netlist of the output section for ADG408 model.

```
.SUBCKT ADG408/AD-X 4 5 6 7 12 11 10 9 15 16 1 2 8 13 14 3
*  Section for control line A0, A1 and A2
*  Main Series Switch combination
*  Output and enable switch section *** see Reference [4] ***
GT 73  88 POLY(2) (73 88) (100 0) 0 0 0 0 1
S_EN_1    88  8  2  14    Sdemux
C_EN_1     2  8          4.2E-12 ; SETS CHARGE INJECTION
.MODEL  Sdemux  VSWITCH  (RON=1  ROFF=1E12  VON=2.0
VOFF=1.4)
* Temperature stage
IT 0 100 1
RT 0 100 0.95692800467
+ TC -0.02224408931100 1.306292978368239e-004
.ENDS
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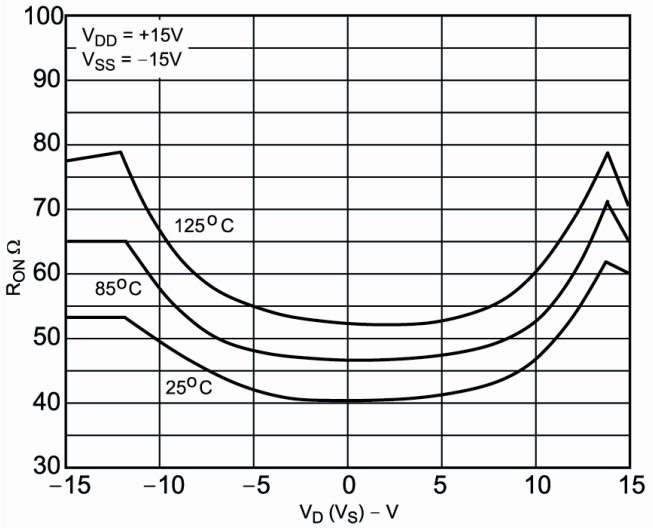

Fig. 5. ADG408 temperature effects.

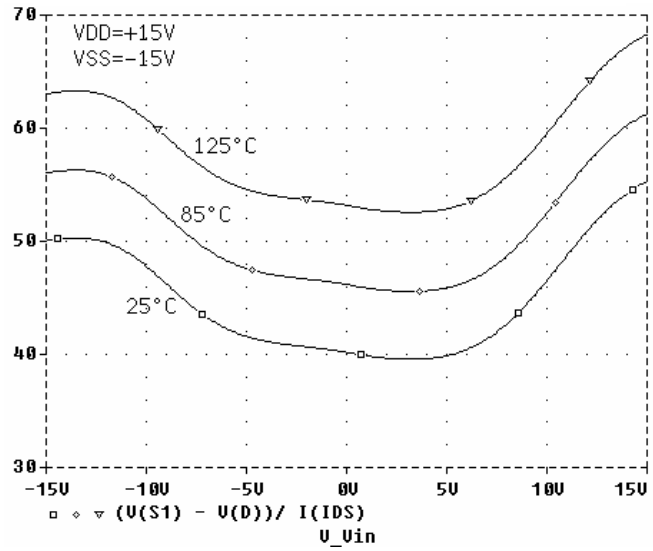

Fig. 6. ADG408 simulated temperature effects.

IV. CONCLUSIONS

This paper presents the development of the analogue multiplexer SPICE macromodel, aimed at improving the modelling of switch on-resistance as a function of temperature. Modelling of the temperature effects of the circuit is independent from the actual technical realizations and the model parameters and can only be obtained from manufacturer's data of the real IC. The macromodel can be used to simulate different kinds of analogue circuits in respect to temperature variations. The detailed comparison with semiconductor data book demonstrates a good correspondence with selected diagrams of the analogue multiplexer ADG408 from Analog Devices. The maximum error between simulation results and manufacturer's data is not higher than 10%. However, other analogue multiplexers, especially those using different topologies or technologies, may well exhibit different functions of the on-resistance R_{ON} versus temperature. These matters are the subjects of further research.

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