

Generating of Basic Wave Digital Elements for Modeling of Two-dimensional Planar Structures

Biljana P. Stošić and Miodrag V. Gmitrović

Abstract - In this paper, the main attention is focus on generating basic two-dimensional (2D) wave digital elements (WDE) and their use for modeling of 2D microwave structures. A reference 2D analog structure is separated into segments. One segment containing four inductors and one capacitor is modeled by frequency-dependent WDE. This four-port WDE is used as base for generating three-port and two-port WDE. Wave digital structure equivalent to the analog structure represents cascade connection of basic WDE and two-port adaptors used for impedance matching. Obtained digital structure is solved in the time domain. The suggested procedure with use of basic 2D WDE is implemented in MATLAB environment. An application example, proving the response accuracy of the new technique, is given.

Keywords – wave digital elements, wave digital structure, microwave circuits, microstrip circuits

I. INTRODUCTION

Microwave planar structures have many applications in practice. Because of this, a great attention is given to their analysis. They are two-dimensional (2D) structures and can be modeled by 2D LC circuits [1-4]. A computer program FAMIL (Frequency Analysis of Microwave Lines) [4] or more known programs GENESYS (RF and Microwave Design Software) and ADS (Advanced Design Software), can be used for analyzing these circuits in the frequency domain.

Standard wave digital elements (WDE), such as delay, adder, multiplier and adaptor, are used in design of wave digital filters [5-8]. A wave digital filter can be designed by direct translation of reference analog filter when WDE are used. In paper [9], a procedure for transmission line modeling using WDE is presented. LC transmission line, observed as one-dimensional (1D) structure, is modeled in two ways: by using unit wave digital element and by cascade connection of T-wave digital elements. In paper [10], a microwave planar lowpass structure is modeled by 1D WDE. Transmission lines are modeled by unit WDE. A basic idea for modeling of a single microwave line by using 2D WDE is presented in paper [11].

In this paper, the main attention is focus on generating what would now be called *basic 2D wave digital elements*. When compared with a 1D wave digital realization, a general 2D wave digital realization approach results in a higher implementation effort. A complex planar structure is to be separated into structure segments first. Then, each structure

segment is divided into multiport segments. Three types of multiport segments occur in the structure: four-port, three-port and two-port segments. A single four-port segment of analog 2D circuit is modeled by four-port network containing inductors in series branches and a capacitor in parallel branch. A bilinear frequency transformation is used for modeling of an analog segment by equivalent symmetrical four-port WDE. This four-port symmetrical WDE represents start element used for obtaining all basic 2D WDE needed for modeling of a complex planar structure. Basic WDE and two-port adaptors for impedances matching are used for obtaining wave digital structure that is equivalent to the reference 2D analog structure. Obtained digital structure is solved in the time domain.

The suggested procedure is built-in in MATLAB environment. The frequency response is found by use of standard MATLAB programs such as `dlinmod.m`, `dimpulse.m` and `fft.m`. An application example, proving the response accuracy of the suggested procedure by use of basic WDE, is given. The analysis results are then compared with the analysis results of equivalent analog circuit obtained by computer program FAMIL.

II. BASIC 2D WAVE DIGITAL ELEMENTS

A planar microwave structure divided into segments is depicted in Figure 1. Three types of multiport segments occur in any complex 2D structure: four-port central (Central – Cen), three-port edge (LeftEdge – LE, RightEdge – RE, UpEdge – UE and DownEdge – DE) and two-port corner (DownLeftCorner – DLC, DownRightCorner – DRC, UpLeftCorner – ULC and UpRightCorner – URC). In order to generating basic 2D wave digital networks corresponding to the multiport segments, a four-port segment is analyzed first. An analog structure of the four-port segment is shown in Figure 2a. Each segment is modeled by inductors in the series branches and capacitor in the parallel branch.

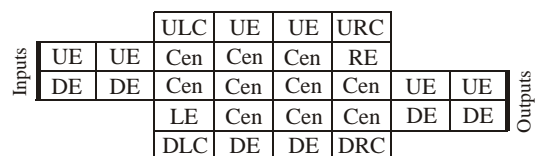


Fig.1. Segmented 2D structure.

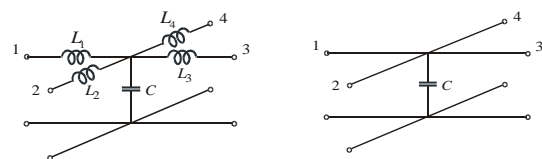


Fig.2. (a) An equivalent LC analog network of four-port segment, and (b) a four-port C analog network.

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The inductances and capacitance can be obtained by expressions given in [3-4]. Wave digital network of the analog LC network shown in Figure 2a, is obtained starting from the four-port network containing capacitor in parallel branch, Figure 2b.

The five-port parallel adaptor with dependent port five is used for modeling capacitor in parallel branch. In this way the four-port wave digital network of the capacitor in parallel branch (WC_Cen), shown in Figure 3, is obtained [1-3]. The WC_Cen is symmetrical because of $L_1 = L_3$ and $L_2 = L_4$ for homogenous structures. This network corresponds to centrally placed segments. For this wave digital network, the equations for wave variables are

$$A_5 = z^{-1}B_5, \quad (1)$$

$$A_S = \alpha_1(2A_5 - A_1 - A_3) + \alpha_2(2A_5 - A_2 - A_4), \quad (2)$$

$$B_5 = A_5 - A_S, \quad (3)$$

$$B_k = B_5 + A_5 - A_k, \quad k = 1, 2, \dots, 4, \quad (4)$$

where A_k and B_k are incident and reflected wave variables. The multiplier coefficients are calculated by expressions

$$\alpha_1 = \frac{2GL}{2GL + 2GLt + GC} \quad (5)$$

and

$$\alpha_2 = \frac{2GLt}{2GL + 2GLt + GC}, \quad (6)$$

where GL and GLt are port conductances.

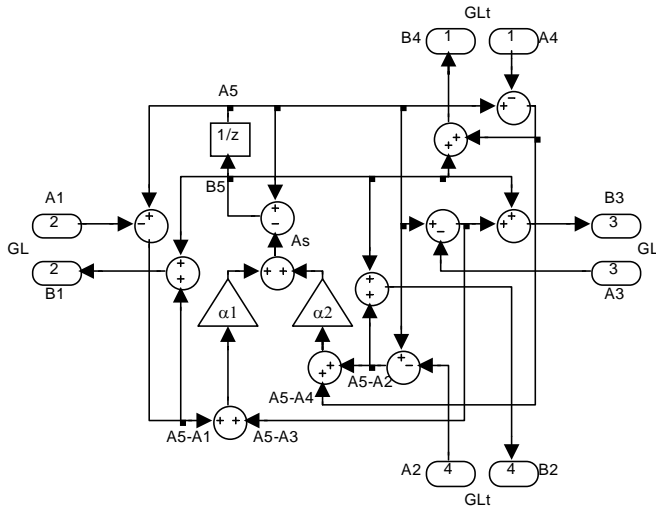


Fig.3. Symmetrical four-port wave digital network of capacitor for centrally placed segments (WC_Cen).

TABLE I

PORT SIGNAL ORDERING FOR WAVE DIGITAL EDGE ELEMENTS AND MULTIPLIER COEFFICIENTS

1) Left	2) Right	3) Up	4) Down
B4 A4 GLt	B4 A4 GLt	B1 A1 GL	B1 A1 GL
B3 A3 GL	B1 A1 GL	B2 A2 GLt	B4 A4 GLt
B2 A2 GLt	B2 A2 GLt	B3 A3 GL	B3 A3 GL
$\alpha_1 = 2GL / SG$ $\alpha_2 = 2GLt / SG$ $SG = GL + 2GLt + GC$		$\alpha_1 = 2GLt / SG$ $\alpha_2 = 2GL / SG$ $SG = 2GL + GLt + GC$	

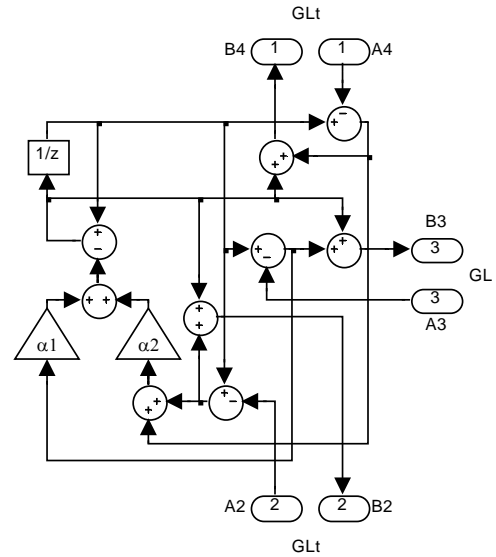


Fig.4. Three-port wave digital network of capacitor for segments edging structure at the left side (WC_LE).

The four-port wave digital network of WC_Cen segment is start point for obtaining wave digital networks of all other segments (three-port and two-port segments).

There are four different segments edging the structure: LE, RE, UE and DE. Ordering of port signals for edge WDE and relations for multiplier coefficients are given in Table I. Three-port wave digital network of capacitor for segment edging structure at the left side (WC_LE) is shown in Figure 4.

Also, there are four different two-port segments placed at the structure corners: DLC, DRC, ULC and URC. Ordering of port signals for corner WDE and relations for multiplier coefficients are given in Table II. Two-port wave digital network of capacitor for segment placed at the structure down left corner (WC_DLC) is shown in Figure 5.

TABLE II

PORT SIGNAL ORDERING FOR WAVE DIGITAL CORNER ELEMENTS AND MULTIPLIER COEFFICIENTS

1) Down Left	2) Down Right	3) Up Left	4) Up Right
B4 A4 GLt	B4 A4 GLt	B2 A2 GLt	B2 A2 GLt
B3 A3 GL	B1 A1 GL	B3 A3 GL	B1 A1 GL
$\alpha_1 = 2GL / SG$ $\alpha_2 = 2GLt / SG$ $SG = GLt + GL + GC$			

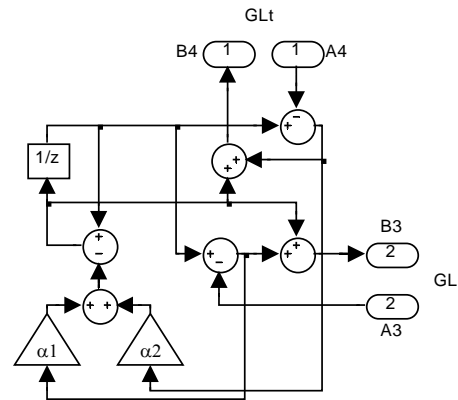


Fig.5. Two-port wave digital network of capacitor for segment placed at the structure down left corner (WC_DLC).

The inductors in the series branches are modeled by unit wave digital elements (UE) [6]. For symmetrical networks, the port resistances of UE corresponding to the inductors L_1 and L_3 are $R_1 = L_1$, and the port resistances of UE corresponding to the inductors L_2 and L_4 are $R_2 = L_2$. Each inductor is represented by a delay element. In this paper, one delay is placed at input port (A1) and the three other delays at output ports (B2, B3, B4), Figure 6a. Some of the wave digital elements corresponding to the analog LC networks for different types of segments such as central (WLC_Cen), edge (WLC_LE) and corner (WLC_DLC), are shown in Figure 6.

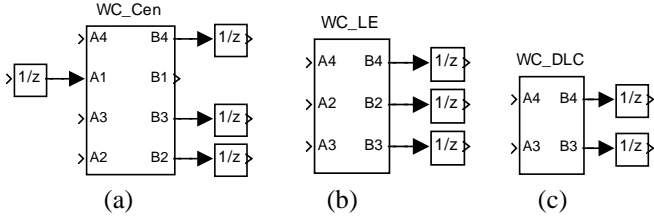


Fig.6. Wave digital elements of LC analog network for:
(a) central segments (WLC_Cen),
(b) edge segments (WLC_LE) and
(c) corner segments (WLC_DLC).

III. MICROWAVE T-JUNCTION AND ITS MODELING BY 2D WDE

A microstrip T-junction is shown in Figure 7. This homogenous planar structure is separated into three structure segments first. Structure segments, Line1 and Line 3, are divided into 3x5 segments, and Line2 into 22x10 segments. Structure lines are then modeled by cascade connection of corresponding WDE. Wave digital structure (WDS) obtained by modeling analog structure with WDE is depicted in Figure 8. Line1 is cascade connection of five SubNetwork3 shown in Figure 9. Adaptors (ADP-In, ADP-L12, ADP-L23 and ADP-Out) are used for port resistance matching. The coefficients of two-port frequency-independent adaptors, α_S and α_L , are given in [6].

In practice, a great number of WDE can be used and complex network obtained. A complex WDS can be formed by multiplication of basic 2D WDE. The WDE are formed in Simulink toolbox of MATLAB environment.

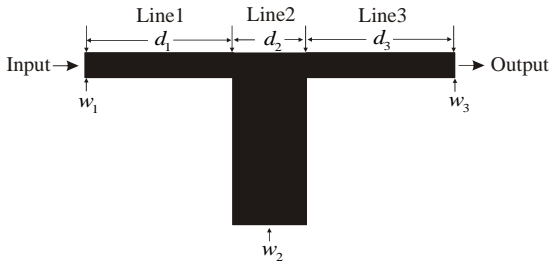


Fig.7. Microstrip T-junction

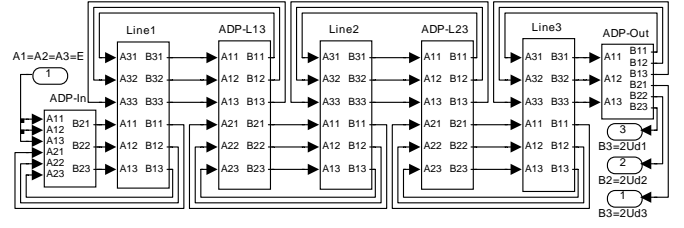


Fig.8. Wave Digital Structure (WDS).

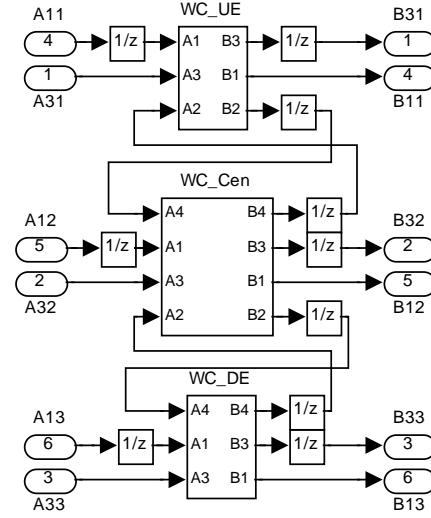


Fig.9. SubNetwork3 in Line1.

IV. APPLICATION EXAMPLE RESULTS

For observed T-junction, substrate material is Polyguide of relative dielectric constant $\epsilon_r = 2.32$ and high $h = 1.58 \text{ mm}$.

The widths of the cascade-connected lines are: $w_1 = w_3 = 4.71 \text{ mm}$ and $w_2 = 34.71 \text{ mm}$. Their lengths are: $d_1 = d_3 = 30 \text{ mm}$ and $d_2 = 15.76 \text{ mm}$. The resistances of 50Ω are connected to the input and output ports.

Formed WDS, verifying the suggested procedure and proposed basic WDE, is depicted in Figure 8. Comparison of WDS 2D simulation results for three sampling frequency values is depicted in Figure 10. It can be concluded that WDS 2D response accuracy is better for higher values of sampling frequency. For this T-junction, increasing of sampling frequency above 750 GHz , influences simulation results a very little. Because of this, Figure 11 shows the comparison of $|S_{21}|$ simulation results of WDS 2D procedure for $F_{oj} = 750 \text{ GHz}$ and program FAMIL.

The multiplier coefficients of the two-port adaptors at the source side (ADP-In) are $\alpha_S = -0.9094$, and at the load side are $\alpha_L = 0.9094$. For block ADP-L12, the coefficients are $\alpha_A(1) = 0.4226$, and for block ADP-L23 $\alpha_A(2) = -0.4226$. Each WDE has two multipliers and their coefficients are given in Table III.

TABLE III

MULTIPLIER COEFFICIENTS OF THE CENTRAL AND CORNER WDE

	WC_Cen		WC_C	
	α_1	α_2	α_1	α_2
Line1 & Line3	0.0022	0.0321	0.0022	0.0326
Line2	0.0278	0.0277	0.0286	0.0285

MULTIPLIER COEFFICIENTS OF THE EDGE WDE

	WC_E			
	WC_LE & WC_RE		WC_UE & WC_DE	
	α_1	α_2	α_1	α_2
Line1 & Line3	0.0022	0.0321	0.0022	0.0326
Line2	0.0282	0.0281	0.0282	0.0281

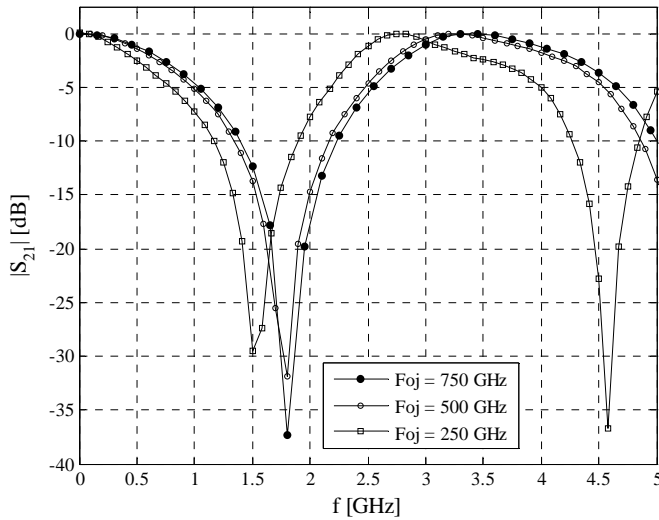
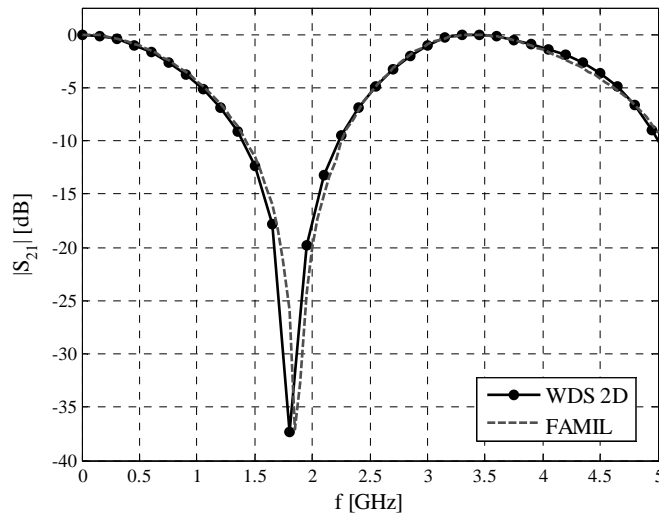


Fig.10. Comparison of WDS 2D simulation results for different sampling frequency values.


 Fig.11. Comparison of $|S_{21}|$ [dB] simulation results for $F_{oj} = 750$ GHz.

V. CONCLUSION

The procedure for modeling of 2D microwave structures by WDE is described. The attention is given to generating the basic 2D WDE. A general four-port analog 2D segment is

modeled by symmetrical four-port digital network. In this paper, basic WDE corresponding to segments placed at different position in the structure, are given. According to the segment positions, there are three types of WDE: WDE for centrally placed segments (WLC_Cen), WDE for segments edging structure (WLC_E) and WDE for segments at the structure corners (WLC_C). Also, a procedure for forming complex WDS equivalent to the reference analog structure is described shortly. In WDS, two-port adaptors are used for port resistance matching. Obtained WDS is analyzed in time domain, and its frequency response is obtained by use of fast Fourier transformation. In order to solve the problem, a program for MATLAB environment is written. The MATLAB standard programs from Simulink toolbox are used. WDS, all basic WDE, and two-port adaptors are drawing directly in Simulink toolbox and save as 'model_name'.mdl files.

An application example, proving the modeling of microwave structure by 2D WDE, is given. The correct choice of the sampling frequency leads to good agreement of the WDS 2D simulation results and analog circuit solution.

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