Design and Implementation of First Order Sigma-Delta Modulator

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***Abstract* – The sigma-delta ADC offers several advantages over the other architectures, especially for high resolution, low frequency applications. First and foremost, the single bit sigma-delta ADC is inherently monotonic and requires no laser trimming. The sigma-delta ADC also lends itself to low cost foundry CMOS processes because of the digitally intensive nature of the architecture. As a result of this, they are widely used in different applications. In this paper an experimental electronic realisation of a first order sigma-delta modulator is presented. The implementation of 1-bit DAC circuit is proposed.**

***Keywords* – A-D and D-A converters, sigma-delta modulator, circuit design, circuit analysis.**

I. INTRODUCTION

Sigma-Delta Analog-Digital Converters (Σ-Δ ADCs) have been known for over thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required. The name, sigma-delta, is a consequence of the integral, or summation over time (Σ), applied to the difference (Δ). Because sigma-delta converters latch on a high speed clock pulse, they do not require sample-hold circuits. Since the bit stream is a train of "ones" and "zeroes", there are no missing codes. This type ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. The high proportion of digital circuitry makes the Σ-Δ ADCs excellent candidates for high yield manufacture in IC form. This circuitry acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a Σ-Δ ADC works, familiarity with the concepts of *over-sampling, quantization noise shaping, digital filtering,* and *decimation* is required. The technique of over-sampling is explained with an analysis in the frequency domain. Where a *dc* conversion has a *quantization error* of up to ½ LSB, a sampled data system has *quantization noise*.

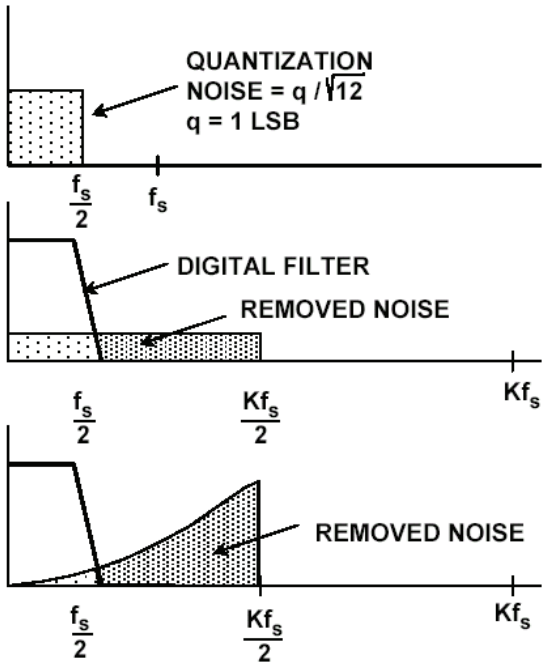

Fig. 1. Noise shaping

A perfect classical n-bit sampling ADC has a *rms* quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of *dc* to $f_s/2$ (where q is the value of an LSB and f_s is the sampling rate) as shown in Fig.1a. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution (often known as its Effective Number of Bits or ENOB) will be less than n-bits. When a much higher sampling rate has been chosen, Kf_s (see Fig.1b), the *rms* quantization noise remains $q/\sqrt{12}$, but the noise is now distributed over a wider bandwidth dc to $Kf_s/2$. If then a digital low pass filter (LPF) is applied to the output, much of the quantization noise will be removed, but without affecting the wanted signal—so the ENOB is improved. Thus a high resolution A/D conversion has been accomplished with a low resolution ADC. The factor K is generally referred to as the *oversampling ratio*. It should be noted at this point that oversampling has an added benefit in that it relaxes the requirements on the analog antialiasing

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filter. The Σ-Δ converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Fig.1c.

II. Basics of Sigma-Delta A/D Converters

The first-order Σ-Δ modulator as shown in Fig.2 is 1-bit ADC (generally known as a latched comparator), driven with the output of an integrator which is fed with an input signal summed with the output of a 1-bit DAC (two-level switched reference) controlled by the ADC output. To complete the ADC a digital low pass filter (LPF) and decimator at the digital output must be added. Σ-Δ modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

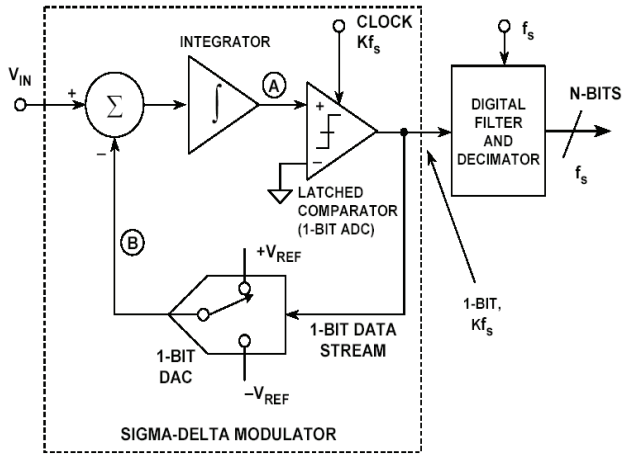

Fig. 2. Basic circuit of Σ-Δ modulator

Intuitively, a Σ-Δ ADC operates as follows. Assume a dc input at V_{IN}. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average dc voltage at node B to be equal to V_{IN}. This implies that the average DAC output voltage must equal the input voltage V_{IN}. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged, the result will be with a meaningful value.

The sigma-delta ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter (Fig. 3). If the number of "ones" in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. Obviously, this method of averaging will only work for dc or very slowly changing input signals. In addition, 2^n clock cycles must be counted in order to achieve n-bit effective resolution, thereby severely limiting the effective sampling rate.

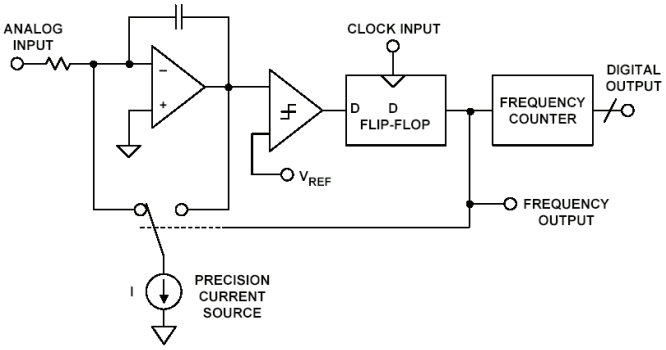

Fig. 3. Basic circuit of synchronous voltage-to-frequency converter

III. Sigma-Delta Modulator Design

The Σ-Δ modulator is the basis of the contemporary oversampling analog-to-digital and digital-to-analog converters. This type of the circuit is very appropriate for high-resolution medium-to-low speed applications such as high quality digital audio, high-precision measurement devices, communication systems, etc. These devices utilize the only low cost conversion method, which provides both high dynamic range and flexibility in converting low-bandwidth input signal. This fact is the reason for the big interest among the microelectronic circuit designers in the operation and practical implementation of the sigma-delta modulators.

In this paper a proposal for sigma-delta modulator design is given on Fig. 4.

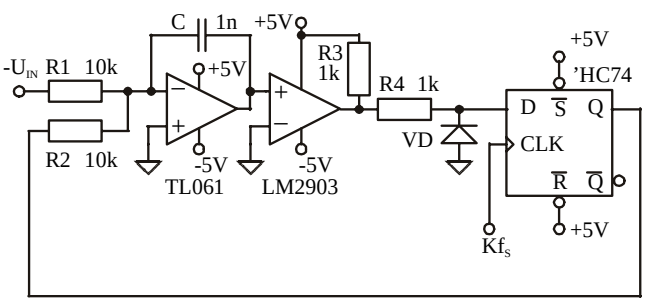

Fig. 4. Σ-Δ modulator design proposal

The circuit comprises of summing integrator, comparator and a D-type flip-flop. The j-FET low power operational amplifier TL061 is connected as a summing integrator, which integrates the difference between the input voltage U_{IN} and the

output product of the 1-bit DAC. The low power low offset voltage comparator with open collector output LM2903 is the next stage of the circuit. In order to be able to perform the wanted operation the D-type positive edge triggered flip-flop must have standard CMOS output (for example 74HC74).

The circuit is similar to the basic circuit of synchronous voltage-to-frequency converter. In contrary to the classical scheme of Σ-Δ modulator, the comparator is not latched. The 1-bit data stream is obtained from the flip-flop output. The statement of the comparator is latched in the Q output after the positive edge of the clock signal Kf_S.

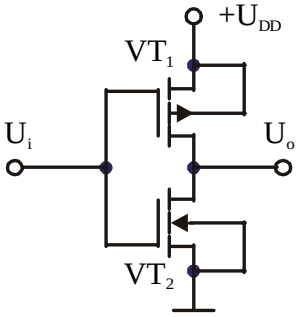

Fig. 5. CMOS output stage

The D-type flip-flop performs the function of the 1-bit DAC. Therefore its output stage must be standard CMOS inverter (Fig. 5). It comprises of two complementary MOS-FET transistors (VT_1-P-channel and VT_2-N-channel). Because of their symmetry the logic "1" is equal to the value of U_{DD} and the logic "0" is equal to the ground. This ability of the CMOS output allows the D-type flip-flop 74HC74 to function as a two-level switched reference because it combines the functions of the memory cell and the two-level switch. So, when the statement of the comparator is high, voltage value equal to the 74HC74 supply voltage will be subtracted from the input voltage value. When the comparator statement is low the value of the subtracted voltage will be zero. To ensure a negative feedback the value of the input voltage of the Σ-Δ modulator must vary from ground to the negative supply. The additional components are with standard application. The resistor R_3 sets the voltage level in the open collector output of the comparator. The resistor R_4 and the diode VD prevent the negative voltage from the comparator output to break-down the input of the flip-flop.

IV. Experimental Results

The experiments were carried out by PSpice simulation and laboratory set-up with testing and measurement instruments in order to integrate the processes of design, simulation, testing and measurement. The studying of these processes and their interaction gives the designer very useful information. To verify the design and simulation the measured values have been compared with the results obtained by PSpice simulation.

In the following figures the modulator's behaviour is depicted with probe.

The resulting output of the analog integrator in the PSpice realisation of the designed sigma-delta modulator is plotted in Fig. 6.

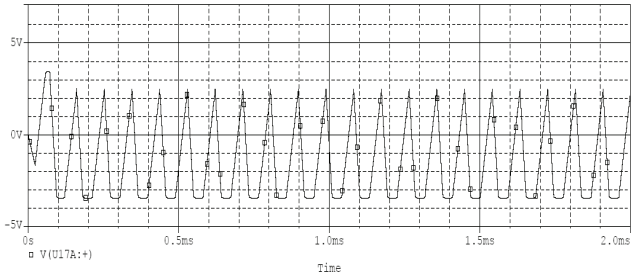

Fig. 6. Summing integrator output voltage

On Fig. 7 the resulting output the Q output of the flip-flop is given.

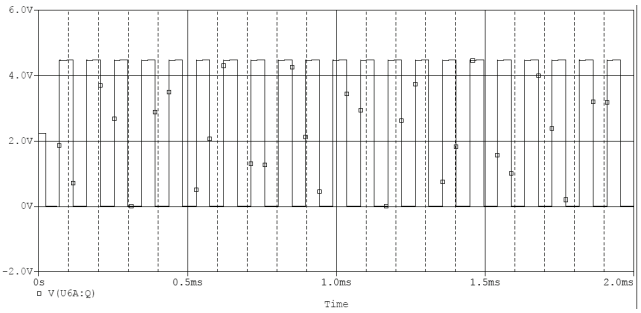

Fig. 7. Q output flip-flop waveforms

The feed from the digital clock impulse generator used for 74HC74 flip-flop is depicted in Fig. 8 while in Fig. 9 the resulting outputs of the 74HC74 (digital presentation of the signal) are shown.

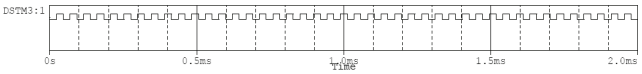

Fig. 8. Digital clock waveforms

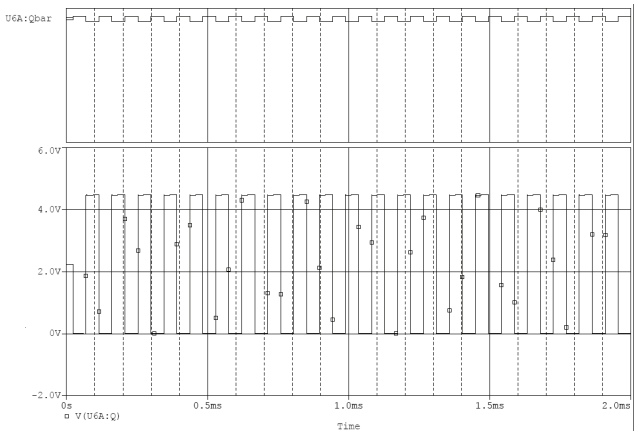

Fig. 9. 74HC74 outputs waveforms

After completing the measurements the obtained results were almost identical with the results obtained from PSpice simulations. The output of the analog integrator viewed on oscilloscope is given in Fig. 10 and the digital output signal observed on oscilloscope can be seen in Fig.11.

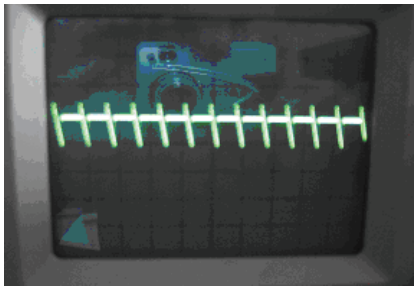

Fig. 10. Real summing integrator output voltage

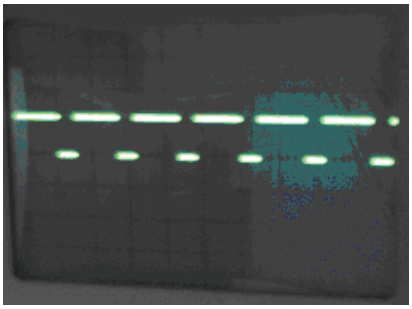

Fig. 11. Real digital output signal

V. CONCLUSION

With the aim of understanding the operation principle, it is especially useful to propose appropriate prototypes of first and higher order sigma-delta modulators. These prototypes should be quickly realisable and should allow easy and simple alteration of the circuit configuration, as well as of the circuit elements' parameters. This would make possible a fast and effective analysis of the designed circuit operation, and a control of the relation between the elements' parameters and the circuit's mode of operation.

The realisation of the designed first order sigma-delta modulator proved the simulation results which approbated it for future incorporation within the laboratory practice of Theoretical Electrical Engineering. Focus for some future experimental work will be the extension of modulator's model to higher order.

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