Simulation Investigation of Frequency Sensitive Digital Phase Detectors

Aleksandar H. Yordanov[1] and Georgy S. Mihov[2]

***Abstract* – In this paper a method for simulation of digital frequency sensitive phase detectors is examined. The main point is to create a simulation method to present phase - voltage response of analyzed schemes by using transient analysis. This can be done by setting to different frequencies to input pulse sequences which creates a linear increase of the phase difference. In that simulation the phase difference is equivalent to time with a predetermined phase step. The step can be changed when a different accuracy is desired and it is depend on input frequencies. In the paper are shown simulations of the most common digital frequency sensitive phase detector and a digital frequency sensitive phase detector working on both fronts of an input signal.**

***Keywords* – Digital phase detector, Simulation of phase - voltage response, ICEST 2007,**

I. Settings for Simulation Analysis of Phase Detectors

The main point of this paper is to crate a method of simulation analysis for digital frequency sensitive phase detectors and mainly their functional dependence. Frequency sensitive phase detectors have certain features which allow conveniently to present phase - voltage response by using transient analysis. This method can be used for analysis of many types of digital phase detectors and further more, it can be used with any kind of simulation programs with transient analysis.

The block diagram for simulation analysis of a phase detector is shown on Fig. 1.

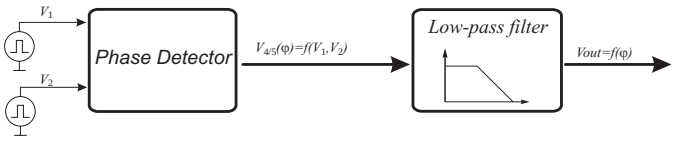

Fig. 1. Block diagram

The method uses two impulse generators with different frequencies.

In this simulation the low-pass filter which is used is active and inverts the input signal. To obtain the phase - voltage response as it expected [1], it is take the leading signal to be v_2. This is equal to take the second output as leading and respectively to invert the output signal, so the output voltage is expected to rise when phase difference is increasing.

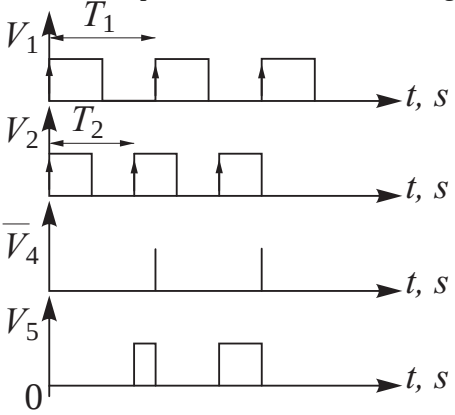

Fig. 2. Input/Output time diagrams

An example of input/output time diagrams is shown on Fig. 2. The signal v_5 is equal to the phase difference between signals v_1 and v_2, respectively frequencies f_1 and f_2.

$$V_1 = v_1(\varphi_1 + kT_1) \tag{1}$$

$$V_2 = v_2(\varphi_2 + kT_2) \tag{2}$$

where k = 0, 1, 2, ….

$$v_1 = \begin{cases} 1, & when\ \ 0 \le t \le \dfrac{T_1}{2} \\ 0, & when\ \ t > \dfrac{T_1}{2} \end{cases} \tag{3}$$

$$v_2 = \begin{cases} 1, & when\ \ 0 \le t \le \dfrac{T_2}{2} \\ 0, & when\ \ t > \dfrac{T_2}{2} \end{cases} \tag{4}$$

φ_1 and φ_2 are starting phases, T_1 and T_2 are periods of both impulse sequences. If it is assumed, that φ_1 and φ_2 are 0 and

$$\Delta t = T_1 - T_2 \tag{5}$$

then

$$V_1 = v_1(kT_2 + k\Delta T_2) \tag{6}$$

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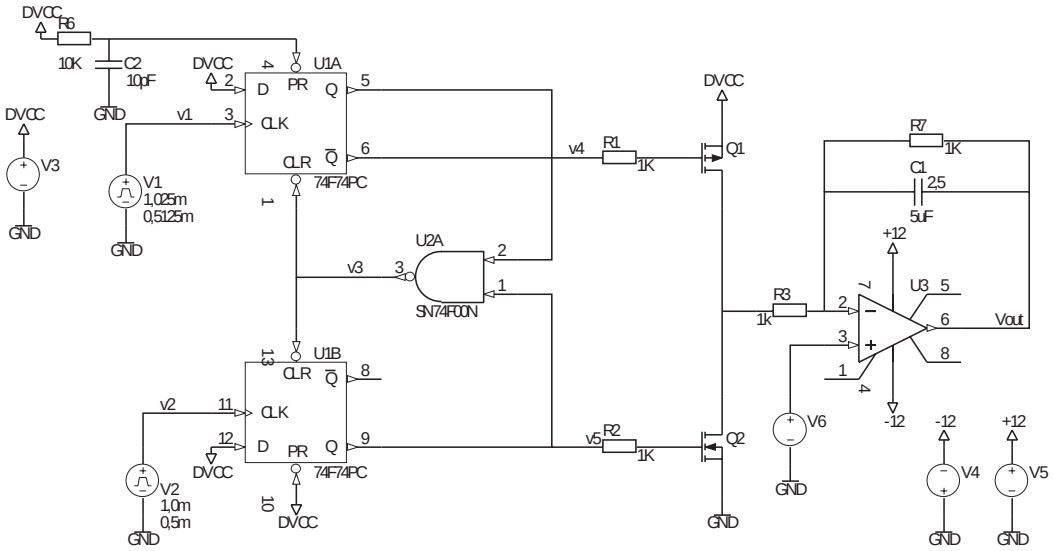

Fig. 3. Scheme of common phase detector

$$V_2 = v_2(kT_2) \tag{7}$$

Delay of signal v_1 towards signal v_2 for one period T_2 is Δt. Time delay Δt can be present as phase delay by using Eq. 5 and 6. To get the phase it is replaced

$$\varphi = q.\Delta t \tag{8}$$

where q is coefficient with a dimension $\left[\frac{rad}{s}\right]$. If delay is equal to the repeating period T_2 then $2\pi = q.T_2$ and

$$q = \frac{2\pi}{T_2} \tag{9}$$

It is replaced Eq. 9 in Eq. 8 and 6 and gets:

$$\Delta t = \frac{\varphi}{q} = \frac{\varphi.T_2}{2\pi} \tag{10}$$

$$V_1 = v_1\left(kT_2 + \frac{k.\varphi.T_2}{2\pi}\right) \tag{11}$$

The expression $\frac{k.\varphi.T_2}{2\pi}$ represents the phase difference between signals v_1 and v_2, which is produced in output of the digital frequency sensitive phase detector. It is clear from Eq. 11, that the phase difference is proportional of period T_2 and the counts of periods k, which is passed. If

$$\frac{2\pi}{\varphi} = n \tag{12}$$

where n is integer, then when k is equal to n, the phase difference between two signals will be 0 or -2π, or +2π. The coefficient n represent the number of points, which describe phase - voltage response.

Example: If $\varphi = \frac{\pi}{4}$ then n=8, i.e. after 8 impulses the phase difference between v_1 and v_2 will be 2π.

Very important result for simulation is that the phase difference φ is linearly proportional of the time. This gives opportunity to change the time line of transient analysis with a phase line, i.e. x-axes is phase. The alteration step of this phase is different from the time step in transient analysis and is equal to coefficient n.

On Fig. 3 it is shown a scheme of a common digital frequency sensitive phase detector. This scheme is well known and studied and its phase - voltage response is varied from -2π to +2π. If two impulse generators are used with different frequencies this alteration will be only from 0 to +2π or from 0 to -2π. This comes from the rotation direction of the phase which can be positive or negative. The full scale phase - voltage response can be produced if one of D-flip-flop is set to start from 1 as initial condition. In the scheme on Fig. 3 this is done by R6 and C2. This circuit hold on the D- flip-flop U1A at a logic level 1 for a time, which is much less then one period of the input signal v_1 but much more then the time of rising front. The initial condition sets an initial phase difference equal to -2π.

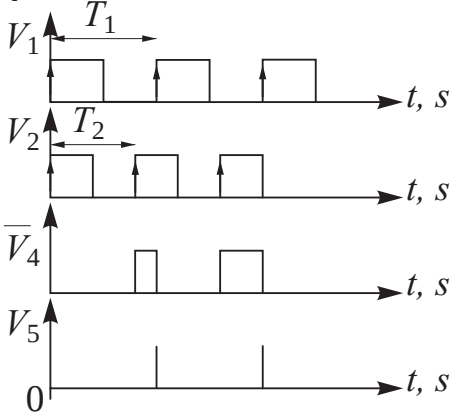

Fig. 4. Input/Output time diagrams, when scheme is set to start whit phase difference φ = - 2π rad

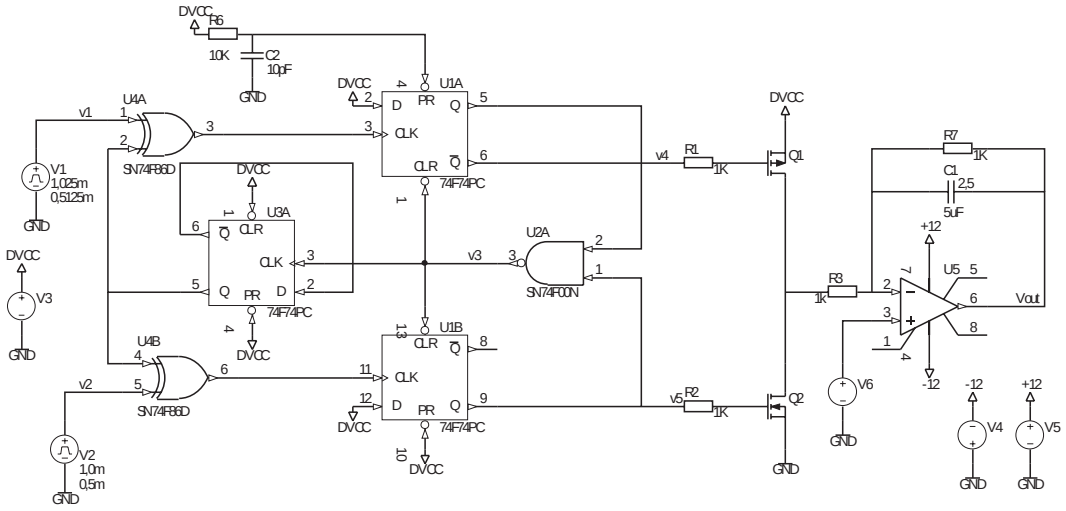

Fig. 6. Scheme of phase detector using both fronts of compared signals

Simulation parameters are:

- The time period of v_2 is 1 ms and the time of impulse is 0,5 ms (it is shown on Fig.3 near by the generator V2). This define a frequency of 1 kHz and a duty cycle of 50%
- The number of points of phase - voltage response in interval -2π to 0 is 40, i.e. n=40.
- From Eq. 12 and 11 for signal v_1 is calculated period 1,025 ms and the time of impulses is 0,5125 ms (it is shown on Fig.3 near the generator V1). This define frequency of 0,9756 kHz and a duty cycle of 50%.
- It is set as an initial condition on capacitor C1 voltage of 2,5 V. This is done because when the phase difference is equal to 0 (i.e. φ=0 rad), than the output voltage is ½ of the whole voltage range (the power supply is 5 V). To skip the setting time of circuit it is recommended to set in simulation 2,5 V on capacitor C1.
- 2,5 voltage is set to not-inverting input of an operational amplifier by a generator V6.
- In transient analysis the time step is set at 10 μs, the start time of the analysis is 0 s and the end time of the analysis is 80 ms.

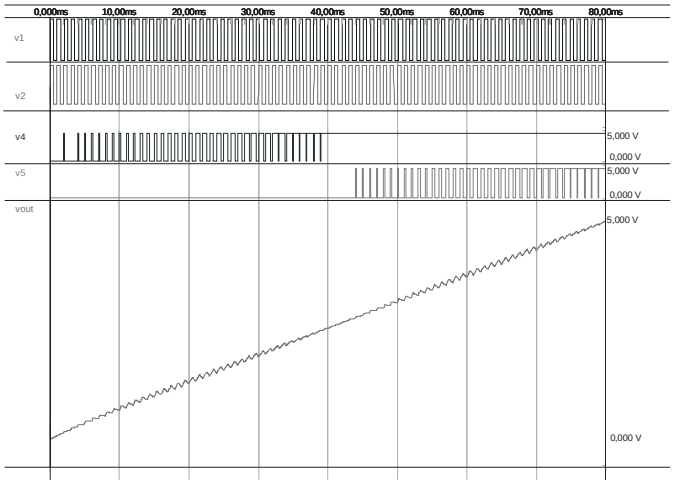

Fig. 5. Transient analysis of common phase detector

Fig. 5 shows a simulation transient analysis of the circuit from Fig. 3. Signals in points v_4 and v_5 give a phase difference between input impulses, which are changed from -2π to +2π. Output signal Vout is proportional of the phase difference which is changed on every period of the input sequence. The diagram of Fig. 5 can be assumed as a phase - voltage response of the scheme of Fig. 3 based on 80 points. It is important to note that this phase - voltage response is not only of the phase detector. It is a phase - voltage response of both the phase detector and the filter used.

II. DIGITAL PHASE DETECTOR USING BOTH FRONTS OF COMPARED SIGNALS

Digital frequency sensitive phase detector using both fronts of compared signals is based on a common scheme and it is shown on Fig. 5. Here input signals v_1 and v_2 are passed on logic elements XOR. These logic gates change working front depending on output signal v_4 and v_5. The scheme of the digital frequency sensitive phase detector using both fronts of compared signals is shown of Fig. 5.

The simulation analysis method is similar to the previous one. Here it should be considered that the scheme works with both fronts of the input signals, i.e. in one period there is two output signals – one for the time of impulse and another one for the time of pause.

$$V_1 = v_1\left(kT_2 + \frac{kT_2}{2\pi}\left(\varphi_{imp} + \varphi_{pause}\right)\right) \tag{13}$$

If the duty cycle is 0,5 then $\varphi_{imp} = \varphi_{pause} = \varphi$ and the Eq. 13 is:

$$V_1 = v_1\left(kT_2 + \frac{k.\varphi.T_2}{\pi}\right) \tag{13a}$$

It is clear that the phase step in this case is twice then the one in previous example and the range is from -π to +π.

The alteration of the front of comparison is done by a control D-triger U3A on the scheme, shown on Fig. 6. When an output impulse is appeared, a control D-triger changes its condition and respectively, changes the working front.

On Fig. 7 is shown the simulation analysis of the scheme on Fig. 6. Input parameters are the same as the those on previous example, but here for one period of input signal there are two output impulses. That is way the number of the phase steps is twice less, i.e. n is twice less (20) and the end time is twice less (40 ms).

Simulation parameters are:

- The time period of v_2 is 1 ms and the time of impulse is 0,5 ms (it is shown on Fig.6 near by the generator V2). This define frequency of 1 kHz and a duty cycle of 50%;
- The number of points of phase - voltage response in interval $-\pi$ to 0 is 20, i.e. n=20.
- From Eq. 13a for signal v_1 is calculated period 1,025 ms and the time of impulses is 0,5125 ms (it is shown on Fig.6 near by the generator V1). This define frequency of 0,9756 kHz and a duty cycle of 50%.

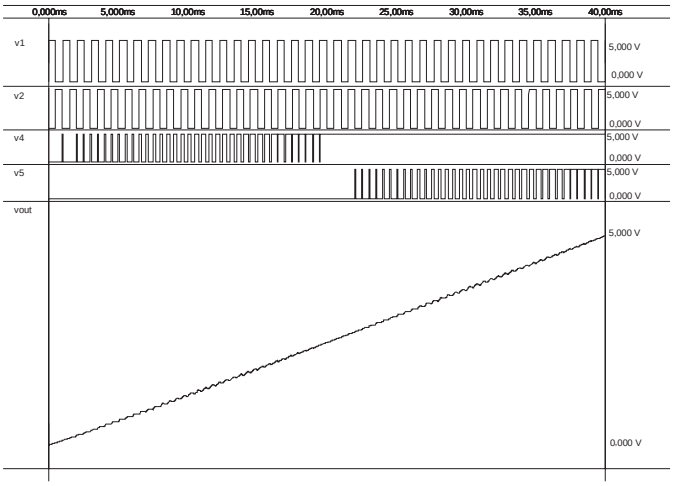

Fig. 7. Transient analysis of phase detector using both fronts of compared signals

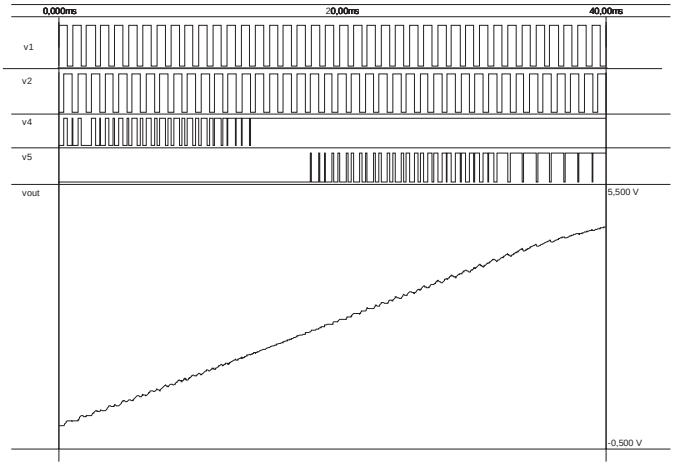

Fig.8. Transient analysis of phase detector using both fronts of compared signals

On Fig. 8 is shown the simulation analysis of the scheme on Fig. 6. Input parameters are the same as the those on previous example except the duty cycle of the both input sequences which, is 60% and the initial phase $\varphi = -0{,}79.\pi$.

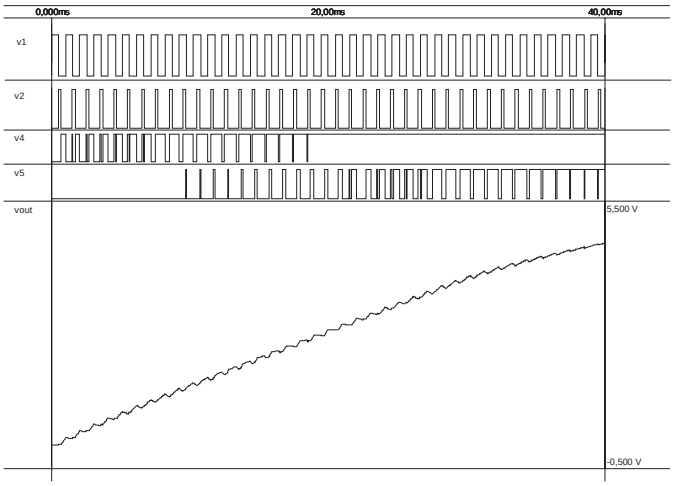

Fig.9. Transient analysis of phase detector using both fronts of compared signals

On Fig. 9 is shown the simulation analysis of the scheme on Fig. 6. Input parameters are the same as the those on previous example except the duty cycle of the input sequences, which is 50% for the signal v_1 and 10% for the signal v_2. The initial phase is $-\pi$.

III. CONCLUSION

In this paper a method for simulation analysis of digital frequency sensitive phase detectors is presented. It is shown a simulation analysis of a common scheme of a digital phase detector and a simulation analysis of a scheme of digital frequency sensitive phase detector using both fronts of compared signals. The simulations of both schemes showed their specific features. The method gives correctly fundamental phase - voltage response of the examine detector and shows the basic features of the scheme.

Most of the common simulators do not give opportunity to set as an input parameter the phase difference between two generators. That is why to examine this kind of schemes is possible only if the phase is exchangeable with another parameter. The most convenient way is to use transient analysis and input generators with two different frequencies. This method gives a phase difference with constant step and linear constant change of input phase.

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