Voltage-Scaling D/A Converters – Analysis and Practical Design Considerations

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***Abstract* – The following article is an attempt to describe the basics of potentiometric D/A converters.**

The analysis of one-stage and two-stage potentiometer-type D/A converters takes into account all the major factors that affect converters' performance. Practical design considerations are also discussed. To support the theoretical analysis, 10- and 12-bit D/A converters were designed and fabricated in 1.0μm and 0.35μm double-poly, double-metal CMOS processes. Experimental results are then analyzed. A good agreement between the theoretical analysis and practical results is observed. The D/A converters under discussion are included in a standard analogue cell library and are used in a successive approximation A/D converter as well.

Keywords – DAC, mixed-signal, CMOS

I. INTRODUCTION

Voltage-scaling (or potentiometer-type) Digital-to-Analog Converters (DACs) use resistors connected in series between the reference voltage V_{REF} and the ground node to selectively obtain voltages between these limits, Fig. 1

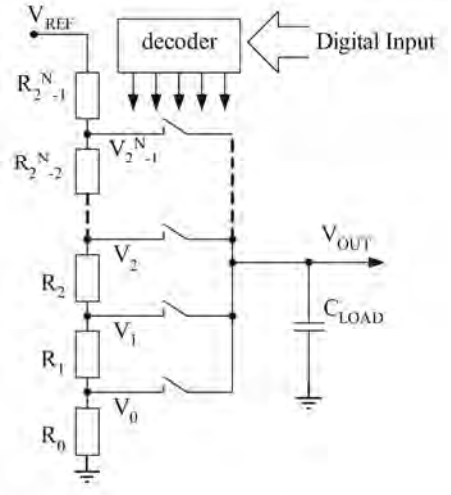

Fig. 1. The principle of operation of potentiometric DACs

With 2^N resistors 2^N reference signals are available and only one of them at a time is passed to the output depending on the digital input. An important advantage of the potentiometer-type DAC is its inherent monotonicity, since the voltage at each tap cannot be lower than the voltage at the tap below it. The voltage-scaling converters are very suitable for current digital CMOS processes as they only need basic devices and have relaxed requirements for device matching.

In high-resolution applications the number of resistors increases exponentially and becomes too large. For example, a 10-bit DAC requires 2^{10}=1024 resistors and 12-bit DAC would have 2^{12}=4096 resistors. Such a big number of resistors occupies too much space; moreover, implementing big arrays of matched devices is difficult and impractical. To reduce the number of resistors required, two-stage structures are used, each of them usually having $2^{N/2}$ resistors, Fig. 2.

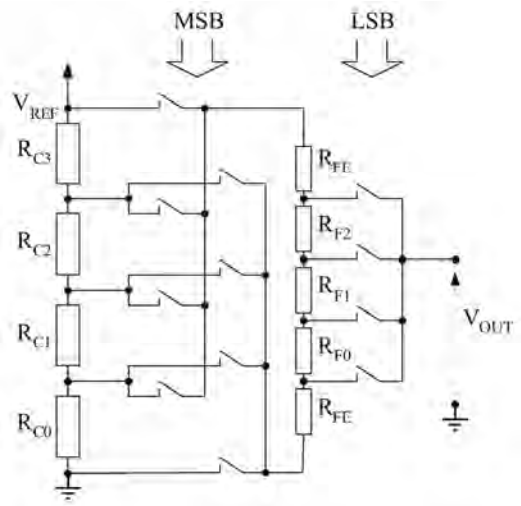

Fig. 2. Two-stage potentiometric DAC

The first stage divides the reference voltage into $2^{N/2}$ equal voltages which are then split into another $2^{N/2}$ levels. Thus the final resolution remains 2^N, since $2^{N/2}$ x $2^{N/2}$ = 2^N. However, the total number of resistors is 2 x $2^{N/2}$ instead of 2^N. For example, a 10-bit two-stage DAC has 64 resistors and a 12-bit DAC has 128 resistors, which is much fewer than the one-stage architecture.

Since single-stage potentiometric DACs can only provide low resolution, the focus in this article is on the two-stage DACs. A good design compromise is to choose the number M of the most significant bits (MSB) that control the coarse divider to equal the number L of the least significant bits (LSB) that control the fine divider. A higher number of MSB would make it difficult to achieve the desired accuracy; fewer MSB would result in more resistors in the fine string and increased output impedance. For that reason and for the sake of simplicity of the equations, the preferred case with

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M=L=N/2 is considered, where N is the total number of bits. Nevertheless, all the expressions are valid if N and N/2 are replaced by the actual numbers M and L.

II. Error sources in the two-stage potentiometric DACs

A. The influence of the fine resistor string on the coarse string

The straightforward approach to make the coarse resistor string independent of the fine string is to use buffer amplifiers between them, Fig. 2. Buffers, however, imply even more difficulties - true rail-to-rail operation is necessary and the offset voltage of the buffers adds to the total error of the converter. So a simplified topology was chosen instead, which does not need buffer amplifiers, providing some basic requirements are met. When the fine string is connected in parallel to any of the resistors in the coarse string, the actual resistance existing between the terminals of that coarse resistor changes:

$$R_C^{ACTUAL} = R_C II\left(\sum R_F\right) = R_C II\left(2^{N/2} R_F\right) \tag{1}$$

Hence the voltage drop across this coarse resistor also changes, the error being expressed as (intermediate steps are omitted for clarity):

$$\begin{aligned}\Delta V &= \left(V_{N+1} - V_N\right)_{ACTUAL} - \left(V_{N+1} - V_N\right)_{IDEAL} \\ &= \frac{V_{REF}}{2^{n/2}}\left(\frac{R_C}{R_C + 2^{n/2} R_F}\right)\end{aligned} \tag{2}$$

Two approaches are possible:

a) keeping the error much smaller than 1 least significant bit (LSB)

b) making the error exactly equal to 1 LSB

The first approach calls for $R_F >> R_C$. This is not difficult to realize, but the resulting output impedance is high. The second approach needs

$$R_F = R_C \times \frac{2^N - 2^{N/2}}{2^N} \approx R_C \tag{3}$$

The fine resistors are smaller (less die area) and the output impedance is lower. However, the resistance of the MOS switches, which is added to the fine resistor string, introduces unacceptable errors. For this reason, the first approach is given preference, provided the load capacitance is low (approximately 1-5 pF)

B. Device mismatch

If $T_{(RI;RII)}$ is the transfer function of a potentiometer,

$$T = V_{REF} \frac{R_I}{R_I + R_{II}} \tag{4}$$

then the absolute deviation of the output voltage due to resistor mismatch can be expressed as follows:

$$\begin{aligned}\Delta V_O &= \frac{\partial T}{\partial R_I} \times \Delta R_I + \frac{\partial T}{\partial R_{II}} \times \Delta R_{II} \\ \Delta V_O &= V_{REF} \times \\ &\left\{\frac{-R_I R_{II}}{\left(R_I + R_{II}\right)^2} \times \frac{\Delta R_I}{R_I} + \frac{R_I R_{II}}{\left(R_I + R_{II}\right)^2} \times \frac{\Delta R_{II}}{R_{II}}\right\}\end{aligned} \tag{5}$$

The maximum is reached when

$$\begin{aligned}&R_I = R_{II} = 2^{N/2} R \\ &\frac{\Delta R_I}{R_I} = -\frac{\Delta R_{II}}{R_{II}} = \delta R \\ &\Rightarrow \frac{\Delta V_O^{MAX}}{V_{REF}} = \frac{\delta R}{2}\end{aligned} \tag{6}$$

In the case of two-stage voltage-scaling DACs, the worst deviation from the ideal output is at mid-scale too. The corresponding output is:

$$\frac{\Delta V_O^{MAX}}{V_{REF}} = \frac{\delta R_C}{2} + \frac{\delta R_F}{2 \times 2^{N/2}} \tag{7}$$

The overall accuracy is actually determined by the coarse resistor string. The matching of two identically designed resistors can be described as [4]:

$$\sigma_R = \frac{A_R}{\sqrt{W_R \times L_R}} \tag{8}$$

where A_R is a process-dependent coefficient. In the case of an N-bit voltage-scaling DAC, R_I and R_{II} are composite resistors, each of them composed of 2^{N-1} unit resistors. Hence the mismatch of the composite resistors is

$$\delta R_I, \delta R_{II} = \frac{1}{\sqrt{2^{N-1}}} \times \delta R \tag{9}$$

Eq. 9 shows an important advantage of voltage-scaling DACs as opposed to binary-weighed architectures: for the same accuracy, matching does not need to be very high. More details on resistor matching are given in Section III – Experimental results.

C. Major carry transitions and differential nonlinearity

For most input codes the on-resistance of the switches has little impact on the device operation as R_{ON} is low compared to the total resistance of the fine resistor divider. There are, however, some codes where R_{ON} directly affects the converter's differential nonlinearity. These are the transitions at which the fine divider is first connected across nodes M and M-1 of the coarse divider with all fine bits "1s" and then the

fine divider is connected across nodes M and M+1 of the coarse divider with all fine bits "0s", Fig. 3.

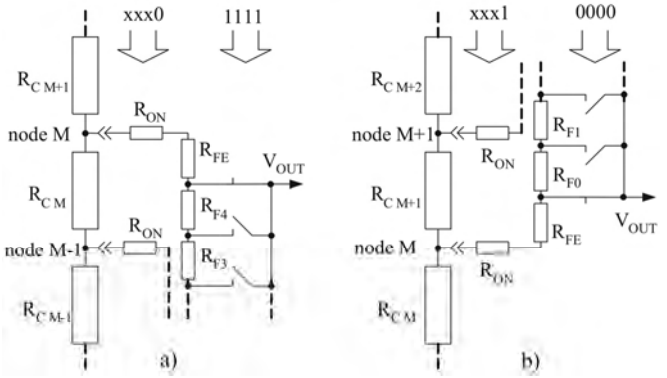

Fig. 3. Evaluating DNL

The voltage step for such a transition is:

$$\Delta V = \frac{V_{REF}}{2^{N/2}} \times \frac{R_C(1+\delta R)^2}{2^{N/2}R_L + R_C(1+\delta R)} + \frac{V_{REF}}{2^N} \times \frac{2\left(R_{ON}+R_{LE}\right)}{R_L} \tag{10}$$

If we take into account that

$$(1+\delta R)^2 \approx 1+2\delta R \qquad R_C << 2^{N/2}R_F \tag{11}$$

Eq. 10 can be simplified to:

$$\Delta V = \frac{V_{REF}}{2^N} \times \left(\frac{R_C(1+\delta R)}{R_F} + \frac{2\left(R_{ON}+R_{LE}\right)}{R_F} \right) \tag{12}$$

And the Differential Nonlinearity (DNL) can be expressed in least-significant bits (LSB) as:

$$DNL = \frac{R_C(1+\delta R)}{R_F} + \frac{2\left(R_{ON}+R_{LE}\right)}{R_F} - 1 \tag{13}$$

The first term of Eq. 13 represents the contribution to the total DNL of the coarse resistor divider. Its influence is negligible (Figs. 7 and 10), for δR=0 the first term becomes nothing but Eq. 3. The second term of Eq. 13 represents the influence of the switches. As R_{ON} cannot be made zero, the value of the R_{LE} resistors must be adapted to compensate for R_{ON} and keep DNL minimum:

$$R_{LE} = \frac{R_F - R_C}{2} - R_{ON} \tag{14}$$

D. Switch ON-resistance

The On-resistance of a closed MOS switch can be approximated as:

$$R_{ON} = \frac{I_D}{V_{DS}} \approx \mu \times C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH}\right) \tag{15}$$

Due to the body effect, the threshold voltage is not constant but varies with the voltage at the switch terminals [3][5]:

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{V_{SB} + \left|2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right) \tag{16}$$

where V_{T0} is the threshold voltage for zero voltage at the source, the V_{SB} is the source-bulk voltage and γ is a process-dependant body-effect factor. As a result, the switch on-resistance is not constant but varies with the voltage at the switch terminals. To alleviate the influence of the body effect, P- and N-MOS transistors are connected in parallel to make a complementary switch. Nevertheless, the body effect cannot be fully compensated for (see also Fig. 8).

D. Output impedance and speed

The major limitation of speed is the output impedance of the D/A converter. In contrast to the R-2R ladders, the output impedance of the potentiometer-type DACs varies with the input code applied. The maximum is reached at mid-scale:

$$R_{OUT} = \frac{1}{4}\sum R_F + \frac{1}{4}\sum R_F = 2^{N/2-2}\left(R_C + R_F\right) \tag{17}$$

The on-resistance of the switches that select the fine output must be added to this value. Two output types are possible:

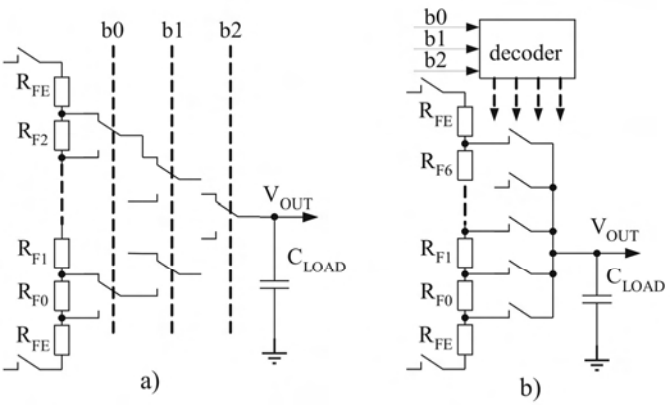

Fig. 4. LSB decoding

a) the binary-weighed tree (Fig. 4.a) does not need an LSB decoder; however, there are always N/2 switches connected in series and the total output impedance is:

$$R_{OUT} = 2^{N/2-2}\left(R_C + R_F\right) + \frac{N}{2}R_{ON} \tag{18}$$

b) The fully-decoded output (Fig.4.b) uses a decoder to control the switches that connect the output to the taps of the fine string. So the total impedance is:

$$R_{OUT} = 2^{N/2-2}\left(R_C + R_F\right) + R_{ON} \tag{19}$$

III. Experimental Results

A family of 10 and 12-bit potentiometric DACs was developed for a standard cell analog library. The converters were fabricated in standard CMOS double-poly, double-metal 1.0μm, 0.6μm and 0.35μm processes. The die photograph of the 12-bit two-stage voltage-scaling DAC is shown in Fig. 4.

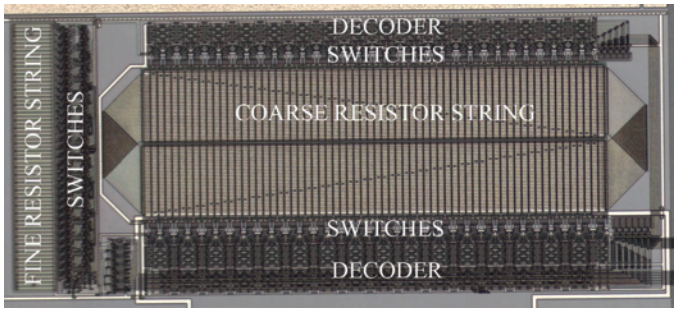

Fig. 5. 12-bit potentiometric DAC, die photograph

In Fig. 5 the matching results of 192 identical Poly1 resistors are shown. Using the same type of resistors, a 2-stage 12-bit potentiometric DAC was realized in a 1.0mm CMOS process. The INL and DNL of this converter are shown in Figs. 6 and 7. The coarse divider consists of 64 poly1 resistors and the fine divider consists of 63 poly2 resistors plus two smaller resistors at the ends of the string. The values of the smaller resistors were calculated according to Eq. 14 in order to compensate for the switch on-resistance. It is clearly seen that although the matching properties of the resistors used are not that good (approx. 1.04 % device mismatch), the INL of converter is much better – approx. 1.5 to 2.0 LSB. This is in agreement with the INL of 1.8 LSB predicted by Eqs. 7 and 9. The state-of-art layout that features common-centroid symmetry and equal wire lengths ensures pretty low nonlinearity. Along the DNL curves, the on-resistance of the switches used is shown versus the converter output. As predicted by Eqs. 7, 9 and 13, the overall INL is determined by the coarse resistor mismatch and the DNL is mainly determined by the variation of the switch-on-resistance along the output voltage.

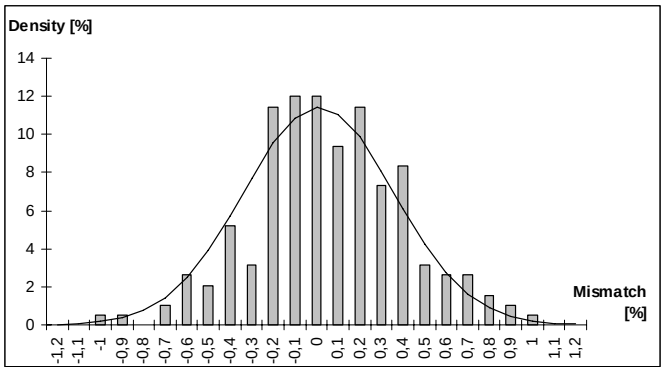

Fig. 6. Measured Poly1 resistor mismatch

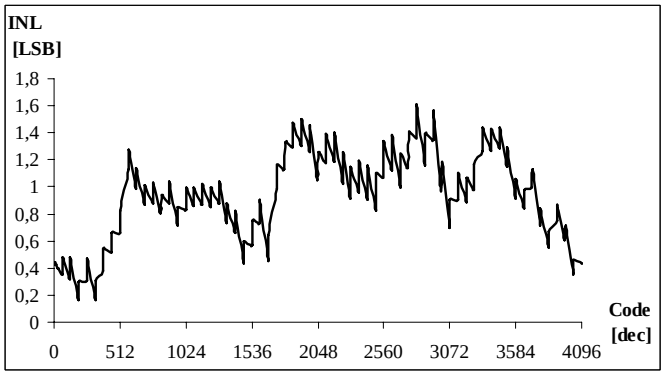

Fig. 7 INL of 12-bit voltage-scaling DAC

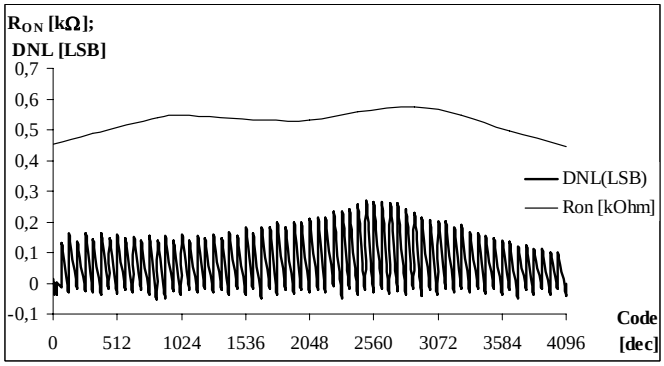

Fig. 8 DNL of 12-bit voltage-scaling DAC

IV. Conclusion

The potentiometer-type DAC is discussed in this article as a simple and effective way to guarantee monotonic D/A conversion. Two-stage topologies that circumvent the problems associated with buffer amplifiers are discussed in greater detail. The major sources of nonlinearities in potentiometric DACs are discussed. The derived expressions are proved by means of design experiments. Experimental results agree with the formulae derived in Section II. The developed D/A converters are very suitable for modern digital CMOS technologies.

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