Computer-Aided Engineering with the help of OrCAD

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***Abstract* – The design of modern electronic appliances always requires some suite of tools to be used. This paper is dedicated to a methodology for design with the help of OrCAD. Some recommendations and more common rules about the whole process of design – from starting a new schematic project, through the circuit description, electrical analysis and simulation, printed circuit board development and fabricating, till the bill of materials and some additional documents, are given as well.**

***Keywords* – OrCAD, PCD, CAE**

I. Introduction

In order to design a modern electrical appliance there is always a need to use some complicated software tools that allow entering and simulating of the electrical circuits, as well as development and preparing to fabricate the corresponding printed circuit boards.

The computer-aided design includes activities from two partially overlapping areas [1] – the automated electrical engineering as well as the drafting and documents automation.

The automation of electrical engineering, often noted as Computer-Aided Engineering (CAE), includes:

- Circuit description – the process of the circuit entering – as text (some languages for hardware description are used, mostly ABEL, VHDL or Verilog) or graphical form (some tools for schematic design are used, there are many of them).
- Circuit analysis – most of all it is a computer-based simulation of the circuit behaviour that could be analog, digital or mixed (analog-digital).
- Technical documenting of the design – some bill of materials, manufacturing and debug reports, operation and repair instructions, etc.

The final result of CAE is an electrical circuit, fulfilling the all requirements of the assigned task.

Some of the activities, included in the drafting and documents automation, often noted as Computer-Aided Design (CAD) itself, are:

- Fitting and placement the elements as well as routing the wires on a common pcb, although in many cases the result could be a monolithic or programmable integrated circuit (or even a system-on-a-chip).
- Some additional reports, intended for Computer-Aided Manufacture (some times noted as CAM), including so called Gerber files, drill files, mask files, etc.

Both activities are integrated in so called integrated CAE systems, or suits of tools, for example OrCAD, Protel, P-CAD, etc.

Next follows a brief discussion of the design flow with the help of OrCAD - one of widely used suits of tools for CAE. The presentation reflects the experience, collected in the Department of Electronics and Microelectronics, Technical University-Varna. OrCAD is selected mainly because of it is fully compatible with CADENCE – another well known integrated software system for computer-aided design of analog, digital and mixed integrated circuits.

II. Presentation

Fig. 1 is a diagram of the OrCAD design workflow [2]. The left side shows the activities (electrical and/or mechanical), that have to be done when entering the design, in the middle is shown the printed circuit board design and the manufacture and documenting activities are shown in the right side of the figure.

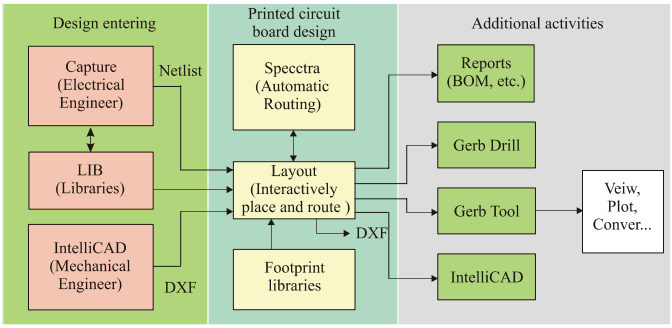

Fig. 1. Design workflow with OrCAD

The design process could be facilitated, as well as mistakes could be reduced, if the follow important steps are observed.

A. Preliminary activities

Before the beginning of a new project it could be helpful to do the next simple things, that allow better organizing of the design, facilitate its navigation, and make redesign (as well as errors fixing) easier:

- Define a simple and well organized structure of project folders [3]. OrCAD creates many files and holding them

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in one folder quickly becomes very confusing. It is much better in the folder, which will keep the project, to create a hierarchy structure. Thus each type of files should be written in its subfolder, which allows much easy navigation and cross-probing, corrections, etc. The specific structure of subfolders depends on the design, for example it could contain subfolders for files of: schematics, libraries, boards, datasheets of used components, assembly related documents, etc.

- Setting up the environment of the schematic should be the first step, especially when a new project will be created [2, 4]. It is important to check (and to change, if needed) the Options menu, which Preferences will be remembered in .ini file and will be used with every new customer, as well as the Design Template, which templates are common for all the next new projects.

B. Creating a new schematic project

Only now did the structure and environment define, a new project may be created, having in mind following specialties:

- What kind of new project will be created – this defines the specific libraries to be used in the project by default [2, 4] since in different cases the components will have different properties. In any case it is possible to use some components from different (type of) libraries, but it supposes a very good knowledge of the OrCAD properties (not only Capture, but PSpice, Layout and Specctra as well).
- Creating a schematic parts (or so called symbols) local library (.olb), as well as a library for the corresponding footprints (.llb) [3]. Although OrCAD creates a cached copy of the part symbol in the design file (which makes schematic project portable), it is preferable to create separate libraries for symbols (and later for footprints). They must be saved in subfolder, especially intended for them. It is a good practice to edit parts always in the library, not in schematics, as this will break the synchronizing between design and the (local) library. It is better avoiding so called heterogeneous parts, however in very large parts (processors, for example) they may be acceptable. Last, even though some standard parts have power pins invisible, making them visible can save a lot of time and trouble later.

C. Real work on the project

Depending on the schematic (Capture) or printed circuit board (Layout) editor is used the main tasks can be divided into two groups [3, 5].

- Inside the schematic editor Capture.
  - ✓ It is good to name all nets, that later will be require special routing rules. This concerns especially the ground and power nets, as well as some specific signals (high impedance input signals, common clock signals, powerful output signals, etc.). The explicit naming of nets is very useful and can be much helpful in the layout process.
  - ✓ A special attention must be paid to programmable logic devices, which behavior must be simulated inside the whole circuit. In some cases the PSpice model of the part can cause problem in Layout, which is possible to be fixed by deleting the model itself (the schematic property PSpice Template).
  - ✓ The annotation is another important step in preparing the design to export to Layout. It must be done including the hierarchical structure of the circuit. If the circuit has blocks that will be reused in the Layout, the option Tools/Annotate/Layout Reuse must be used in annotation, too. For schematics with more than one sheet (circuit pages), the option Add Intersheet References must be used. The DRC (Design Rules Check) must be always done before the netlist generation of the schematics.
  - ✓ It is a good practice to define in the circuit the most important properties that will be used later in the Layout. It concerns at least the PCBFootprint property, which can considerably facilitate the packaging of the circuit (i.e. the process of converting schematic symbolic parts to parts of the real world – like footprints of the elements). Although it is possible to do that in the Capture itself, for more complicated circuit is much easier to export them to Excel (Tools/Export Properties), make the all changes (Notepad will be useful, too), and import them back to Capture (Tools/Import Properties). Take in account that as the values of the elements are a separate property, it is important to have all elements with equal values with the same text notation in their value fields, else OrCAD will treat the elements with different text values (for example 100nF and 0.1uF) as completely different parts. This will complicate parts ordering and make part list (BOM) unreadable.
- Inside Layout (the printed circuit board editor).
  - ✓ The first step (after or even before the board outline is drawn) should be defining all the layers that will be used in the design (so called Board Stackup). As the Gerber files are close coupled with the layers, it is a good practice to define them here, although it could be done later too.
  - ✓ Next to define is the default padstack. The minimal size of the drill depends on the technology to be used, and must be entered into layers DRILL and DRLDWG. Each board shop has its requirements on the minimum annular ring size (the amount of metal beyond the size of the drill) based on the drill diameter, with a typical value of 20 mils (about 0.5 mm). If plane layers (POWER and GND) will be used a clearance around the drills must be defined, too. As a last thing, if a solder-mask is supposed to be used, it should be defined in layers SMTOP and SMBOT with a slightly large diameter (about 5 mils) than the annular rings. There is no need to define all the layers. As a common rule, the layers, that should be defined for thru-hole parts are: TOP, BOTTOM, INNER, PLANE, SMTOP, SMBOT, DRLDWG and DRILL; and for the surface mount parts they are: TOP, SMTOP and SPTOP. The default net properties should be checked in this point-the minimal width should correspond to the fabrication process to be used.

✓ After the board outline is defined is good to place the mounting holes first. If the boxes of their properties 'Not in Netlist', 'Fixed' and 'Locked' are not checked (which is a common mistake) the Layout will move them (or even delete) later.

✓ A common mistake is allowing Layout to do an automatic Place and Route, which could be acceptable vary rarely. The placement and routing of a board is much more an art than a science, and is best learnt by lots of practice. As the designer always knows how its circuit works, much better than any piece of software, the majority of manually placed and routed boards should be a higher quality than the automated. There are only a few cases (like memories board) when automatic place and route can do. Careful placement and routing can insure that the circuit board will perform to its fullest potential. The automatic placement and routing software tools have their place, but they should be used very carefully. Before the beginning of placement and routing it is good at least to specify which type is the board: a general analog, general purpose digital, high-performance analog, high-speed digital or radio frequency (RF). Of course most designs are a mix of the above board types, so the placement and routing strategies should be blended, too.

✓ Almost in any design the power and ground connections must be routed before anything else. It is a good idea to use as much as possible the interactively ways of routing (Edit Segment Mode as well as Add/Edit Route mode), but not the auto routing itself. For a successive interactive routing can be used the column Route Enabled from the Nets Spreadsheet, which allows enabling/disabling of the chosen net. A "good" ground means "low-impedance" of the ground (almost the same relates to the power connections). So the goal is to create a ground that has the lowest resistance at any frequency or board location. The ground plane is the best possible solution. Even if it is impossible to dedicate an entire layer to ground, large ground areas on both (top and bottom) sides of the board can come closer. In such cases the COPPER POUR option must be used. Active components which draw significant switching current should always be "bypassed". The typical value for bypass capacitor is 100nF, but two, or even three different values capacitors can be used to bypass different frequencies. When bypassing do not replace multiple capacitors with one single capacitor – it defeats the entire purpose of bypassing.

TABLE I
CLEARANCES FOR ELECTRICAL WIRES

Distance (clearance) between tracks			
Voltage (DC or Peak AC)	Internal layers	External layers	
		Sea level<3050m	Sea level>3050m
0-15V	0.05mm	0.1mm	0.1mm
16-30V	0.05mm	0.1mm	0.1mm
31-50V	0.1mm	0.6mm	0.6mm
51-100V	0.1mm	0.6mm	1.5mm
101-150V	0.2mm	0.6mm	3.2mm
151-170V	0.2mm	1.25mm	3.2mm
171-250V	0.2mm	1.25mm	6.4mm
251-300V	0.2mm	1.25mm	12.5mm
301-500V	0.25mm	2.5mm	12.5mm

✓ Only after the ground and power nets are routed, is time to continue with the rest connections. For multi-layer responsible boards and the inner layer wires must be wider, than those of outside (top and bottom) layers. As a common rule, each track should be as short as possible. The clearance definitions must take in account requirements of the fabrication process, the layer position (internal or external), the voltages, the operational height of the board over above the sea level, etc. Table I allows roughly definition for the clearances.

- Final steps should be taken to finish the board and prepare for production.

✓ The OrCAD suggests two possibilities – the ECO (Engineering Change Order) and Back Annotation. The first one is used from inside the Capture (so called forward annotation, i.e. when changes are made in schematics), and the second one is used for changes made during Layout. The renaming of components in the board is at least one example where is good to use back annotation. During debug on a larger board it could be very hard to find where a specific component is, because components seem to be named randomly. Using the Options/Components Renaming (and Right, Down in the rename directions) in Layout will be a good turn to the debug engineer.

✓ The next step is to check for any spacing errors (DRC – Design Rule Check). Instead of trying to remove errors manually (one by one), the Auto-Remove Violations tool could be use, but this is not a good idea – it will actually rip-up offending traces and move parts, so a lot of cleanup and rerouting after using this tool should be done.

✓ Cleaning up the design is a step before the final, which includes mitering the corners and exits from the pads, removing extra vias and drill size adjusting. The last means to adjust (consolidate) the drill sizes in accordance to the board shop limitations. It is a good practice to consolidate drills anyway (this will save money at least). Another good practice is to adjust the silkscreen layer - all text should be oriented in the same direction for readability and it cannot overlap pads or vias. A good documenting of the design helps both in manufacturing and debug. It is useful to add some useful text to the board, for example the names of some important nets and pins, as well as the initials of the person who designed it. In the special layer Drill Drawing should be added the Drill Chart and the board dimensions. It is good practice beneath the drill table to include the name, phone number and email of the designer. Because a separate Gerber file will be generated for each layer, outside the boundary of the board some text could be added, to indicate what layer this is.

✓ The last step is creating and viewing the Gerber files that will be sent for fabrication. If they had been defined as was suggested in the beginning generation now is quite easy – just Auto-Run Post Processor must be selected.

OrCAD has a built-in Gerber viewer and editor called GerbTool. In fact, this is a very powerful program that allows viewing and editing of the Gerber files – it is often to catch mistakes in this program that are not seen in layout.

- ✓ To finish the work is good to cleanup the project folder – OrCAD generates a lot of files that can be deleted (if necessary, they can be generated again). The files that must be kept are: for Capture - project (.opj), design (.dsn) and library (.olb) files; for Layout – netlist (.mnl), library (.llb), template (.tpl) and the board (.max) files; for Gerber – all the layers files.

III. Conclusion

In this paper a concise review of some important activities of electrical appliances design methodology with the help of OrCAD are given. Following the shown consecution should lead to lower mistakes in the design process, better and more reliable printed circuit boards, as well as easier to debug, redesign and maintenance devices. Most of the given recommendations are applicable not only to OrCAD design, but to all designs that use some modern CAE systems.

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