One Solution of Portable Pulse Generator Design

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Abstract – **This paper describes methodology of design and construction of pulse generator designed for laboratory testing of effect of electrical pulses on metabolism of micro organisms. The device is realized as a portable device with substantive battery supply, and it is based on integrated circuits in CMOS technology with minimal consumption. Frequency synthesis is realized by using PLL circuits and two specially constructed counters which realize multiplication and division of referent oscillator frequency.**

Keywords – **FPGA, PLL, pulse generator**

I. INTRODUCTION

Recently, the attention of microbiologists is increasingly directed towards research of micro organisms' electrical activity. The results of some researches imply that the most micro organism, especially morbid ones', manifest significant bioelectrical activity with frequencies ranging up to 1MHz, [1]. Moreover, a possibility of inhibitory effect on micro organisms' metabolism has been observed, achieved by electrical pulses of adequate frequency, which is especially efficient if the pulses are unipolar. Particularly interesting in this sense are rectangular unipolar pulses with duty factor near the value of 0.5 which, except for their effect on frequency of the fundamental harmonic, also enable the simultaneous effect on several frequencies that correspond to higher harmonics (especially to third and fifth one).

For several years it has been possible to find pulse generators originated from this type of researches on the market in western countries. Such devices have evolved from simple, astabile multivibrators based on NE555 integrated circuit into very complex microprocessor based systems.

Functional requirements imposed on such devices are following:

- generation of unipolar rectangular signals with frequency up to 1MHz and amplitude up to 15V,
- possibility to program the length of working intervals ranging from 1 to 30 minutes,
- under load and overload output protection,
- user friendly interface,
- battery supply with as many working hours as possible.

A representative of this class of devices [2] has been analyzed in detail, and the following serious deficiencies are noticed:

- only basic frequency of 30kHz was realized, and to obtain any other frequency requires a separate module to be purchased,
- the consumption of the device is comparatively high and the lifetime of battery elements (AA/LR6, 3 pieces) is relatively short, about 10 hours, and finally,
- the user interface is fairly scant (light diodes, keys and sound indicator).

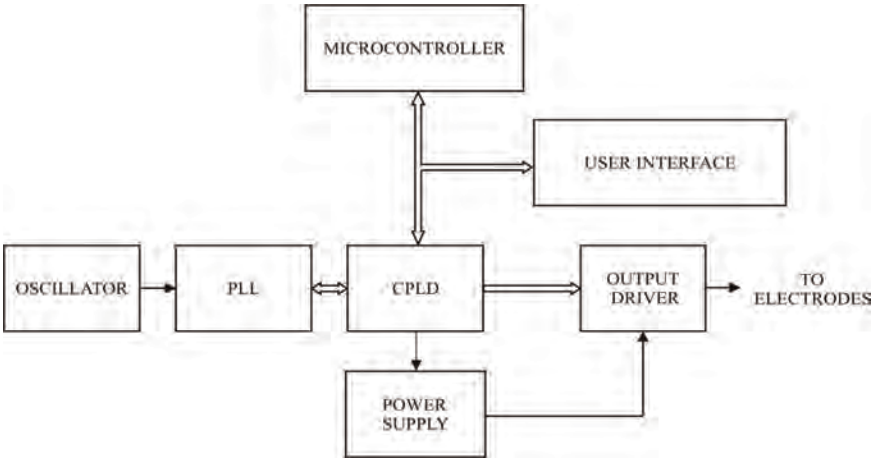

Fig. 1. Global structure of device

In endeavour to resolve the perceived deficiencies, the authors have constructed an entirely new pulse generator. The functional characteristics of this device are verified in laboratory tests of three manufactured prototypes.

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In comparison with competitors [2], this device displays considerably better functional capabilities, and at the same time it is significantly cheaper.

II. Device Description

Global structure of the device is represented in Fig 1. The main functional task – synthesis of rectangular signals of a given frequency – is realised by PLL based on integrated circuit 74HC4046, Fig 2. It is a component realised with HCMOS technology and optimised for work on low voltage of supply (3-6V) with the maximum supply current of approximately 0.5mA on working frequencies up to 1MHz. Among other things this device contains a VCO and 3 phase comparators. It is mass produced and has a low price. In this case we used a phase comparator II which is susceptive to signal edges, and associated passive R/C components are calculated in such way to cover the frequency range of 30kHz to 1MHz.

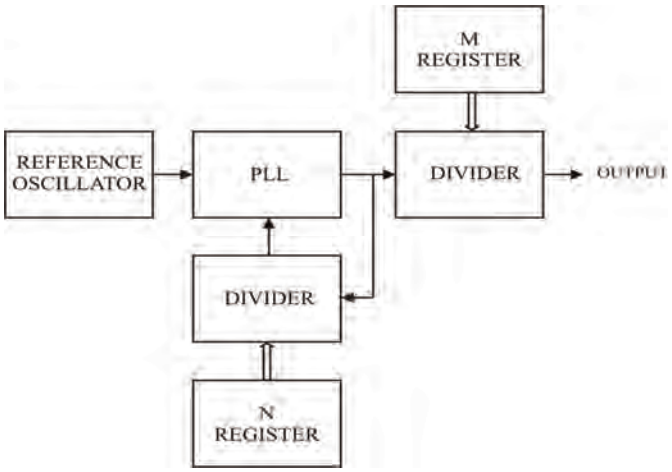

Fig. 2. PLL circuitry for frequency synthesis

Reference oscillator is based on integrated circuit 74HC4060, controlled by a cheap crystal unit 32768Hz ($f_0 = 2^{15}$ Hz). This frequency has been chosen for the following reasons:

- it is easy to attain frequency multiplication up to required 1MHz with associated 6-bit dividers,
- the microcontroller is disburdened from the basic task of frequency synthesis and this working frequency is high enough for remaining tasks (servicing of the user interface, time control, supervision etc.), which significantly decreases its power consumption,
- arithmetic operations are significantly simplified in the process of divider coefficient calculation, because multiplication and division with 2^{15} can be realised by simple operations of bit shifting.

PLL circuitry has two frequency dividers constructed exclusively for this application. These are 6-bit frequency dividers with the possibility of frequency division in 1-64 range with preservation of almost ideal duty factor (0.5). Division coefficients are held in 6-bit associated registries N and M, which are directly accessible by the microcontroller, so that the overall process of given frequency synthesis is reduced to calculation of optimal values of dividers, and synthesized frequency has the value:

$$F = f_0 * N/M \quad (1)$$

Such dividers are not produced as commercially available integrated circuits, therefore their functionality is realised by complex programmable logic circuit (CPLD) Xilinx XCR3064XL. This component leaves enough resources for a number of additional functions (control and status registers, microcontroller glue logic, subsidiary counters etc.). In this way, the number of integrated circuits in the system is considerably decreased and the layout of the PCB is simplified. Moreover, XCR3064XL has low consumption that is in this case estimated to be at most 0.1mA. Finally, available development tools [3] make the implementation process (structure description in VHDL, functional simulations and verifications, component translation and programming) uncommonly efficient.

Based on criteria such as consumption, price, availability of development tools and available internal resources, for the working microcontroller we have chosen PIC16F84A of Microchip [4]. It belongs to a widely used microcontroller family with the following characteristics:

- 14-bit RISC core,
- 1024 words of program FLASH memory,
- 68B RAM memory,
- 64B EEPROM data memory,
- upper limit frequency of 20MHz,
- 18-pin DIP enclosure.

Device is supplied by three battery elements of AA/LR6 type, generating from 3V to 4.5V. Input protection from inverse voltage is built in, as well as the possibility that the microcontroller, after end of work, automatically shuts down the whole device in order to reduce consumption. The voltage of battery elements is controlled through two comparators based on LMV339 circuit and a voltage reference LMV431. When the voltage on one element falls below the value of 1.1V, the first comparator signalises the low battery status to the microcontroller, which is shown to the user by periodical blinking of a LED diode, and when it falls under the value of 1V, microcontroller will automatically shut down the whole system. In this way it is possible to utilise almost the entire stored energy, with protection from over exhaustion of elements that could lead to electrolyte leakage.

The voltage supplied for digital circuitry is 3.3Vdc nominal and it is a product by LDO regulator LP2981. This circuit is characterised by extremely low allowed value of input-output voltage dropdown of only 20mV with a normal working current of 5mA, which allows emptying of battery elements to the minimal working voltage of 3V for the built in integrated circuits i.e. 1V per element.

Generated pulse series is transferred from LVCMOS voltage level to desired output voltage level (6-12V) by

translator circuit MC14504. This circuit is supplied by DC/DC converter based on switching regulator MAX608 that has a characteristic of low consumption and low working voltage.

The converter topology is classical "*boost*", and the user tunes output voltage through rotation pot. Both transformer and voltage translator have built-in over current protection, and the remaining two comparators from LMV339 component follow the device's output current and signalize the state of current overload and low-supply to the microcontroller.

In comparison to the commercial solution, the elements of user interface are extended so as to give a higher degree of user interactivity. The concept of photo signalization using LED diodes and audio signalization using signal buzzer is retained as suitable, both from functional and energy point of view. The number of keys is increased to three in order to ease movement through user menu. LCD display, type PVC60101, is introduced with possibility to write 16 alphanumerical characters that are used in the starting phase of setting the working parameters (frequency, time interval), as well as for display of messages.

III. Design Methodology

During the beginning phase of project the working principles of device and functional requirements have been analysed from the user's point of view, as well as the construction of existing commercially available solutions. Based on these circumstances, the functional criteria that designed device should realise were established and the global pointers for construction of some of its subsystems were given.

Special attention was given to the frequency synthesis - the basic function of the device. The structure, PLL plus two dividers, is adopted as the most perspective, and then the detailed research in order to establish the optimal value of referent frequency and counting range were carried out. A separate program was written in C programming language, which was executed on a personal computer and which analysed the set of frequencies that could be generated. The result was that with the reference frequency of 32768Hz and 6-bit dividers it is possible to cover desired frequency range (0.5 kHz – 1MHz) with 2485 different values, which is satisfactory covering density.

Further work went on in two directions. The first one was related to solution to the problem of calculation of optimal values of coefficients N and M based on output frequency F and reference frequency f_0. In this sense, a distinctive algorithm was developed and was firstly implemented and verified as a program in C programming language on a personal computer, and later is was translated into assembler code for the target microcontroller. The other direction was related to solution to the problem of frequency divider synthesis, and the result was a verified and optimised code in VHDL that was afterward translated for target CPLD.

In the following phase, the components were chosen and the design of remaining segments of the system was carried out, which resulted in electric scheme and bill of material. The delivery time of components was used for designing the device PCB (printed circuit board), choosing the enclosure and planning of the elements installation.

For the needs of (re)programming of CPLD circuits, a low voltage version of Xilinx parallel download cable was developed, which was completely compatible with manufacturer's existing programming tools and specifications of parallel port of a personal computer, and which enables safe work with components with supply voltage of 2.5V or 3.3V.

The complete process of writing and testing of the software for Microchip's microcontroller was carried out within the interacted development environment of this manufacturer - MPLAB IDE version 6.10. For the optimisation reasons, the program code was written in assembly language and MPASM translator and MPLINK linker were used as programming tools. The programming of the microcontroller was conducted through a programmer especially constructed for this purpose. It consists of probe that contains microcontroller and four-pole relay, used to place the microcontroller into working or programming regime. The relay is controlled through a switch that is based on the programmer connected to a personal computer through a parallel port, and to a laboratory voltage supply. In this way the development and the testing of program support was considerably accelerated, because no time was lost on physical transfer of microcontroller between device and programmer.

After the completion of development, the device was thoroughly tested in laboratory conditions. Stable work was confirmed with overall current consumption under 20mA, which guaranties over 50 working hours using standard battery elements. Out of 20mA, only 3.4mA are used for internal supply, remaining current flows through the external load (body).

IV. Conclusion

In this paper, the construction and development process of the device was described, starting from the prototype level that was verified in laboratory conditions. With careful selection of components and appropriate design steps, the quality of the solution that significantly surpasses the commercially available devices in the same category was achieved.

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