# One Easy-to-Implement Method for BER Performance Testing of Uncoded Ultrahigh Capacity (Gbit/s) Radio Link

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*Abstract* - **In this paper we describe method for bit error ratio (BER) performance testing of uncoded ultra high capacity radio links, which key features are: simple modulation techniques which yields to high rate serial data streams (up to 1Gbit/s) and huge BER range (from 1E-2 to 1E-12). Algorithm for parallel signal processing for PN sequence generation at transmitter site and synchronization to incoming PN sequence at receiver site is described in details. Some remarks about FPGA/CPLD and microcontroller software implementation are given.**

*Keywords* – **BER testing, digital radio, paralel signal processing**

## I. INTRODUCTION

Bit Error Ratio - BER is one of basic parameter of digital communication system [1]. Therefore, its measuring is one of basic measurement. The basic idea is to simulate information source by PN sequence generator [1]-[4]. The communication system transmits this sequence. During transmission errors occurred. To detect these errors at the receiver site it is necessary to have reference PN generator the same as transmitted, and errors represents the difference between incoming and reference sequence (Fig 1.).


Fig 1. BER measuring

The ratio between the number of errors $N_{err}$ and number of transmitted bits $N_b$ is called bit error ratio *BER* and in limit process it yields to error probability $P_e$.

$$BER = \frac{N_{err}}{N_b} \xrightarrow{N_b \to \infty} Pe \qquad (1)$$

BER measurement is very important in digital radio, since it should satisfy required performance in spite of presence of various types of feding. Therefore usualy radio systems are equiped by various types of forward error correction FEC mechanizms. As a consequence in digital radio BER as a system measure has very large range from as low as $10^{-12}$ to above $10^{-2}$. According to this, synchronisation algorithm and error pulses processor are crutial components BER measurment equipment.

In ultra high capacity digital radio interfacing problems between radio components and BER measiring euipment significantly increases especialy in early radio design testing phases. One of remedies to this is to implement BER measuring features in radio itself, usualy in FPGA chips. One such method is presented in this paper.

## II. CLASICAL APPROACH

First we should consider clasical aproach in designing BER testing circuitry. The structure of PN generator (Fig 2.) is well described in [1]. The length of PN sequence should be enough that its discrete behavior does not effect the behavior of telecommunication system, especially in clock and carrier recovery. ITU-T have standardized PN patterns according to system capacity [3], and reactions in PN generator (Fig 2.) are defined in it. For high capacity systems usually $2^{23}$-1 and $2^{31}$-1 are used.

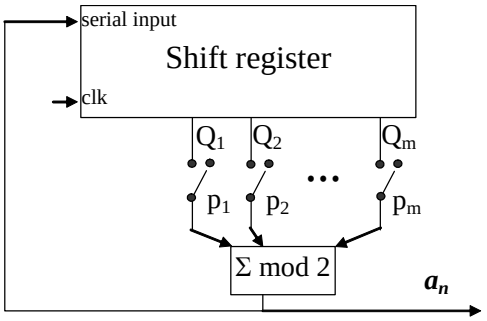


Fig. 2. Classical PN generator

The basic problem in BER measuring is synchronization of reference PN generator to incoming sequence. Very simple idea, that could be derived from functioning self synchronous scrambler is given in [2], so called close loop synchronization. The concept (Fig. 3.) is at the beginning of synchronization data from line are directly copied into shift register (switch

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position 1). When shift register is full, the reaction is closed (switch is moved to position 2). If error did not occurred during data coping the reference PN generator is synchronized to incoming sequence. If the error occurred corresponding error rate between reference and incoming sequence is close to 0.5. In practical systems it is rarely necessary to estimate BER higher than 0.1, so we would focus on this limit. The crucial question is how long sequence $(N_b)$ should be, and how many errors $(N_{err})$ should be measured to determine this "false synchronization". Too long sequence would lead that slip occurrence would not be detected, and BER meter would give high error rate. On the other hand, too short sequence would lead that false loss of synchronization alarm may be caused by error multiplication process. This problem is described in details in [4], and it is shown that detecting $N_{err}$= 51 errors in a sequence shorter than $N_b$ =511 bits is adequate for the most of purposes of testing data transmission systems without forward error correction (FEC) which have very high BER.

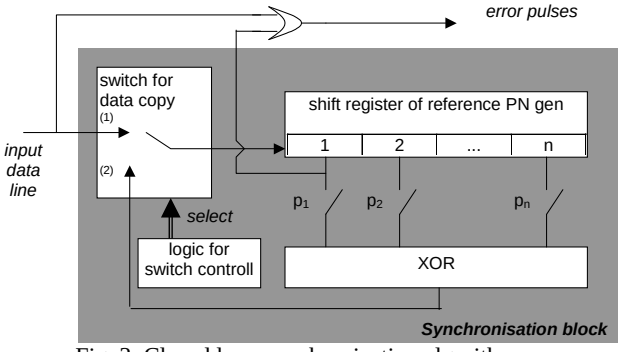


Fig. 3. Closed loop synchronization algorithm

On the other hand, requirement for residual BER of a high capacity digital radio is $10^{-12}$ [6]. The crucial question is how long should measurement last to confirm such state. The answer is in determining confidence limits of BER described by equation (1) as a estimate of $P_e$. In [6] is proposed algorithm for measuring BER with predetermined confidence for binomial distribution of errors. In [7] formula for confidence limits for Binomial, Poisson distribution of error process, and for BER as a Normal distribution process are given. According to this we created Table I. It is obvious that data for Binomial and Poisson distribution gives very close results, while for normal distribution slightly differs.

TABLE I
CONFIDENCE LIMITS CL FOR VARIOUS DISTRIBUTIONS

| *conf. level* | $N_{err}$ | Distribution | | |
|---|---|---|---|---|
| | | Binom. | Poisson | Normal |
| 1-α = 50% | 0 | 0 | 0 | 0 |
| | | 1.39 | 1.39 | 0.45 |
| | 10 | 7.73 | 7.73 | 8.08 |
| | | 13.00 | 13.02 | 12.37 |
| | 100 | 93.37 | 93.09 | 93.48 |
| | | 107.17 | 107.58 | 106.98 |
| 1-α = 99% | 0 | 0 | 0 | 0 |
| | | 5.28 | 5.30 | 6.63 |
| | 10 | 3.73 | 3.72 | 4.52 |
| | | 21.28 | 21.40 | 22.11 |
| | 100 | 77.02 | 76.12 | 77.35 |
| | | 126.88 | 128.76 | 129.29 |

Constructing BER measuring device directly according to given principle is restricted by FPGA device speeds which nowadays is slightly higher than 500MHz [8]. However entire system could be parallelized, which made possible realization of multi Gbit/s devices by using ultra high speed parallel/serial converters that are usually placed on many novel FPGA devices like Xilinx RocketIO [8]. We would describe such modification in details in this paper.

The very important results from Table I for low residual BER measurements, are upper confidence limit when zero errors are measurement. According to this significant saving in measured time could be achieved.

## III. BERMETER CONCEPT

### *A. Parallel signal processing architecture*

The basic structure of modern ultra high speed signal processing is shown in Fig. 4. The total bit rate is divided into several low bit rate branches and than serialized by clock multiplier and high speed ser/des register. Ratio between high and low speed clock *Rsd* is usually 8, 16 or 32.

On the receiver side, high speed clock is recovered (*RxClk)*, and at that clock data are shifted into shift register and at every *Rsd* pulse copied into parallel register. Than follow the parallel synchronization algorithm that resolve the delay. After it the data that origins form the first processing branch on the transmitter site, occurs at the first processing branch on the receiver site.

The only limitation for such processing construction is that there is no infinite feedback on successive *Rsd* data bits. In that manner exact value of the signal after Rsd clocks could be calculated. For this purpose we find symbolic calculation in Wolfram Research Mathematica software very useful.

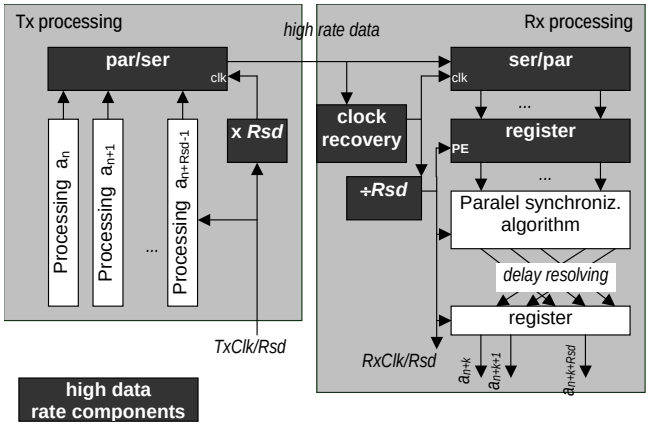


Fig. 4. General parallel signal processing architecture

### *B. Parallel PN generator*

On the example of PN sequence $2^{15}$-1, we would describe behavior of parallel PN generator. In classical serial PN generator:

$$a_1(n+1) = a_{15}(n) \oplus a_{14}(n), \qquad (2)$$
$$a_i(n+1) = a_{i-1}(n), i = 2,...,15$$

where $\oplus$ denotes modulo 2 addition, or *xor* logic gate.

To parallelize this algorithm into Rsd=8, we have

$$a_1(n+1) = a_{15}(n) \oplus a_{14}(n),$$
$$a_1(n+2) = a_{15}(n+1) \oplus a_{14}(n+1) = a_{14}(n) \oplus a_{13}(n+1), \qquad (3)$$
$$...$$
$$a_1(n+8) = a_{15}(n+7) \oplus a_{14}(n+7) = a_8(n) \oplus a_7(n),$$

which yields of structure of two eight bit registers (Fig 5).

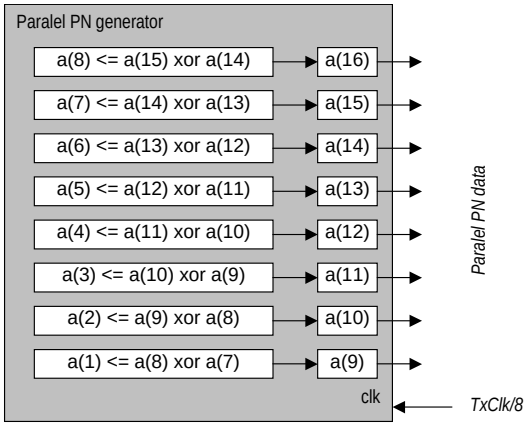


Fig. 5. Parallel PN generator in $2^{15}$-1 case

We also must mention that logic for avoiding forbidden state of all zeros in this case should be added. Such logic could be very easy become a botle neck of the system and therefore it partitioning and fiting into FPGA device should be done with great care.

*C. Parallel Error detector*

Fortunately, for parallel PN error detector only number of errors should be measured, but error positions are not necessary. Therefore delay resolving logic could be skipped. This give us opportunity that corresponding structure could be constructed very directly (Fig 6).

For switch control in synchronization process instead of adding errors in accumulator register, symbol error signal could be used. Since symbol error probability is about *Rsd* times higher than BER, the lower bound of measurement is decreased to about 0.1/Rsd. For most radio application such reduction is not critical.

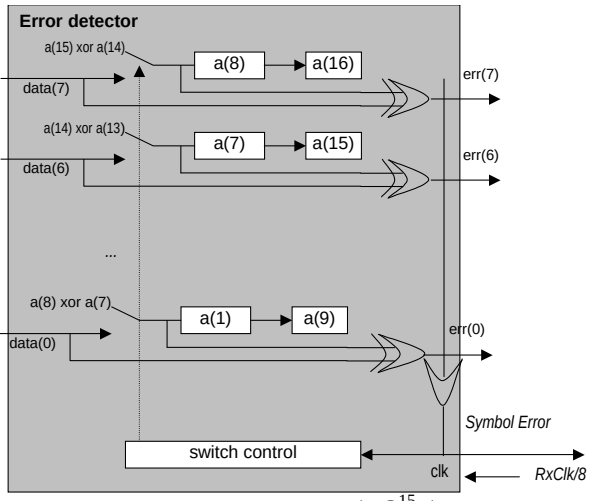


Fig. 6. Parallel Error detector in $2^{15}$-1 case

*D. Error pulses processing*

The major difference to classical implementation of BERmeter is that accumulator for error addition should be implemented instead of error counter. Although Rsd times slower than the bit rate, such implementation may cause problems at high speed operation problems. One of possible solution is to implement Rsd parallel error counters, and add its values at the end of measurement time. If the measurement time is fixed (usually 1s) than only limitation is FPGA-microcontroller data bus speed, which is usually not critical.

For basic error tests measurement with predetermined confidence could be implemented. Such method drastically decreases measurement time, and may be very useful during development phase of a radio system. According to model given in [4][7] a look up table is created that have a number of errors that should be counted for given confidence level $n_e(\alpha,cl)$. Until given error number is not reached, the symbol counter counts transmitted symbols. When it is reached, the counting stops, and BER is calculated and displayed. BER calculation logic could be simplified if only BER order of magnitude indications should be given by LEDs. Than it consists only on SR flip flops that are preseted when number of symbols passed certain value. For example if required number of errors is equal to 80, and Rsd=8, than SR latches are reseted at the beginning and preseted if symbol counter passed though state of 10, 100, 1000 etc.

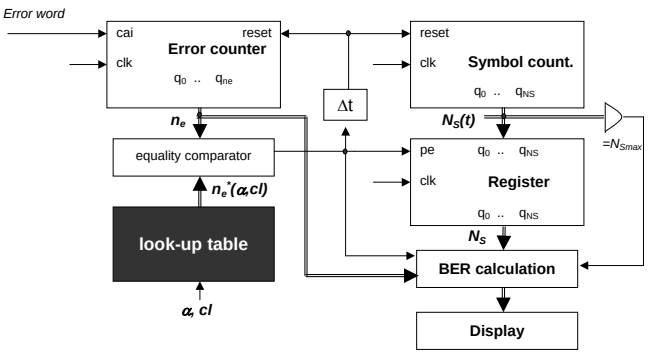


Fig. 7. Predetermined confidence BER measurement hardware

## IV. PRACTICAL IMPLEMENTATION

The model of such BER meter is designed for data rate of 155Mbit/s and could be easily extended to 622Mbit/s (Fig 8, 9). Instead of radio device, fiber optic interface is used [9], and error injection is performed with optical signal attenuation. This model could be easily adopted to 60GHz radio with ASK or DBPSK modulation, where instead of optical interface base band PECL level signal should be fed to microwave mixers at the transmitter and receiver.

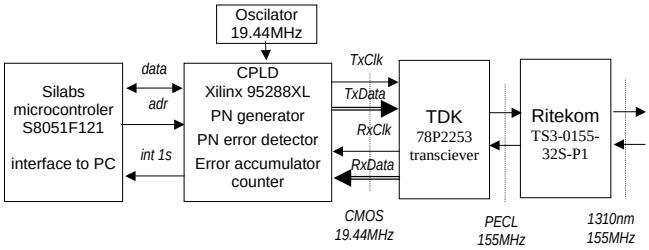


Fig. 8. BERtester model block diagram

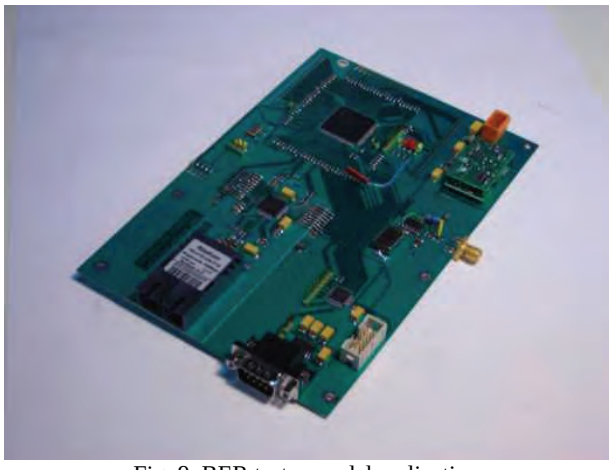

Fig. 9. BER tester model realization

Entire parallel processing is implemented in a Xilinx CPLD 95288XL device [8], operating at only 19.44MHz. As a serializator with clock multiplier, and deserializator with clock recovery circuit a TDK 78P2253 transceiver is used [10]. For interface with PC Silabs microcontroller S8051F121 is used. The microcontroller performs BER calculation and each second it transmits data to PC via serial RS232 interface.

Given platform is used to test prototype of high capacity digital radio with following parameters:

- Modulation type: QPSK, 16QAM and 128QAM
- FEC: uncoded, inner convolution code with Viterbi decoding and outer ReedSolomon(255,251)
- System capacity: 35, 70 and 155Mbit/s

Flat fading is simulated by variable attenuators, while selective fading is simulated by specialy constructed lattice filter. Cycle slips are simulated by punching local oscillator circuitry by rubber hammer.

Constructed BER tester model shows that it could easilly measure BER up to 2 $10^{-2}$, and accurately detect cycle slips. Long term monitoring testing gave result of zero errors in 16 hours, which according to Table I yilds to residual BER lower than 7.4 1E-13.

## V. CONCLUSION

Described method for BER testing is very easy to implement in almost any FPGA or CPLD structure. High speed serialiser/deserialiser could be external component, as described in model, or internal resource of an FPGA chip. Algorithm could be used for measure BER from $10^{-2}$ to as low as $10^{-12}$, and therefore used both for FEC coded or uncoded systems. Practically implemented model could be used both for fiber optics and ASK/DPSK ultra high rate digital radio.

## ACKNOWLEDGEMENT

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