Development and Spice Simulation of Current Mode Control System for Multiphase Full Bridge Transistor DC-DC Converter

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Abstract – **A multiphase full bridge transistor DC-DC converter with PPhM (pulse-phase modulation) and current mode control system is developed and simulated in the present paper. Using programmable logical inputs, the system can be configured to control two, three, or four converters. The work of the control system with four-phase bridge transistor DC-DC converter is simulated using the OrCAD PSpice program.**

Keywords **–Full bridge transistor DC-DC converter, Pulse-phase modulation, Control system, PSpice simulation**

I. INTRODUCTION

Multiphase DC to DC conversion is applicable when output current significantly exceeds the nominal current specified for each individual semiconductor in use. At the same time the ripple frequency equals the frequency of a single phase converter multiplied by the number of phases which reflects into smaller and less heavy filter components as chokes and capacitors.

This approach is well known from the SCR DC-DC era [1], when the semiconductor switching frequency limitation was a major factor. The significant clock frequency increase in the modern CPUs, recently put a lot of pressure to decrease the supply voltage and therefore to enormously increase the supply current. To meet these new requirements the IC manufacturers came up with specialized chips supplying multiphase control to DC-DC converters. A typical example is Texas Instruments TPS40090 [2]. A typical feature of all these ICs is that they are all designed for parallel operation of multiphase Buck converters.

In the present paper a multiphase bridge DC-DC converter is developed, based on current mode Phase Shifted PWM DC-DC converter with a transformer output and a current-double rectifier [3].

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II. CURRENT MODE CONTROLLED PHASE SHIFTED FULL BRIDGE INVERTER WHITH CURRENT-DOUBLE RECTIFIER

The DC-DC converter from [3] is based on voltage control. Paralleling the outputs is done by active current sharing using a specialized IC - UC 3907 and the multiphase principle is difficult to be realized.

In [4], [5] and [6], charge current mode control with Buck DC-DC converters is revealed. Appling the same approach on Phase Shifted PWM bridge converter with current-double rectifier will be discussed next.

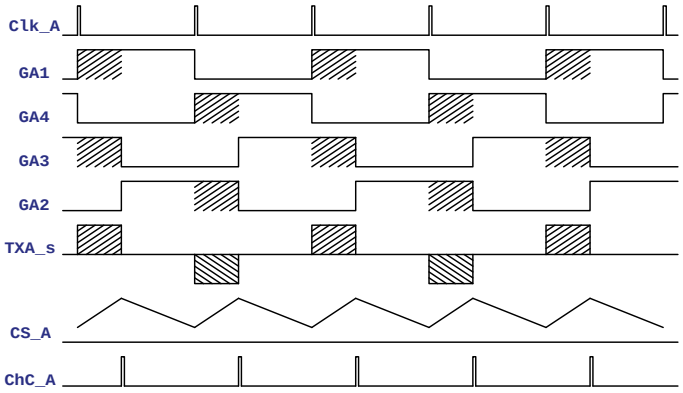

Fig. 1. Principle of operation of current mode Phase Shifted PWM bridge transistor inverter

Phase Shifted PWM bridge inverter basic principle of operation is shown in Fig.1. Clock signal Clk_A feeds a T-flip flop which outputs Q and $\overline{Q}$ used for driving of one inverter leg (GA1 и GA4). The same signals are also used for synchronization of another externally clocked R-S flip flop which outputs the second leg gate drives based on ChC_A (Fig.2).

Externally clocked R-S flip flop schematic diagram is shown in Fig. 3. Q and $\overline{Q}$ are inverted to each other and are meant to drive the second inverter leg (GA2 и GA3).

ChC_A is generated at the peak of the rectified output current (Fig. 4).

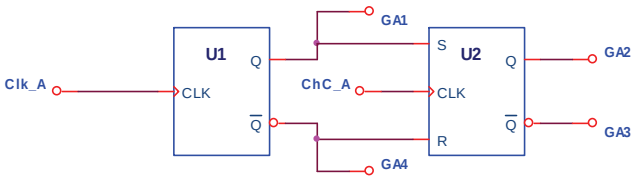

Fig. 2. Full bridge gate drive generation

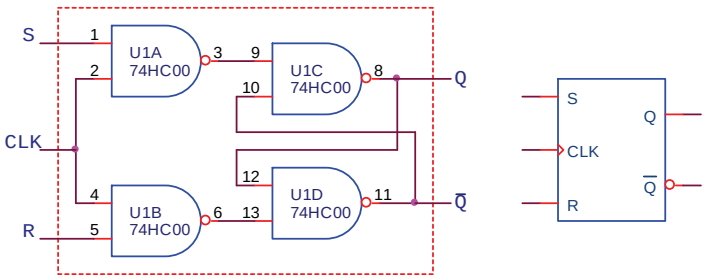

Fig. 3. R-S flip flop internal diagram with external clocking

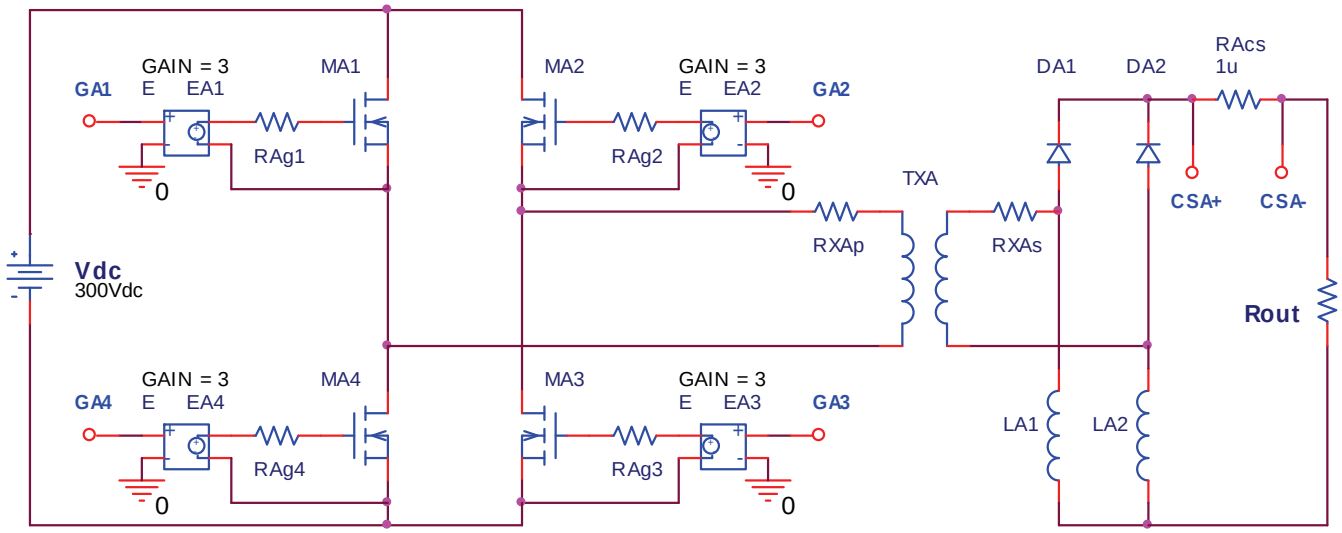

Fig. 4. Current mode Phase Shifted PWM full bridge transistor inverter

Phase shifting between GA1-GA4 and GA2-GA3 (waved areas in Fig. 1) is a function of the following parameters: choke value LA, load impedance R_{out} and the output current reference. TXA_s is generated in the transformer secondary coil TXA.

A charge current mode controller is illustrated in Fig. 5. Rectifier output current is tracked across a sending resistor Racs. Current to voltage converter GCSA charges capacitor CAch up to a voltage proportional to the integral of the output current for the time while it is rising. Switch SA is open for the duration of this time and is closed while the current is falling thus shorting capacitor CAch. Control to SA is given by U1A, U1B and U2A. As soon as capacitor Cac is charged up to the reference voltage +Vref, comparator U3A generates ChC_A which clocks the R-S flip flop (Fig. 2).

III. Four-Phase Current Mode Controlled Phase Shifted Full Bridge Inverter whith Current-Double Rectifier

Four-phase full bridge DC-DC converter is controlled by current mode Phase Shifted PWM system. Its principle of operation is illustrated using the timing diagrams shown in Fig. 6. Its topology is made of four identical stages similar to the one in Fig. 4. These are indexed A, B, C and D just for the purpose to make difference for the *PSpice* simulator.

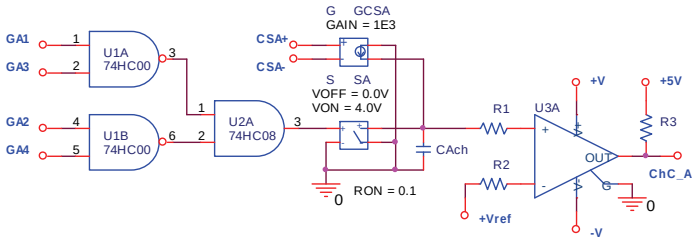

Fig. 5. Charge current mode controller diagram

The same indexing applies to their components as well. Each converter has its own charge current mode controller as shown in Fig. 5.

Clk_A, Clk_B, Clk_C and Clk_D pulse sequence is generated by a quad clock as the time between two neighboring pulses equals the master period divided by the number of phases. Fig. 7 shows how these pulses take part into the bridge gate drive sequence.

The first two components (U1 and U2) match with those in Fig. 2. Their functional inputs and outputs carry the suffix A and are meant to control the first DC-DC converter (A). U1 and U2 are considered master controllers as the rest (U3 through U8) are following them. U1 and U2 phase is 0 as the rest controllers are synchronized against them through GA1 and GA4 which are applied to R and S inputs of R-S flip flops U3, U5 and U7.

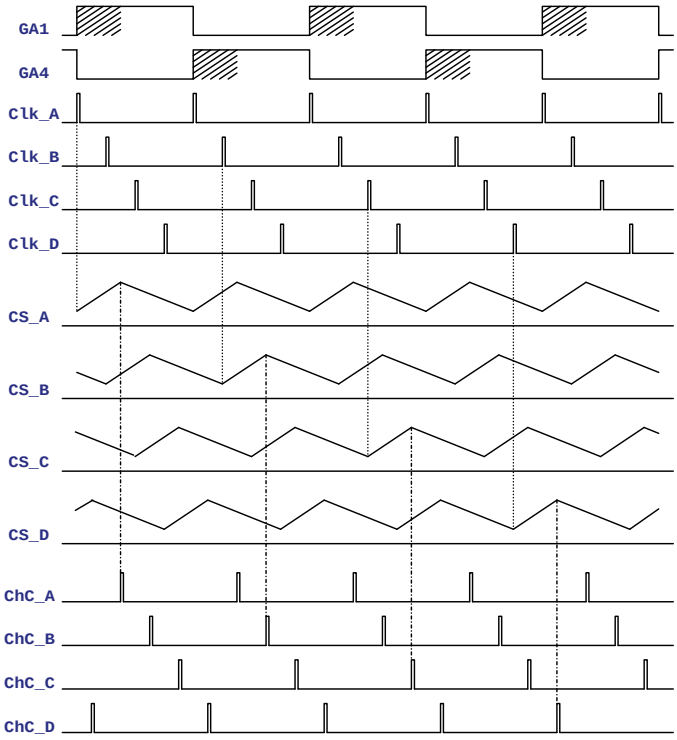

Fig. 6. Four-phase full bridge DC-DC converter with current mode Phase Shifted PWM timing diagrams

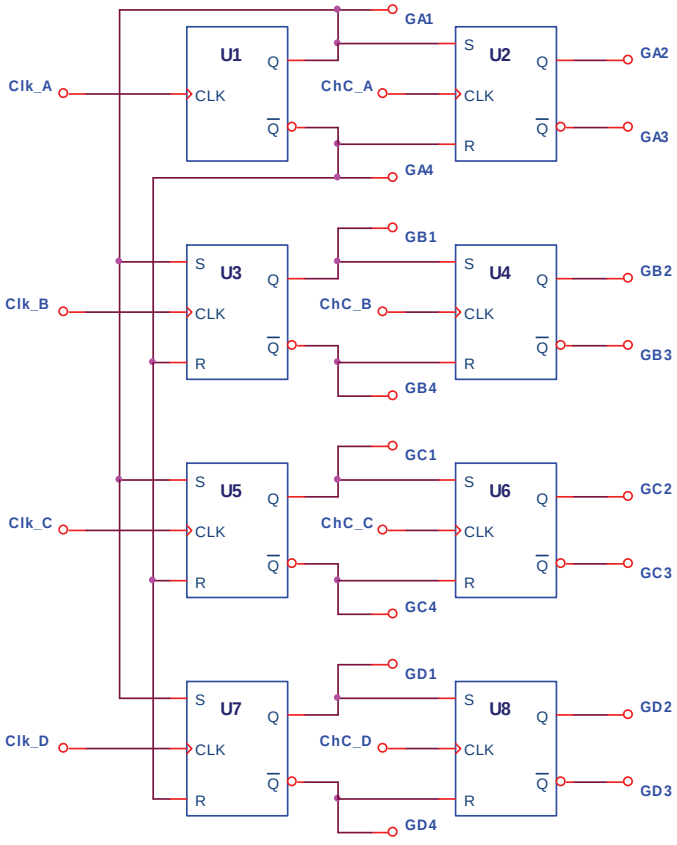

Fig. 7. Multi-phase Full bridge converter gate drive topology

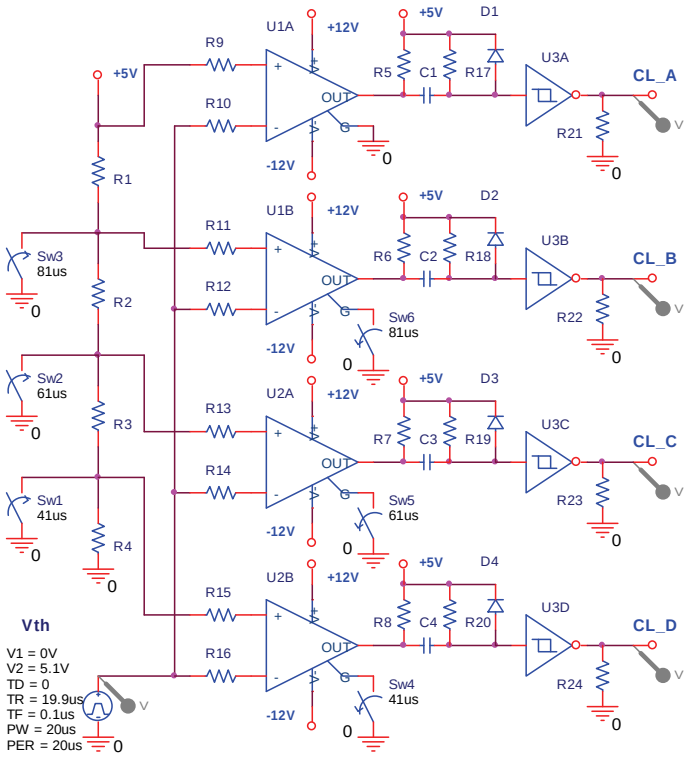

Fig. 8. Programmable clock

Clocks Clk_B, Clk_C and Clk_D set the beginning of each phase shifting which indicates when the output current begins rising after a fall in the corresponding DC-DC converter (B, C, and D). At the corresponding output current peaks, ChC_A, ChC_B, ChC_C and ChC_D are generated. These signals are clocking R-S flip flops U2, U4, U6, and U8 which are synchronized by GA1, GA4; GB1, GB4; GC1, GC4; GD1, GD4.

The clock generating Clk_A, Clk_B, Clk_C and Clk_D timing sequence is illustrated in Fig. 8. Vth pulse source parameters are selected in such a manner that it generates a linear tooth-saw voltage. Phase sifting is set by a precision voltage divider R1, R2 R3, R4. Designed in this way, the topology features equal phase shifting in two, three and four phase systems. This is achieved by sequential commutation of switch pairs Sw1-Sw4; Sw2-Sw5; Sw3-Sw6.

Timing diagrams in Fig. 9 illustrate the programmable clock operation. Simulation is done in *OrCAD PSpice* [7]. Four pulses are generated for the first period in accordance with Sw1-Sw4; Sw2-Sw5; Sw3-Sw6 commutation. Follow three, two and one.

Figure 10 shows the output currents for each DC-DC converter and their summing across the load resistor. As seen on the timing diagrams, the most advantages with the multiphase DC-DC converters are:

- average output current is four times the average current through one phase;
- output current ripple is four times less than of a single phase;
- output current ripple frequency is eight times higher than the transistors switching frequency.

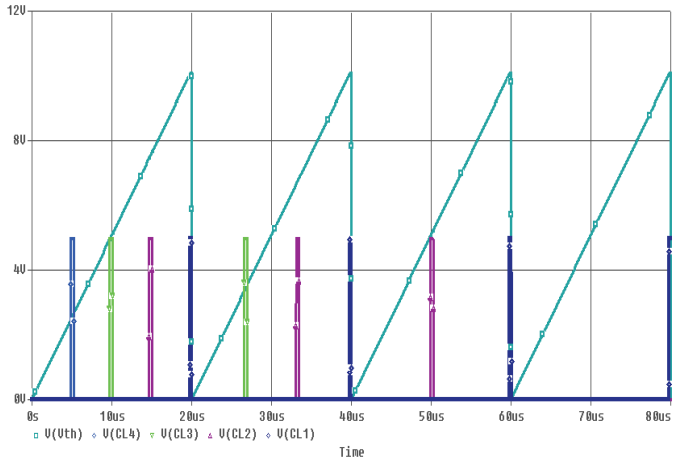

Fig. 9 Programmable clock output timing

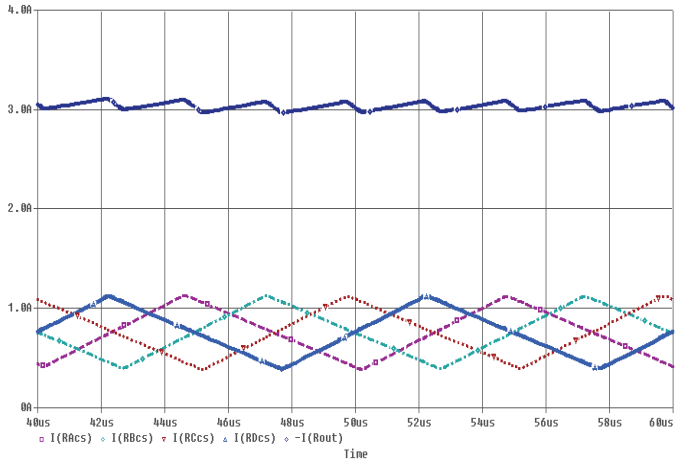

Fig. 10. Four-phase full bridge DC-DC converter simulation results

All these benefits put fewer requirements on the output filters (chokes and capacitors). This leads to more compact and less heavy power supplies, while maintaining the output current ripple to minimum level.

The selected method of charge current mode control features excellent transient respond characteristics at various loads. It takes only few cycles to fully equalize the currents in each phase at no load to full load switch.

IV. Conclusion

A control system has been synthesized in the present paper for the four phase current mode controlled full bridge transistor DC-DC converter. A variant of the clock generator is proposed with the possibility to control one, two, three, or four converters, using programmable logical inputs. The work of the converter is simulated using the *OrCAD PSpice* program.

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