

# CDMA Coded Wrapper-Based SoC Interconnect

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**Abstract** – An efficient technique for realization of on- and off-chip system bus based on wrapper technology and CDMA techniques is proposed in this paper. It is intended to achieve an efficient data transfer among IP cores in System-on-Chip, SoC, and among chips on circuit boards. The main benefits of using this technique relate to decreasing the number of wires on system bus which varies from 25% up to 81%, while the main disadvantage deals with increasing the latency of Read and Write processor cycles. The system throughput depends on bus width, and its min value is 179 Mbps and max 2.783 Gbps. The proposed solution is implemented on FPGA circuit from Xilinx Spartan 3e series.

**Keywords** – System-on-Chip, CDMA technique, Wrapper.

## I. INTRODUCTION

Current VLSI design trends are shifting toward the System-on-Chip (SoC), or a single die incorporating several homogeneous or heterogeneous Intellectual Property (IP) cores. The communication sub-system used to connect IP blocks becomes one of the major bottlenecks for future SOC and has a significant, even a dominating, effect on the performance of a device, and therefore represents a key component to be investigated during architecture definition and tuning [1].

The communication architecture for SOC should be able to transport the heterogeneous traffic efficiently while still maintaining the required performance. In general, communication architectures can be categorized into three main classes: point-to-point interconnect, bus, and network-on-chip [2]. There is no standard solution as to establishing a fast, flexible, efficient and easy-to-design communication network to connect a large number of IP cores that have heterogeneous requirements. Current techniques to reuse the scarce interconnection resources at the physical level can be categorized into several schemes, time-division, code-division, frequency-division, and their combinations. In a time-division scheme, the interconnect resources are shared in the time domain. Arbitration and control of the interconnects are also made based on timing information of the communication modules. In contrast to the time-division schemes, code division schemes expend the resources in the code-space domain, while control of the channel access is also being made on code-space domain. Most of interconnect networks in modern SOC rely on busses, which apply time-division multiple access (TDMA) to reuse expensive on-chip wires, e.g. the AMBA bus, Core Connect etc. Code-division

multiple access (CDMA) has recently been proposed as a new interconnect mechanism for next generation systems [3] - [5].

In this paper, we focus on code-division scheme and we introduce a CDMA coded wrapper based system bus as an interconnect within SoC. We also give the structure of a wrapper logic and discuss the benefits and drawbacks of the proposed solution. In general, by using this technique the number of wire on system bus is decreased in average for 50%, while the main disadvantage deals with increasing the latency of Read and Write processor cycles.

## II. TAXONOMY OF ON-CHIP COMMUNICATION

According to the used taxonomy on-chip communication architectures, see Fig. 1, can be divided into the following three main classes [2]:

a) Point-to-point interconnect - pairs of processing units communicate directly over dedicated physically wired connections. Because of its simplicity, this architecture has been widely adopted in many applications. Custom interconnect, sometimes referred as ad-hoc interconnect, is simply connecting processing elements by wires when there is a necessity. On the other hand, uniform interconnect often has well defined interconnect topology, which can be precisely specified by equations or graphs [6].

b) Bus architectures - long wires are grouped together to form a single physical communication channel, which is shared among different logical channels. An arbitration mechanism is used to control sharing of the bus. A hierarchical shared bus defines a segmented bus architecture. Bus segments are connected via a bridge, which may buffer data. An alternative approach is to use a split-bus. This refers to a set of custom-design segmented buses. Bus segments can be interconnected in an ad-hoc manner, or based on a systematic approach [7].

c) Network-on-Chip (NoC) - is an architecture inspired by data communication networks, such as LANs and WANs, with inter-processor communication supported by a packet switched network. The basic concept of NoC is to communicate across the chip in the same way that messages are transmitted over the Internet today. Communication is achieved by sending message packets between blocks using an on-chip packet-switched network [8].

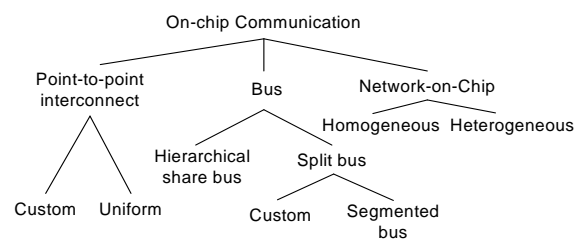


Fig. 1. Taxonomy of on-chip communication architectures

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The most widely adopted interconnect architecture for the SoC design is bus-based due to its low cost. This architecture usually employs hierarchical buses, and tends to distinguish between high-performance system buses and low complexity and low-speed peripheral buses.

On-chip buses can be classified into:

a) standard buses - specify protocols over wiring connections between IP cores. IP cores are designed to comply with one of these protocols and can be reused in another SOC using the same bus. However, they cannot be connected to a different bus without changing their bus interface logic [9].

b) wrapper-based buses - a promising technology for reusing IP cores because it separates the communication logic from the cores thereby avoiding the connectivity problems related to physical bus protocols. The wrapper-based approach uses the IP core interface protocol, which is independent of the physical bus protocol, and uses hardware wrappers to handle the core-to-core communication. Hence, IP cores complying with the interface protocol can be integrated into SoCs with different physical buses as backbones. However, attaching simple wrapper hardware increases the access latencies, so the wrapper must be optimized and be given more hardware logic to optimize its performance [9], [10].

During the last decade there has been some pronounced interest in using high-bandwidth communications protocols to meet the interconnect needs of IP cores within the SoC. One such promising technique is CDMA. CDMA is a spread spectrum technique which encodes information prior to transmission onto a communications medium, permitting simultaneous use of the medium by separate information streams. The basic idea of this technique is that interconnect wiring can be drastically reduced by using CDMA encoding and an appropriate interconnection strategy. CDMA technology relies on the principle of codeword orthogonality, such that when multiple codewords are summed, they do not interfere completely with each other at every point in time and can be separated without loss of information. [5].

According to the previous mentioned, in order to develop a solution for wide range of embedded applications that require low cost, IP core reusability, efficient core interfacing, and moderate communication performance, we propose a CDMA coded wrapper-based SoC interconnect as an efficient proposal which can be used on a complex chip.

### III. MULTIPROCESSOR SYSTEM BASED ON CDMA TECHNIQUE

The global structure of a multiprocessor system on which we will implement a CDMA technique is sketched in Fig. 2. It is bus based system with multiple masters, i.e. participants that originate a transaction and source or sink data. Inherent in the definition of a bus is its exclusive nature. Only one master can use the bus at a time; all other potential masters must wait. Bus arbitration (i.e., the sharing mechanisms) thus becomes a significant part of any bus specification. The master competes for access to the bus, initiates a transaction, waits for the slave to respond, and then relinquishes the bus. The master may

then initiate a second transaction or – through arbitration – lose control of the bus to another master [11].

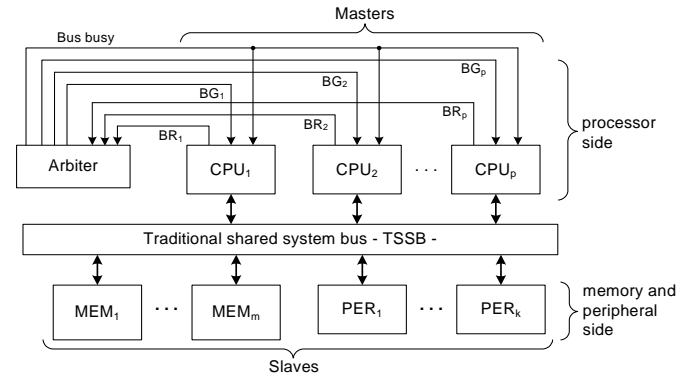


Fig. 2. A traditional bus topology

Arbitration protocols are needed to prevent conflicts when several processors share a common resource. Five arbitration protocols, commonly used in digital systems, are listed according to the method used to assign priorities to the processors: 1) equal-priority protocol, 2) unequal-priority protocol, 3) rotating-priority protocol (round robin), 4) random-delay protocol, 5) queueing protocol (FIFO). Different computer bus architectures and protocols used to resolve the bus contention problem were discussed in several good reviews [12], [13]. Realization of the arbiter logic is not in focus of interest in this paper.

When we implement a CDMA technique on multiprocessor system presented in Fig. 2, on obtain a scheme given in Fig. 3. By comparing structures sketched in Fig. 2 and Fig. 3, we catch sight of the following differences:

a) The traditional shared system bus, TSSB, from Fig. 2 is substituted with a CDMA shared system bus, CSSB.

b) In Fig. 3, at processor side, a master bus wrapper, BW\_CPU, drives the CSSB. The master bus wrapper logic converts traditional bus signals into CDMA coded bus signals.

c) CSSB is composed of three buses: data CDMA coded bus,  $DATA_{CDMA}$ , address CDMA coded bus,  $ADR_{CDMA}$ , and Control bus. The Control bus is identical for both systems (given in Fig. 2 and Fig. 3).

d) The bus arbiter, BA, given in Fig. 3 is realized using the following two building blocks: arbiter select logic, ASL, and arbiter control logic, ACL. The ACL's output defines which CPU's bus will drive the BW\_CPU.

e) Each memory or peripheral block is connected to CSSB via a corresponding slave bus wrapper logic,  $BW\_MEM_i$ ,  $i=1, \dots, m$ , or  $BW\_PER_j$ ,  $j=1, \dots, k$ , respectively. The slave bus wrapper logic converts CDMA coded bus signals into traditional bus signals.

### IV. WRAPPER STRUCTURE

The structure of the bus wrapper is given in Fig. 4. At first, we will classify the interface signals into six parts:

1. Main communication protocol signals: these signals indicate when the address or data is ready, or they can tell the other side to transfer data, such as STATUS, RDY and VAL.

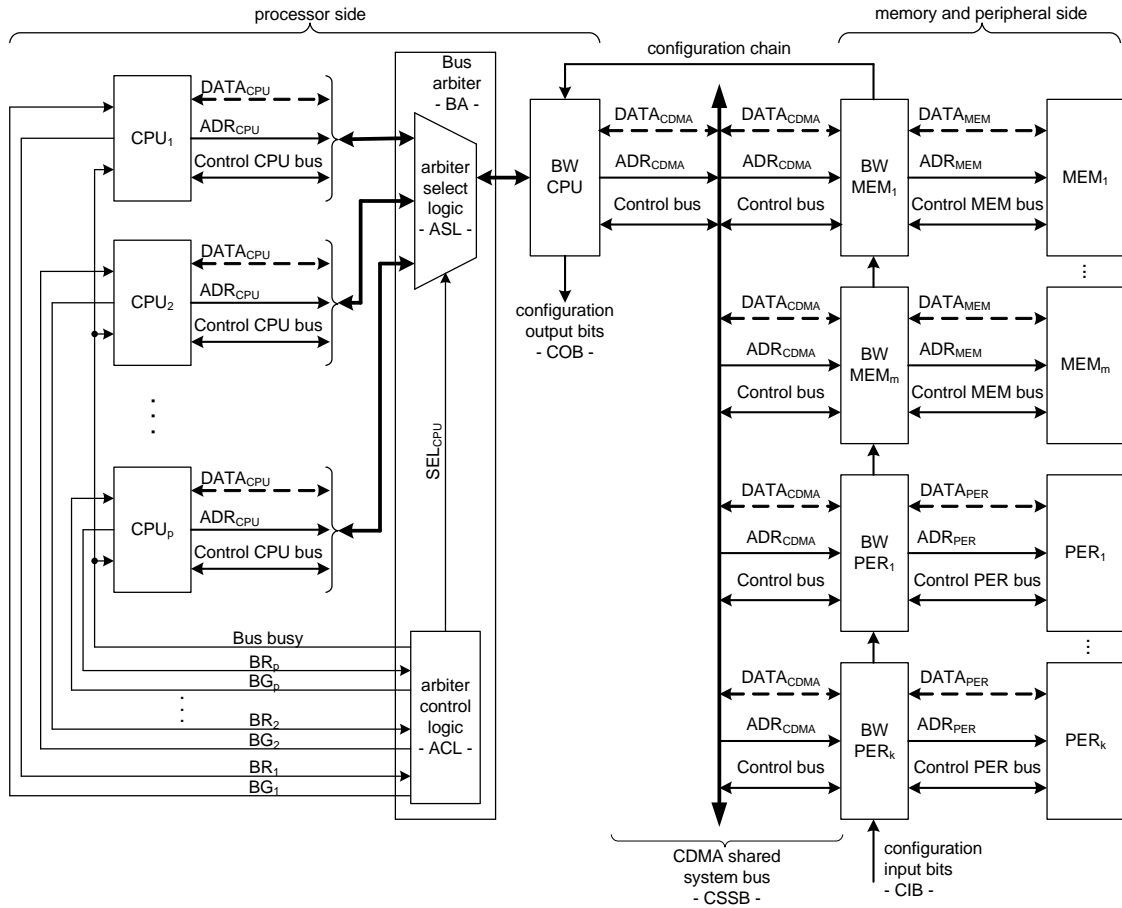


Fig. 3. Multiprocessor system organized round system bus which uses wrappers as interface logic and CDMA transmission technique

2. Command signals: they contain read/write, memory/input-output, interrupt request and interrupt acknowledge command signals, and can tell the other side what activity to perform now. RD, WR, M/IO, INTR and INTA belong to these signals.

3. Data transfer signals: they are main data bus signals signed as DATA.

4. Address decoder signals: they point to the current address and are signed as ADR.

5. Configuration signals: they present input and output configuration bits, CIB and COB.

6. Clock signal: this input clock signal, CLK, is used for generation of internal clock signals.

After classifying the interface signals, we can design six modules of the bus wrapper (see Fig. 4):

a1) Bus Wrapper Control Unit, BWCU: manages operation of bus wrapper and is implemented as a FSM. The state of a BWCU is determined by input/output signals.

a2) Command decoder, CD: translates the control bus signals between traditional and CDMA bus.

a3) CDMA Data Encoder/Decoder, DED: it is bidirectional converter. It operates in semiduplex mode using time division multiplex. In a direction CPU→CDMA bus it converts the CPU output data into CDMA coded data, in opposite it converts the CDMA coded data into CPU input data.

a4) CDMA Address Encoder, AE: converts binary coded address into CDMA coded address.

a5) Configuration Register, CR: accepts and holds configuration bits.

a6) Clock Generator, CG: is implemented as a PLL system. It generates internal clock signals, synchronously with the global system clock, CLK, used for driving the BW\_CPU's building blocks.

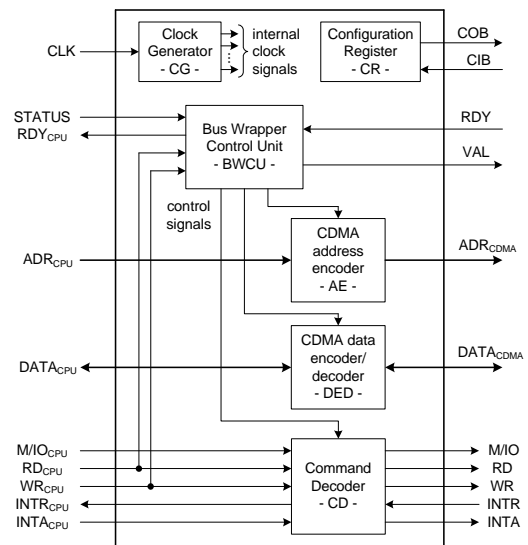


Fig. 4. Wrapper structure

TABLE I  
DATA TRANSACTION SPECIFICATION

BW	8		16			32				64			
SCW	4	8	4	8	16	4	8	16	32	4	8	16	32
CBW	6	4	12	8	5	24	16	10	6	48	32	20	12
GC_Tx	1079	1557	2155	3111	4114	4307	6219	8225	18479	8611	12435	16447	36955
GC_Rx	747	674	1491	1345	985	2979	2687	1927	1441	5955	5371	3851	2851
D_Tx	3.607	3.673	3.516	3.401	4.005	3.679	3.515	3.678	3.933	3.660	3.726	3.690	4.101
D_Rx	4.845	5.160	5.195	5.606	5.576	5.923	5.508	6.034	5.593	5.749	5.409	6.928	7.017
STH	413	194	770	357	179	1351	726	331	179	2783	1479	577	285
DTL	4	8	4	8	16	4	8	16	32	4	8	16	32
BR	25	50	25	50	68.75	25	50	68.75	81.25	25	50	68.75	81.25

Notice: BW - bus width in bits; SCW - spreading code width in bits; CBW - CDMA coded bus width in bits; GC\_Tx - gate count in Tx; GC\_Rx - gate count in Rx; D\_Tx - delay of the Tx in ns; D\_Rx - delay of the Rx in ns; STH - system throughput in Mbps; DTL - data transfer latency in cycles of internal clock; BR - bus reduction in %; Target device: xc3s1600e-5fg484 from Spartan 3e series

## V. RESULTS

Results concerning simultaneous data transfers over wrapper-based interconnect which uses CDMA technique are presented in Table I. As can be seen from Table I, the proposed method can be implemented on address and data buses of different size, such as 8-, 16-, 32-, 64-bits, etc. At behavioral level, master and slave wrappers are described using VHDL code. The wrapper logic is implemented on FPGA circuit xc3s1600e-5fg484 from Xilinx Spartan 3e series.

By analyzing the results we can conclude the following:

- For all system bus width (8, 16, 32, 64) the system throughput, STH, is higher for SCW = 4, and is within the limit from 413 Mbps for BW = 8 up to 2783 Mbps for BW = 64. The STH decreases as SCW increases
- Data transfer latency is proportional to the spreading code size, and varies from 4 cycles of internal wrapper clock for SCW = 4 up to 64 cycles for SCW = 64.
- Data processing of the receiver, D\_Rx, is always higher in respect to data processing at the transmitter side, D\_Tx.
- In general, for all bus width the bus reduction, BR, increases as the spreading code size increases, and is within the limits from 25% up to 81.25%.

## VI. CONCLUSION

An efficient system for simultaneous data transfers over CDMA coded wrapper-based system bus is described in this paper. The structure of the wrapper, at behavioral level, is described using VHDL code. The proposal can be implemented for 8-, 16-, 32-, 64-bit address and data buses, as constituents of the system bus. Using CDMA coding the size of the address/data bus, in terms of number of wires, is reduced according to the following formula

$$CBW = \frac{BW}{SCW} \lceil \log_2 SCW + 1 \rceil$$

In general, bus reduction is within the limits from 25% up to 81.25%, the system throughput is within the limit from 413

Mbps for BW = 8 up to 2783 Mbps for BW = 64, for SCW = 4.

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