Concept of signal processing in ultra-high capacity (1Gbit/s) millimeter wave IP digital radio

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Abstract – **In this paper we describe concept of base band and intermediate signal processing for ultra high (around 1Gbit/s) milimeter wave links. The dominant propagation effect in this frequencies is rain attenuation. Thanks to IP packet transmission adaptive capacity could be easily implemented, which gives tradeoff between capacity and receiver threshold. In this paper we focused on adaptive DBPSK and Pi/4-DQPSK modulation. We proposed the realization that avoids costly DSP components for extremely high bitrates, and focus on analogue realization, which is nowadays much cheaper for this application. System block diagrams and results of experimental design idea verification are given.**

I. INTRODUCTION

Ultra high speed millimeter wave radio links are most appropriate for urban solution, business and ISP IP networks, because of their quick installation and reconfiguration, smaller interference and much higher capacity than in lower frequency bands. The price of such wireless link is usually much more cost effective than leasing or deploying fiber optics link.

In millimeter wave link there are several bands allocated for point to point link purpose:

1. Band 58-63GHz, which is in many country license free, with only limitation of max 55dBm EIRP, minimal antenna gain of 30dBi, and maximum output power of 10dBm [1]. The main drawback of this band is peak of oxygen attenuation (about 15dB/km) which restricts hop length to up to 2km. [4][5]
2. Band 64-66GHz, known as high density network [2], where channel bandwidth is limited to multiples of 30MHz up to 240MHz.
3. Band 71-76 paired with 81-86GHz, which is the most suitable band for point to point link application, since channel spacing is multiple of 250MHz up to 2GHz [3]. In this band oxygen attenuation is not much severe (less than 1dB/km) and hop lengths up to 10km could be achieved.

The most significant propagation effect in these bands is rain attenuation, which dominantly determines individual link availability [5]. Thanks to packet organization of IP traffic usage of adaptive modulation, capacity and/or FEC could be very efficient method for increasing of link availability at expense of link capacity in small amounts of time when rain event occurs. We must note that only drastically reduction of receiver threshold (about 10dB, or more) would have significant effect in these frequencies due to rain intensity distribution and rain attenuation [4][5].

Having these regulations and propagation effects in mind the first and the third band are of great interest since simple modulation schemes could be used. For practical realization of modem it is very important that in these cases components primary designed for fiber-optics and/or SATA communication in PC computer [6], together with lower cost FPGA [7] and MMIC [8] could be used. Since sample rates are very high (even up to 2Gs/s), costly digital signal processing DSP (analogue/digital-ADC and digital/analogue-DAC converters and FPGA multiplier resources) should be avoided due to extremely high price. Instead analogue components, together with differential logic (typically PECL or LVDS) logic devices should be used.

Therefore, we focused on DBPSK and Pi/4 DQPSK with noncoherent demodulation due to modem simplicity, and relatively good BER performance [9]. Low spectrum efficiency of these modulations is not of importance for this application.

II SYSTEM BLOCK DIAGRAM

A. Entire system

One of the most important assumptions is that system should implement adaptive capacity, modulation and/or coding schemes, that yields to different capacity at radio level. Therefore Ethernet interface should perform bridging function. From the bridge point of view entire radio acts as contra directional transmission system that gives to the bridge gaped clock to which it responds with parallel date. Considering novel bridge (like Maxim-IC DS33X162) [6] chips we assumed 8 bit parallel bit stream. After this follows the framer together with Reed Solomon coder which are easy to implement even in lower end FPGA [7].

The second stage is base band signal processor at transmitter side, which is the most critical part for maintain low cost of the entire system. We intend to use external parallel to serial converter with multiplication factor from 8 to 16 (like Maxim MAX9205 and MAX9207) [6], which would give final Gbit/s level data stream from parallel symbol level data obtained from low cost FPGA, like Xilinx Spartan III [7]. Some details about parallel signal processing could be found in [10].

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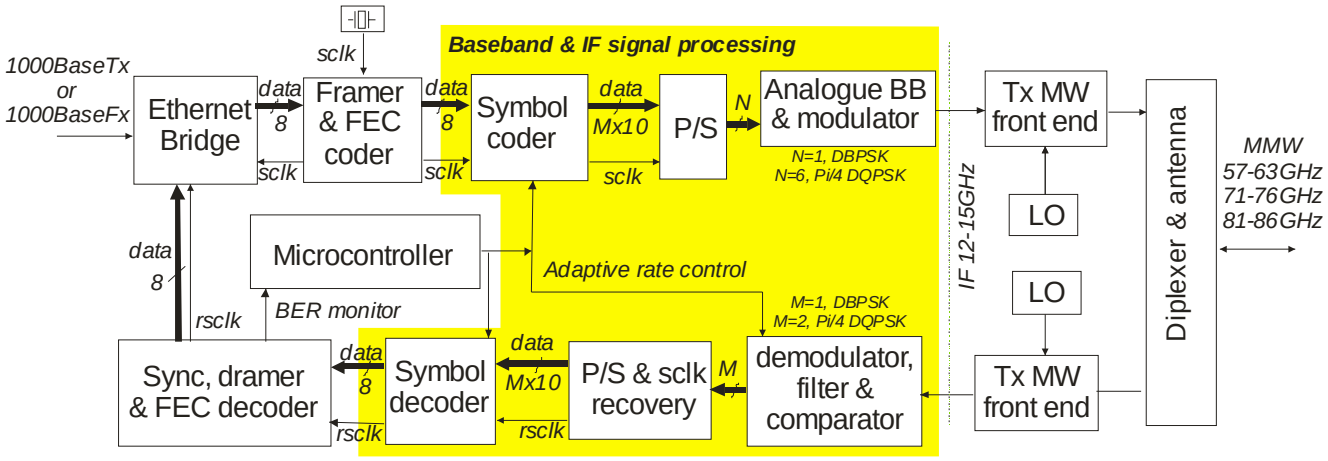

Fig 1. System block diagram

High bandwidth analogue operational amplifiers are used for interfacing between LVDS logic and microwave mixers, and may be got from several manufacturers [6][11].

In order to maintain moderate ratio between modulation bandwidth and central frequency, modulation is performed at 12-15GHz intermediate frequency. At these frequencies we can find high quality MMIC mixer, IQ modulator and demodulator devices [8], or they may be custom designed.

Than follows the mm wave part of the system that up converts the intermediate frequency signal to desired mm-wave frequency from 60 to 90 GHz. In the receiver direction after the antenna follows classical receiver front-end consisting of LNA, down converting mixer, filter and IF frequency AGC block, which are not subject of this paper.

The receiver IF is in the same band as the transmitter. Due to extreme high bandwidth of the signal we assume non-coherent demodulation by differential receivers. After the demodulation follows the serial/parallel converters with clock recovery circuits that converts incoming data into parallel data stream. Than we perform symbol decoding and give receiver 8-bit parallel data stream.

The final stage of the receiver is frame synchronizer with FEC decoder. This block also performs pseudo BER monitoring and alarming. The very important part of the system is microcontroller subsystem that monitors system performance and decides about modulation/capacity changes. This system uses several bits of the frame for internal single hop communication, while for TNM purposes SNMP could be implemented.

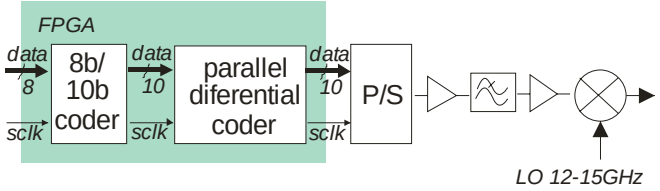

Fig. 2. DBPSK modulator with serializers

B. DBPSK modem with adaptive rate

The easiest to implement modulation scheme is DBPSK. On the transmitter side (Fig. 2.) the incoming data stream is coded by 8B/10B code in order to remove DC and low frequency components. Than follow parallel realization differential coder and serializer with x10 multiplication factor with differential output. Signal from digital differential output is than converted to analogue level and filtered by high bandwidth operational amplifier, buffered and fed into microwave mixers IF port, that acts as a modulator.

Modulator operation at lower bit rate is done at FPGA level since it requires only bit repetition. Additional filtering is unnecessary since, the system works in this condition very small amount of time during the rain falls, which is less than 0.05% of time on well planned hop.

The receiver (Fig. 3.) is construct as differential receiver. After amplification signal is unequally splited into LO side (high power, attenuation about 1dB) and RF side (low power, attenuation about 10dB). Than it is fed into two delay lines each tailored to Tb of specific bit rate: Tsh – symbol duration for high bit rate (about 1Gbit/s, therefore Tsh=1nS) and Tsl – symbol duration for lower bit rate (about 100Mbit/s, and therefore Tsl=10ns). Delay line of Tsh could be realized by meander strip-line technology, while Tsl could be realized by coaxial cable.

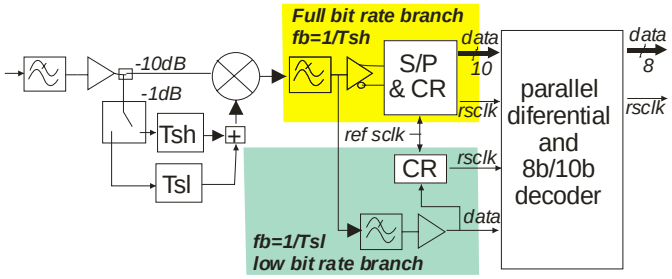

Fig 3. DBPSK demodulator for adaptive bit rate with deserializers and clock recovery

After the mixer follows the buffer and a filter section. The first filters section corresponds to Niquist filtering at the highest bit rate, and it is followed by comparator circuit and deserializer with clock recovery circuitry. For clock recovery circuitry it is necessary to obtain reference clock from local crystal oscillator. Then follows parallel symbol decoder and 8b/10b decoder.

For lower bit rate operation there are additional filter, comparator and clock recovery circuitry, that avoids deserializer and are fed directly to FPGA.

C. Pi/4 DQPSK modem

To achieve better spectrum efficiency we decide to use Pi/4 DQPSK modulation since it could be also differentially demodulated. Similarly to DBPSK adaptive bit rate is also performed by different delay lines.

Conventional Pi/4-DQPSK modulator is described in [10] (Fig. 4.). The main part of modulator is IQ modulator which modulation base band inputs are:

$$u_k = (u_{k-1}I_k - v_{k-1}Q_k)/\sqrt{2},$$
$$v_k = (u_{k-1}Q_k + v_{k-1}Q_k)/\sqrt{2} \quad (1)$$
$$I_k, Q_k \in \{-1,1\}, u_k, v_k \in \{-\sqrt{2}, -1, 0, 1, \sqrt{2}\}$$

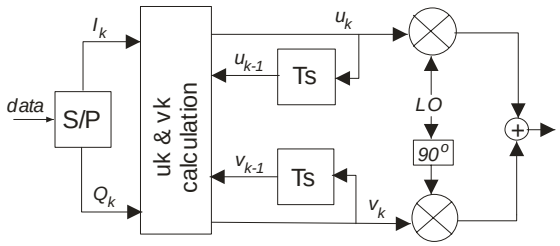

Fig. 4. conventional Pi/4-DQPSK modulator

In conventional realization may be easily obtained by simple DSP and ADC. On Gbit/s such realization would be extremely expensive and therefore we decide to implement it by analogue arithmetic cells made of operational amplifiers. Each level of u_k and v_k could be represented by three bits which in differential logic are represented by +1 and -1, or simple "+" and "-". In that way:

$$u_k = A1 \cdot U_{A1} + A2 \cdot U_{A2} + A3 \cdot U_{A3},$$
$$v_k = A1 \cdot V_{A1} + A2 \cdot V_{A2} + A3 \cdot V_{A3}, \quad (3)$$
$$A1 = 1/\sqrt{2}, A2 = 1/2, A3 = (\sqrt{2}-1)/2$$

The values of U and V for each constellation symbol are given in Table 1.

TABLE 1. SERIALISER DIFFERENTIAL OUTPUT POLARITY FOR SYMBOL GENERATION

cons sym.	u_k	v_k	U_{A1}	U_{A2}	U_{A3}	V_{A1}	V_{A2}	V_{A3}
0	1	1	+	+	-	+	+	-
1	0	$\sqrt{2}$	+	-	-	+	+	+
2	-1	1	-	-	+	+	+	-
3	$-\sqrt{2}$	0	-	-	-	+	-	-
4	-1	-1	-	-	+	-	-	+
5	0	$-\sqrt{2}$	+	-	-	-	-	-
6	1	-1	+	+	-	-	-	+
7	$\sqrt{2}$	0	+	+	+	+	-	-

*Zero can be coded as {+,-,-} or {-,+,+}

The complete Pi/4-DQPSK modulator consists of FPGA signal processor that besides 8B/10B coding and splitting signal into I and Q branch also calculates three bit representation of u_k and v_k symbols. Calculating of uk and vk according to equations (1) could be done by simple, and speed efficient look-up table with 8 inputs and 6 outputs. Since serializers are 10 bit wide, there is necessity for simultaneous computing 10 successive u_k and v_k, which is still does not take much of FPGA resources.

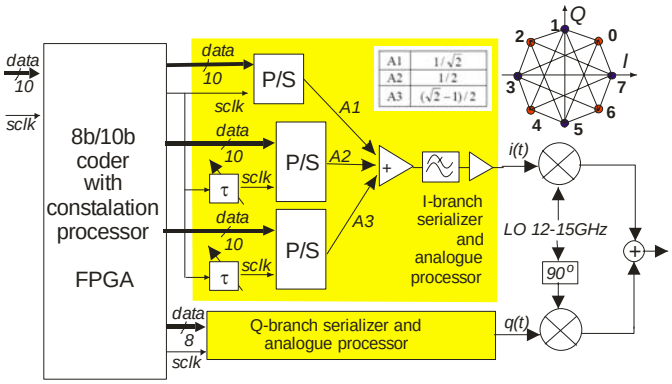

Fig. 5. Ultra high bit-rate Pi/4-DQPSK modem

In this design very critical is phase adjustment of clock multipliers in serializer circuitry. Therefore additional delay tuning circuits should be implemented.

Unlike the complexity of the modulator, the demodulator (Fig. 6.) is much simpler and does not differs much from classical concept given in [9]. Similarly to DPSK case, I and Q outputs of IQ demodulator are filtered, compared with zero and fed into deserializer circuitry with clock recovery. The phase adjustment of two independent deserializer is now much simpler, since it is done at symbol level. It could be completely implemented in FPGA by using delay locked loop –DLL circuitry [7].

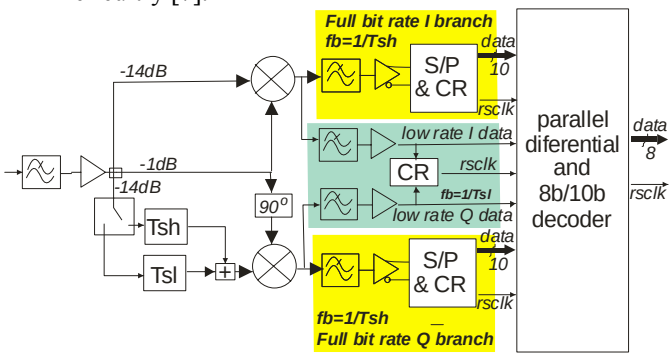

Fig. 6. Differential Pi/4 demodulator

Also, similarly to DBPSK case, operation at lower bit rates at the transmitter side is implemented as symbol repetition, while at the receive side it is done as different delay line at IF frequency and parallel, low bit rate branch at base band level.

If we carefully look the hardware structure we can notice that DBPSK case is actually included Pi/4-DQPSK case. In that way, realization of Pi/4-DQPSK give us not only adaptive rate possibility, but also an adaptive modulation.

III EXPERIMENTAL DESIGN IDEA VERIFICATION

In order to verify our concept we have made an experiment for DBPSK case (Fig 7.). For signal generation we use Anritzu ME520 pattern generator for which clock is provided by Rhode Schwartz SM300 signal generator. The bit rate is varying from 80 to 200Mbit/s. For the DBPSK modulator we used Hittite HMC412 double balanced mixer [], which LO at 12GHz is provided by signal generator HP8673B. The differential DBPSK receiver is constructed by custom design microwave wideband amplifier, that gives total signal power of about +10dBm and than is spited by 3dB

splitter and fit to receiver HMC412 mixer. As a delay line to LO port of the mixer we used various length coaxial cables. The received signal is monitored on 1GHz bandwidth oscilloscope Agilent MSO7104 (Fig 8.).

As expected, on demodulator we got the transition pulse on each data transition in transmitted data stream. The pulse width is correlated by coaxial cable delay line length. Therefore, if the delay line should have delay line should be smaller, *Ts* to prevent inter-symbol interference. To got the highest demodulated signal level the delay should be close to *Ts* as much as possible. According to this, the delay line is not much critical and may result in some small additional implementation loss. The smallest measurable pulse width, with acceptable quality was about 2ns which corresponds to 500MHz bandwidth. This proves proper choice if mixer devices.

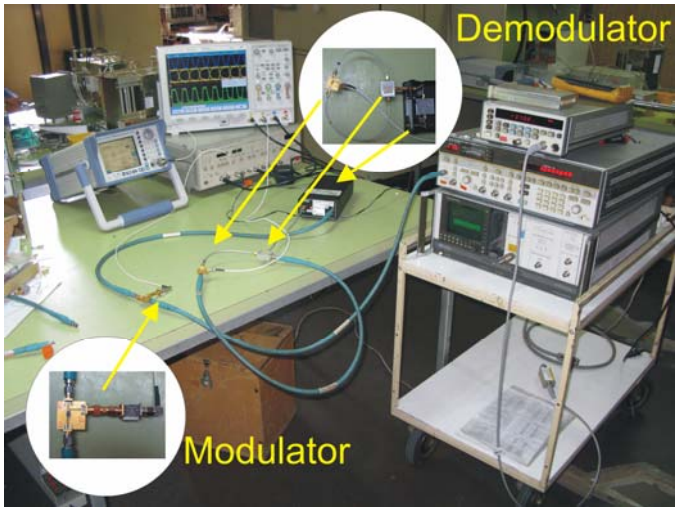

Fig 7. Laboratory test of DBPSK IF subsystem

On given method find the most critical is LO level fed to demodulator mixer. This problem could not be solved by simple adding additional amplifier due to additional delay insertion. Therefore proposed unequal coupler is the proper solution.

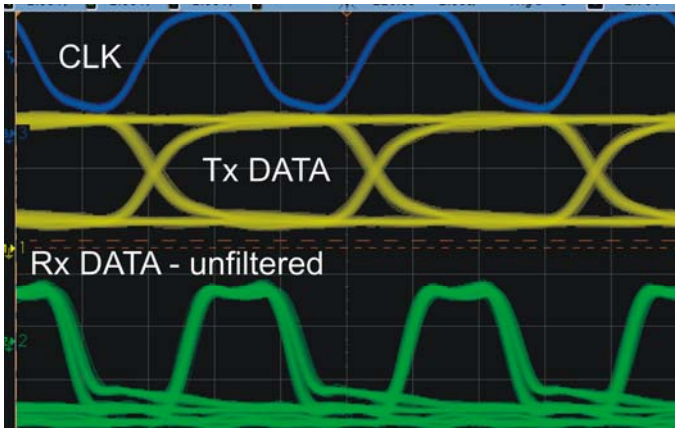

Fig 8. Measured signals

Finally we try external filtering of demodulated signal by transferring measured data from oscilloscope to PC. We simulate in Matlab analogue filter response and obtained acceptable quality eye-pattern, with not significant zero-crossing jitter (Fig. 9.).

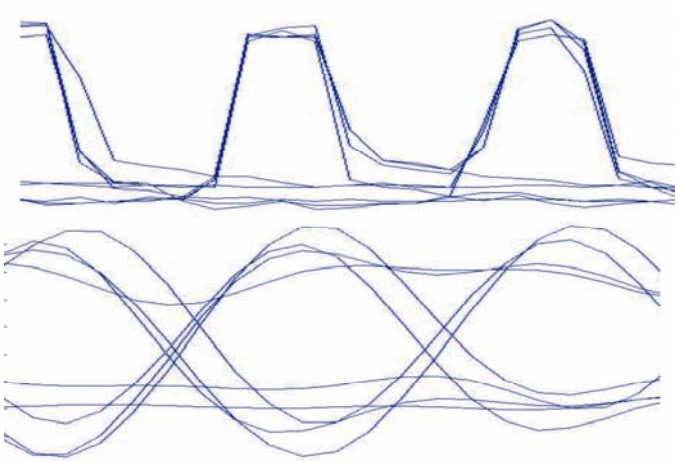

Fig 9. Filtered demodulated signals

IV Conclusion

Experimental design idea verification proved that described concept of IF and baseband signal processing for ultra-high capacity millimeter wave radio is realizable with relatively low cost of entire system. The base band signal processing is not crucial for DBPSK is simple, and not critical. In realization of Pi/4-DQPSK case we expect the most significant problems at transmitter part, especially with timing adjustment of serializers.

V Acknowledgement

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