Software Receiver for Return Path Signals in Cable Television Networks

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Abstract - **In this paper, a new software receiver for return path signals using flexible digital signal processing is presented. The receiver is based on direct digitization of the entire 5-65 MHz upstream spectrum. The digitized signal is passed to a digital front-end that performs baseband conversion, filtering and decimation. After that, the signal is send to the digital signal processor (DSP) where demodulation, derandomization and FEC decoding is performed. The architecture of the receiver shown allows the implementation of DOCSIS and DVB standards on a single hardware platform. In addition, the architecture is optimized for an implementation with an application-specific integrated circuits (ASICs).**

Keywords – **CATV system, Return Path Receiver, DOCSIS, DVB-C, digital front-end, DSP.**

I. INTRODUCTION

Modern CATV system are characterized by the application of digital and optical technologies. Cable distribution networks are bi-directional that makes it possible for additional services (such as Internet access, VoD, VoIP etc.) to be provided to the subscribers. Two-way transmission of high-speed interactive services is performed by Cable Modem Terminal System (CMTS) that is located in the headend or the hub. Cable Modem (CM) or Set-Top-Box (STB) is used in order to receive the data packets addressed to the subscriber and to transmit the data to the CMTS.

Two major systems were developed for the delivery of high-speed interactive services across cable networks: DOCSIS and DVB (DVB-C and DVB-RCC). These two systems are incompatible, although there is an extension to DOCSIS called Euro-DOCSIS, which adapts DOCSIS to the European cable environment, but changes are only at the physical layer. Therefore, there is a need to develop devices that can handle both standards. The application of such programmable and flexible devices in the headend and STBs allows implementation of multiple standards on the same hardware platform.

When building the software headend architecture a solutions similar to the software radio principle have been applied [1-2]. A flexible digital signal processing in downstream direction at the headend is rather straightforward as the hedend acts as transmitter of a certain number of data signals. Therefore the signal processing of the received upstream signal at the headend is most challenging because of the point-to-multipoint architecture of existing CATV networks.

The investigations in this work are focused on the digital front-end of the return path receiver used in the modular software headend architecture. The purpose was to choose the most suitable scheme solution and to specify the requirements to the single functional units.

II. FUNCTIONAL REQUIREMENTS

The required signal processing elements for upstream transmission according to the standards DOCSIS and DVB-RCC are [3-5]:

1) combination of time division multiple access (TDMA/A-TDMA/S-CDMA) and frequency division multiple access (FDMA);

2) upstream frequency range: 5 - 42 MHz (for DOCSIS) and 5 - 65 MHz (for DVB);

3) supported channel widths: 200 kHz, 400 kHz, 800 kHz, 1.6 MHz, 3.2 MHz, 6.4 MHz (for DOCSIS) and 1 MHz, 2 MHz and 4 MHz (for DVB);

4) modulation schemes: QPSK or 16QAM (for DOCSIS) and differential QPSK and 16QAM (for DVB);

5) differential-coded and Gray-coded symbol mapping for DOCSIS;

6) spectral shaping: square-root raised cosine with roll-off factor $\alpha = 0.25$ (for DOCSIS) and $\alpha = 0.3$ (for DVB);

7) randomization: polynomial $1 + x^{14} + x^{15}$ (for DOCSIS) and $1 + x^5 + x^6$ (for DVB) with programmable seed value for DOCSIS;

8) forward error correction (FEC): Reed-Solomon (RS) decoder with variable input length and variable error protection - 18 … 255 bytes data input, 0 … 10 bytes error protection (for DOCSIS) and RS(59,53) decoder (for DVB);

9) upstream burst: programmable preamble with variable length (for DOCSIS), unique word (for DVB).

This multitude of requirements can be performed when most of the headen's functionality is realized in software.

One of the main causes to worsen communications over the reverse path channel of a CATV system is the noise funneling effect. Noise and interference couple into the network due to poor shielding, loose contacts, mismatches, etc. As this happens in all branches of the network, these influences accumulate while they propagate through the tree-and-branch network and sum up in the headend. In result, the carrier-to-noise ratio (CNR) and the carrier-to-intermodulation product ratio (CIR) at the receiver input of the CMTS are reduced to an unacceptable value and communications over the reverse path channel get worse or simply break off. Hence, when designing the reverse path it is of great importance to provide such values of parameters CNR and CIR that ensure given bit

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error ratio (BER). The service delivery over CATV networks requires different BER values varying in the range of 10^{-4} to 10^{-7}.

Because of the frequency dependence of the transfer function and the noise, the return channels have different CNRs. This can be taken into account by applying different constellation sizes on the channels. For low SNR, a robust scheme like QPSK is appropriate while for high SNR higher order QAM schemes are more suited. A necessary condition is that neither the transfer function nor the noise power vary over time. This is fairly true for the broadband and the narrowband noise, but not for the impulse noise. As these influences are not localized in the time or frequency domain, the modulation scheme alone can offer no remedy, but channel coding is the proper antidote. With forward error correction (FEC), the interference due to the impulse noise can be combated.

III. SOFTWARE HEADEND ARCHITECTURES

A new concept that combines the digital signal processing requirements for both standards, the so-called software headend, was introduced in [6-7]. This concept is derived from the software radio principle that was introduced in mobile communications.

There are three main types of software headend that each use different techniques to separate the upstream channels – modular, parallel and FFT-based.

The modular software headend architecture manifolds the signal channel structure M times to support M upstream channel. All digital signal processing units for one upstream channel are grouped into module. This architecture offers most flexibility regarding the number of upstream channels because modules can simply be added or removed. The main disadvantage of this solution is the large amount of identical functional units if many upstream channels have to be supported.

Fig 1 shows the digital signal processing elements required to demodulate and decode one specific channel. Here the input signal is the completely digitized upstream spectrum that includes the return signals of all active software terminals (cable modems and STBs). The sampling rate of the incoming complete signal is selected to be about 150 MHz. In the digital down converter (DDC) a channel selection and down-conversion of the selected RF signal to baseband is performed. Channel selection is done by means of numerically controlled oscillator (NCO), whose frequency and phase are adjusted from signal formed in the carrier recovery functional unit. The resulting baseband in-phase (I) and quadrature (Q) streams are filtered by digital low-pass filters (DLPF), to form the required baseband digital signals. These filters have to provide all possible roll-off factors and bandwidths. In addition to filtering, the DLPFs also reduce the sampling rate to values, required by the Nyquist condition. The decimation factor D depends on the bandwidth of the selected signal.

The signal detector tests the baseband digital signal for a specific pattern than occurs when the preamble is received. For DOCSIS, the preamble is chosen in such a way that the transmitted symbol sequence is composed of P symbols alternating in the first and third quadrant of the complex plane. For DVB, the fixed pattern and the fixed length of the unique word can be used only. When the preamble passes through the detector, a peak with linear increase and decrease can be observed. The position of the pick indicates the beginning of an upstream burst and is used for timing recovery. The timing recovery functional unit passes data to the resampling block that regains the exact sampling point of time. After resampling, the blocks for symbol decision, demaping and differential decoding follow. Finally, the functional units for derandomization and a FEC decoding supply the output bitstream of the selected channel.

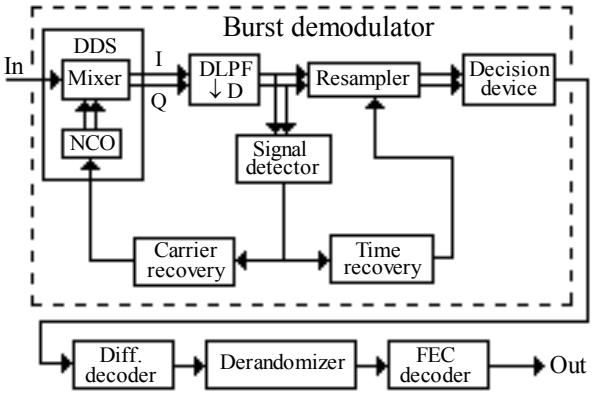

Fig. 1. Single module of the modular software headend

The functional units that are used in the parallel software headend perform digital signal processing of all upstream channels. Each unit has got M parallel inputs that are switched to the selected functionality (each upstream channel requires its own set of parameters). As it is shown in Fig. 2, the complete digitized upstream spectrum passes first through M-channel filterbank with decimation. This block has to be flexible, because the matched filters support the different bandwidth and the central frequencies have to be adjustable to currently used carrier frequencies. In the burst demodulator the following operations are performed: downconversion of the selected RF signal to baseband, signal detection and resampling.

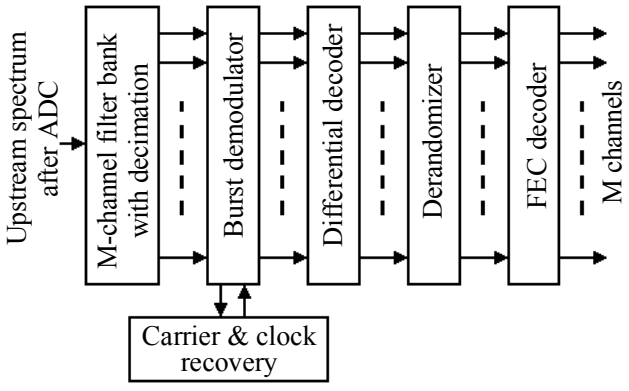

Fig. 2. Parallel software headend

It is evident, that in contrast to the modular software headend the filtering and decimation in this architecture are pulled out of the burst demodulator. This results in a modified

burst demodulator with less complexity that is completely clocked with the decimated sampling frequency. The main advantage of the parallel software headend is that only one implementation of each functional unit is required, resulting in less hardware amount but significant faster circuits.

The FFT-based software heandend makes use of one or more fast Fourier transforms to separate the upstream channel.

IV. Block diagram of the return path receiver

It is well known that the heterodyne receiver can easily adapt itself to many different standards requirements achieving a very good sensitivity and selectivity. However the need of the large number of external components, i.e. the image rejection filter, and the complexity of the structure causes problems if a high level of integration is necessary and flexibility features have to be implemented.

These disadvantages of the heterodyne receiver can be avoided through using architectures that allow many of the conventional receiver functions, such as channel selection, demodulation and decoding to be implemented (performed) by digital signal processing. Therefore it is necessary to convert the complete upstream signal to digital by the analog-to-digital converter (ADC). As the bandwidth of the received signal is 65 MHz, this would require an ADC with a sample rate of a least 130 MHz. It is well known, that for conversion speeds of 1 MHz to 100 MHz, the pipelined ADC finds its best position. The resolution N of an ideal ADC can be calculated from the following equation:

$$CNR_p[\text{dB}] = 6.02N + 1.76 \text{ dB}, \quad (1)$$

where SNR_p is the peak value of this parameter.

A general block diagram of the return path receiver is shown in Fig. 3. The complete upstream spectrum in the range of 5 to 65 MHz is selected by a bandpass filter (BPF) and after amplification is digitized through a wideband ADC. In this receiver, the ADC is operated at a 153.6 MHz sampling rate with resolution of 10 bit/sample. A variable gain amplifier (VGA) is used to adjust the received signals to the dynamic range of the ADC. After A/D conversion, the complete signal is sent to the fully digital front-end.

The first function of the digital front-end is to convert the spectrum of a desired signal to baseband. Channel selection is done by means of numerically controlled oscillator (NCO), whose frequency is controlled by the DSP. The baseband signal is then passed to a cascaded integrator comb (CIC) filter, where digital filtering and decimation is performed. For the different bandwidths the sampling rate can be decreased by different decimation factors D_k ($k = 1, \ldots, 8$). The final stage of the digital front-end is the matched filter, which performs square-root raised-cosine (SRRC) Nyquist filtering. This filter has to provide all possible roll-off factors and bandwidths required for the standards DOCSIS and DVB-RCC. The required bandwidth, roll-off factor and decimation factor are adjusted programmable by means of digital signal processor (DSP).

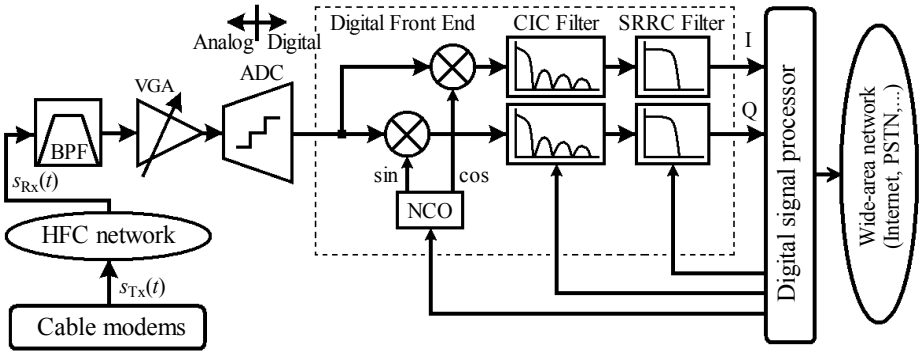

Fig. 3. Block diagram of the return path receiver

The DSP unit includes digital demodulator, derandomizer and FEC decoder. The basic function of the digital demodulator is to perform carrier and timing recovery, channel equalization, ingress noise cancellation, and make symbol decision and demapping. More information about this functional unit and applied techniques for signal processing is given in [7-8].

V. Detailed description of the digital frond-end

In Fig. 4 a simplified block diagram of the NCO is shown. The NCO contains sine and cosine generators which can be viewed simply as ROM-based Look Up Tables (LUT) that perform the following functions:

$$\begin{aligned} \sin[n] &= \sin[2\pi n/N] \\ \cos[n] &= \cos[2\pi n/N], \end{aligned} \quad (2)$$

where: n is the address input to the LUT, N is the number of samples in the LUT. Incrementing n from 0 to $N-1$ causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The time required to increment n from 0 to $N-1$ is the period of the sine and cosine waveforms produced. The LUT address is incremented once each cycle of the clock by an amount equal to the phase word input. The phase angle is accumulated and stored in the phase

accumulator register. The output of the phase accumulator is used to address the sine and cosine LUT's.

The frequency of the sine and cosine waveforms f_{NCO} is defined as follows [9]:

$$f_{NCO} = f_{clk} * \text{phase}\left[(k-1)\ldots 0\right]/2^k , \quad (3)$$

where: f_{clk} is the frequency of the input clock, phase[(k -1)…0] is k-bit tune data. The frequency tuning resolution is given by:

$$\Delta f_{NCO} = \pm 0.5 f_{clk}/2^k . \quad (4)$$

Two digital multipliers are used to heterodyne, or mix, the input data samples with the NCO quadrature waveforms. The downconversion process has translated the signal of interest (a purely real signal located at 5-65 MHz) down to baseband (a complex signal located at 0 Hz).

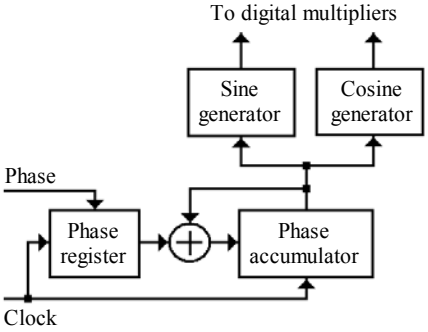

Fig. 4. Simplified block diagram of the quadrature NCO

Here presented digital frond-end contains two filter types. The decimating CIC filter is composed of three sections. The first section consists of digital integrators and operates at the A/D sampling rate. After integrator section follows a rate change, or decimation, section. The decimated samples feed into the comb filter section, which operates at the sample rate divided by D_k. As the CIC filter does not require any multipliers and is therefore useful at high sampling rates, its filtering characteristics are severely limited. That is way its essential function is to decrease the sampling rate and to keep passband aliasing within specified limits.

The system function for the CIC filter, referenced to the high speed sampling rate, is found by combining the transfer function of the integrator and comb sections, i.e. [9]

$$H(z) = \frac{\left(1-z^{-D}\right)^P}{\left(1-z^{-1}\right)^P} = \left[\sum_{m=0}^{D-1} z^{-m}\right]^P . \quad (5)$$

where: P is the number of stages, D is the decimation factor. The frequency response for the CIC filter is given by

$$H(f) = \left(\frac{\sin(\pi f)}{\sin(\pi f/D)}\right)^{2P} . \quad (6)$$

where f is the sampling frequency f_s relative to the decimated rate, f_s/D.

The square-root raised cosine (SRRC) filter is used primarily for isolating the signal of interest by attenuating out-of-band signal energy. Its frequency-domain description is piecewise function, given by

$$H(f) = \begin{cases} T^{1/2}, & f \le (1+\beta)/2T \\ \left(\frac{T}{2}\right)^{1/2}\left\{1+\cos\left[\frac{\pi T}{\beta}\left(f-\frac{1-\beta}{2T}\right)\right]\right\}^{1/2}, & \frac{1-\beta}{2T} < f < \frac{1+\beta}{2T} \\ 0, & \text{otherwise} \end{cases} \quad (7)$$

where $0 \le \beta \le 1$ is the roll-off factor and $T = 1/f_s$. The bandwidth of a SRRC filter can be calculated as

$$BW = \frac{1}{2T}(1+\beta) . \quad (8)$$

VI. Conclusion

The return path receiver presented in this paper provides very good sensitivity and selectivity and satisfies the high quality requirements that exist in professional equipment for CATV headends. The receiver is based on direct digitization of the upstream channel spectrum and makes use of highly sophisticated algorithms for timing and carrier recovery, channel equalization, and ingress noise cancellation. Using this concept, a 4-input/16-output receiver can be integrated in a single chip, which also includes 4 downstream modulators and critical medium access control (MAC) functions. A software-controlled switch integrated in the chip allows sending to each one of the 16 digital front-ends and demodulators the desired input port signal, and then each digital front-end selects the desired upstream channel. In addition to the increased CMTS density, such receiver architecture also offers cable operators full flexibility in network planning and handling the evolution of their cable plants without human intervention at hubs and cable head-ends.

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