A Synchronized Two-Phase Generator for High-Precision Impedance Bridge

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Abstract - **An electronic circuit generating two orthogonal square-waves is described. The generator is based on simple JK flip-flop circuit; theirs clock is driven by a phase-locked loop circuit, which ensures frequency and phase synchronization of its output with an external sync signal. Due to application of the circuit in high-precision impedance bridge the maximum deviation of the phase shift between the square-waves should be smaller than $0{,}05^0$ and the frequency range of the generator is 100 Hz – 100 kHz.**

Keywords – **Two-phase generator, impedance bridge.**

I. INTRODUCTION

There are two types of high-accuracy, automated impedance bridges: transformer bridges [1], [2] and systems employing digital sine-wave technique [3], [4]. The former are used for extremely high accuracy comparisons of like impedances and the latter when also unlike impedances are to be compared. In precision transformer comparator bridges for like impedances comparison which structure is shown in Fig. 1 the unbalance voltage $\underline{\Delta U}$ (underlined to express its complex character) is proportional to the difference of the compared impedances and the measuring current $\underline{I}_x$:

$$\underline{\Delta U} = (\underline{Z}_X - \underline{Z}_N)\frac{\underline{I}_X}{2}, \tag{1}$$

so the impedance difference of the compared standards can be calculated using the formula:

$$\underline{Z}_X - \underline{Z}_N = \frac{2\underline{\Delta U}}{\underline{I}_X}. \tag{2}$$

If a series equivalent circuit of the impedance standard is assumed, the above equation can be express as:

$$(R_X + \mathrm{j}X_X) - (R_N + \mathrm{j}X_N) = 2\,\mathrm{Re}\left\{\frac{\underline{\Delta U}}{\underline{I}_X}\right\} + 2\,\mathrm{j}\,\mathrm{Im}\left\{\frac{\underline{\Delta U}}{\underline{I}_X}\right\} \tag{3}$$

Comparing the left and right sides of real and imaginary parts one can obtain:

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$$R_X - R_N = \frac{2|\underline{\Delta U}|\cos\varphi}{|\underline{I}_X|} \tag{4}$$

$$X_X - X_N = \frac{2|\underline{\Delta U}|\sin\varphi}{|\underline{I}_X|}, \tag{5}$$

where φ is the phase shift between the unbalanced voltage ΔU and the measurement current I_x.

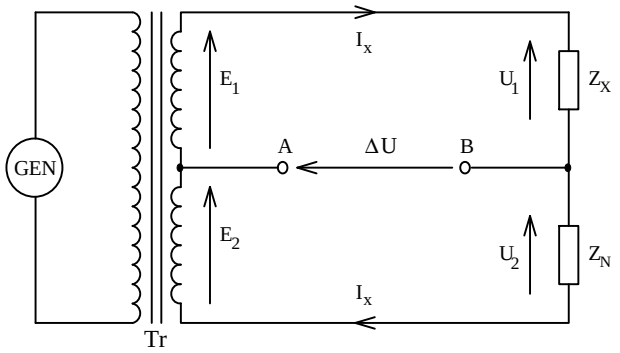

Fig. 1. Circuit diagram of unbalanced bridge for impedance standards comparison

Taking Eqs. (4) and (5) into consideration, it is not difficult to see that to determine differences of resistance and reactance, the unbalance signal $\underline{\Delta U}$ should be decomposed into in-phase with $\underline{I}_x$ and quadrature component [1]. A block diagram of circuit enabling direct measurement of differences of both impedance components (ΔL and ΔR) is shown in Fig. 2.

The unbalance voltage $\underline{\Delta U}$ is provided from the diagonal of the bridge (Fig. 1) to two phase-sensitive detectors [5]. On the outputs of the detectors the voltages proportional to the numerators of the fractions in the (4) and (5) equations appear. The signals are further converted into digital form and transmitted to the microcontroller. The measuring current $\underline{I}_x$ is converted to a voltage signal, which after rectification and AC filtering has the value proportional to the modulus of the measurement current, so - to the denominator of the fractions in the Eqs. (4) and (5). The voltage after conversion is transmitted to the microcontroller which calculates the resistance and reactance differences according to the (4) and (5) formulas.

A significant influence on the accuracy of measured difference of the impedance components has the synchronized two-phase generator, which produces two orthogonal square-waves with 0.5 duty cycle as reference for the phase-sensitive detectors [5]. One of them is in phase with the $\underline{I}_x$, the second is shifted by 90^0 from the former. To achieve high accuracy of the impedance bridge in a wide frequency range the maximum deviation of the phase shift between the square-waves should

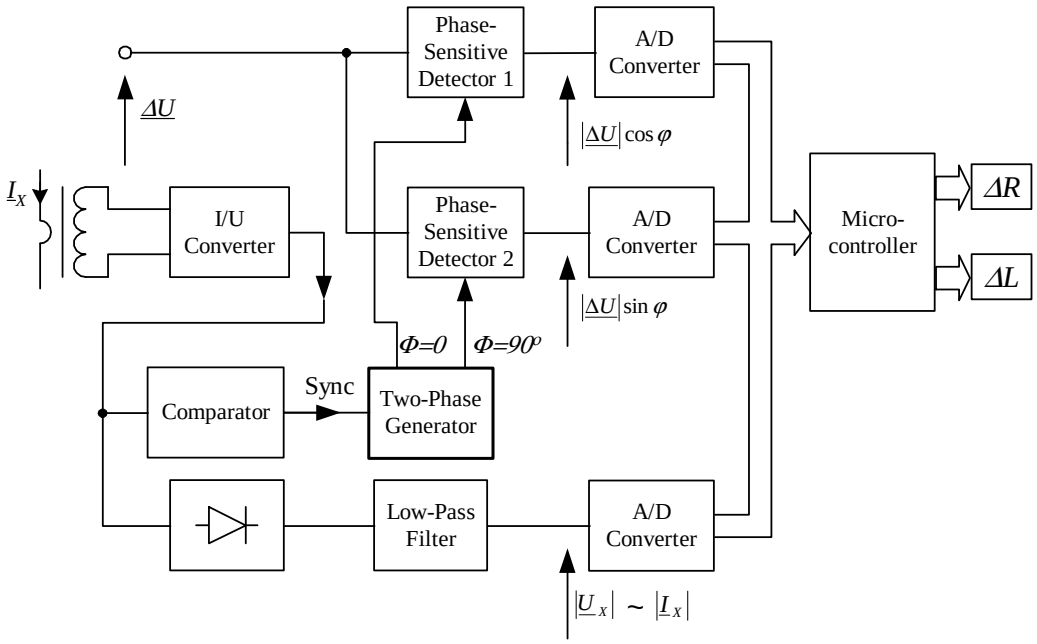

Fig. 2. Block diagram of circuit for ΔL and ΔR measurement

be smaller than 0.05^0 in the whole required frequency range (100 Hz – 100 kHz). Taking the above into consideration we can conclude that the two-phase generator cannot be built using standard phase shifters because they don't guarantee high stability of the phase shift.

II. TWO-PHASE GENERATOR

Two square-wave signals with a 50% duty cycles and different in phase by exactly 90^0 can be generated using a simple digital circuit shown in Fig. 3.

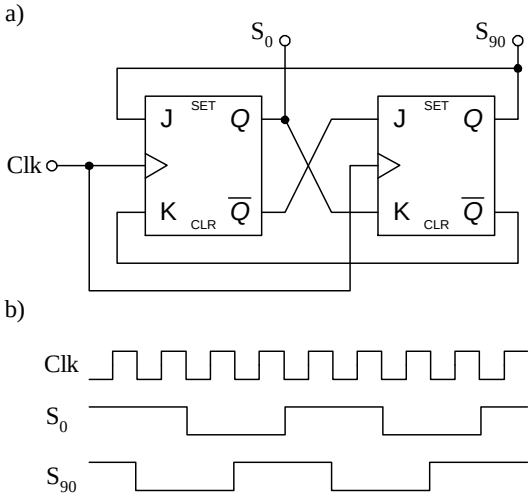

Fig. 3. Two-phase square-wave generator: a) circuit diagram, b) timing diagram

The clock signal Clk is provided in parallel to two JK flip-flops. Using proper loop connection on the S_0 and S_{90} outputs we obtain two square-waves with a phase difference of 90^0 (Fig. 3b). The propagation delay time in digital circuits is dependent on the output load capacitance and for the CMOS circuits can be described by the following formula [6]:

$$t_{PHL} = 22 \text{ ns} + 0.16 \text{ ns/pF}. \quad (6)$$

Ensuring the same load capacitances on the generator outputs one can obtain the same propagation delay times of the signals on the S_0 and S_{90} outputs. Hence, the phase shift between S_0 and S_{90} is equal to exactly 90^0 and the duty cycles of the square-waves are equal to 0.5. Taking Equ. (6) into consideration it is not difficult to see that for the 100 kHz (the worst case in the considered frequency range) the $0{,}05^0$ (~1,4 ns) deviation of the nominal phase shift appears when the difference in the output loads is 9 pF. However, it is not difficult to meet the requirement of adjusting the output load capacitances with a precision of 9 pF.

The main disadvantage of the proposed circuit is that the frequency of the clock signal should be four times higher than frequency of the measuring current $\underline{I}_x$, and additionally is necessary to synchronize the phase of the S_0 signal with the phase of the $\underline{I}_x$.

III. SYNCHRONIZATION OF THE GENERATOR

The PLL circuit was used to ensure the synchronization of the two-phase generator with the measuring current $\underline{I}_x$ (Fig. 4).

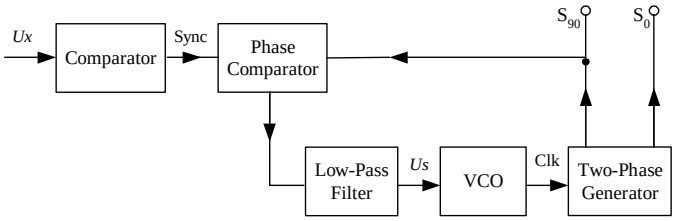

Fig. 4. Block diagram of the two-phase sync generator

The output voltage U_x from the I/U converter (Fig. 2), which is in phase with I_x and whose absolute value is proportional to the absolute value of I_x, is further converted to the square-wave by the comparator and provided to the phase comparator. On the second input of the phase comparator the S_{90} signal from the two-phase generator (Fig. 3) is provided. An Exclusive-OR gate works as the phase comparator [7]. The average output voltage from the phase comparator is the resultant of the difference in phase between the signals U_x and S_{90}. When the phase difference between the synchronizing signal (Sync) and S_{90} signal is equal to 90^0 then the average value of the voltage on the output of the phase comparator is equal to zero. The output voltage from the phase comparator (often named "phase-error signal") is filtered by the low-pass and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The phase locked loop circuit changes the frequency of the controlled oscillator until it is matched to the U_x in both frequency and phase. In the steady-state (the PLL is called "locked") the S_0 square-waves is in phase with the U_x, and the S_{90} signal is shifted by 90^0. Then the VCO frequency is four times higher than the U_x frequency.

When the frequencies of the signals on the inputs of the phase comparator differ, then the phase shift between them, so also average value on the output of the phase comparator, changes with the differential frequency. If the differential frequency is higher than cutoff frequency of the low-pass filter, the VCO input voltage U_S is equal to zero so the oscillator isn't tuned and the PLL cannot reach lock. The PLL works properly when the difference in frequency between the synchronizing signal (Sync) and the output signal from the VCO when $U_s = 0$ (known as the free-running frequency) is smaller than the cutoff frequency of the low-pass filter. The range meets the above requirement is called "capture range". The capture range is defined as the band of frequencies centered around the VCO natural frequency lock with an external input signal from an unlocked condition. The lock range is defined as the band of frequencies centered on the VCO's natural frequency over which a PLL can maintain frequency lock with an external input signal (Fig. 5).

Extending the capture range of the PLL by extending the bandwidth of the low-pass filter is disadvantageous because the phase-error signal is ineffectively filtered and the unwanted variation of the U_s signal occurs that leads to the fluctuation in the VCO output frequency (jitter frequency). The lock range of the PLL is limited only by the VCO range and is usually much wider than the capture range. If an incoming frequency is far moved from that of the VCO, so that their difference exceeds the pass band of the low-pass filter, it will simply be ignored by the PLL. Thus, the PLL is a frequency-selective circuit. The PLL can return into the active state when the incoming frequency goes into the capture range.

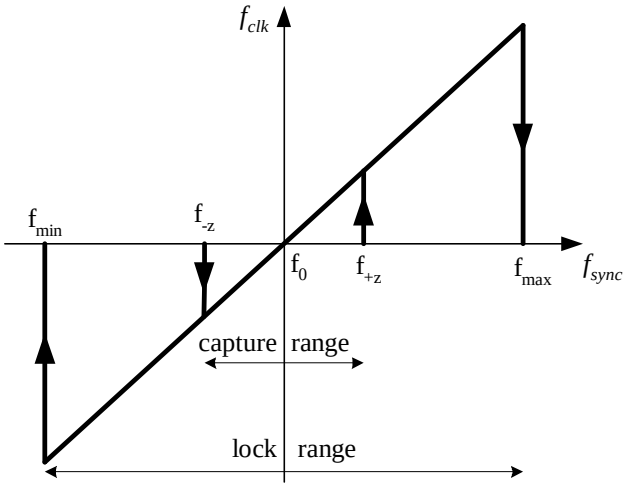

Fig. 5. PLL capture and lock ranges

Taking the above under consideration we can conclude that the cutoff frequency of the low-pass filter is always a result of compromise between the wide capture range of the PLL and the high stability of the VCO. To ensure both: wide capture range and high frequency stability the circuit shown in Fig. 4 was modified by applying the frequency ratio detector FRD based on two cargo pumps (Fig. 6).

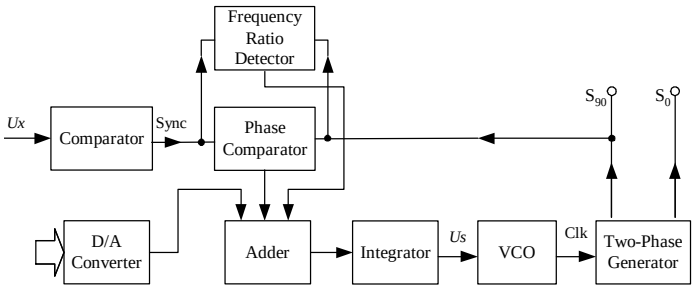

Fig. 6. Block diagram of the two-phase sync generator with the frequency ratio detector

When the frequencies of the U_x and the S_{90} signals are the same, the voltage on the output of the FRD is equal to zero. If the frequencies differ, then the output voltage is positive or negative according as which frequency (U_x or S_{90}) is higher. Furthermore, when the frequencies of the U_x and the S_{90} are significantly different, the error signal on the output of the phase comparator is equal to zero but the non-zero voltage from the output of the FRD is provided through the adder to the integrator circuit that causes increase (or decrease) of the U_s signal. It means that the VCO is tuned and the frequency of the signal S_{90} is going close to the frequency of the

synchronizing signal Sync. In case of small difference in frequencies of the U_x and S_{90}, the voltage on the FRC output decreases and the slow rising (or falling) voltage from the output of the phase comparator sets the phase shift between the U_x and S_{90} to be 90^0. Then the PLL capture range identical to the lock range which means that the PLL can lock on signal within all VCO range.

In a real circuit on the outputs of the phase comparator and the frequency ratio detector a parasitic voltages occur. The result of this is a small (about 0.8^0) stable phase error. The error can be limited to less than 0.05^0 by providing a correction voltage to the adder. For this purpose the generator was furnished with the digital-to-analog converter which enables (together with a microcontroller) auto-calibration of the all measuring circuit. Then, to the inputs of the phase sensitive detectors (Fig. 2) the U_x voltage is provided instead of the unbalance voltage ΔU. The phase error of the two-phase generator is reduced when the voltage on the output of the phase sensitive detector no.2 is equal to zero. If the value is non-zero, then a proper correction value is provided to the DAC.

IV. CONCLUSION

The two-phase generator described in the paper enables one to generate two orthogonal square-waves needed to control the phase sensitive detectors used in the high-precision impedance bridge. The phase error of the generator is less than 0.8^0 and can be reduced to 0.05^0 by using the auto-calibration. The frequency range of the generator is 100 Hz – 100 kHz and is determined by the assumed frequency range of the impedance bridge. The detector circuit presented in the paper was used in high precision impedance comparator. Its usefulness was proved by the calibration of different impedance standards in wide frequency range.

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