Noise Modeling and Simulation for JFETs at Low Frequencies

Pesha D. Petrova[1], Dimitar P. Petrov[2]

Abstract – **In this paper two low-frequency noise models for JFETs are proposed. Noise in the first of them is modelled by internal sources and in the second one, with external Vn - In sources, respectively. The models are analyzed. PSpice/MATLAB simulations are performed and the results are presented.**

Keywords – **JFET T - small – signal equivalent circuit, Input noise, PSpice/MATLAB simulation, Vn-In noise model.**

I. INTRODUCTION

The sensitivity of many today's communication systems is limited by noise. A very important source of noise in these systems is the electronic devices that form the heart of the signal processing and transmission components in them. These are irreducible sources of noise, and it is important to realize and to model their noise characteristics. Therefore, the noise modeling is a fundamental prerequisite for the computer-aided design in the modern communication systems. In order to predict correctly the noise behavior of such systems, accurate noise models for semiconductor devices are required. Without them, the design and optimization of the circuit noise characteristics cannot be successful.

Since the key components in many circuits are the JFETs, extensive work has been carried out in the field of noise modeling and analysis for these devices. The existing JFET physical noise models, such as, Pospieszalski, Gummel – Pun, and Puce models [1], [2] generally show good agreement with measured data, but they are too complex and require too many parameters. For this reason, their using for noise modeling and analysis is not effective. In order to be easily used, as well as, to take into consideration the effects under the influence of the bias condition, temperature, source resistance, and frequency, the models should be simplified.

In many cases for practical applications, noise modeling for JFETs can be split into a high and a low frequency segment. On the base of the small-signal JFET models [1], [2], [3], two low-frequency noise models are presented, and an analytical approach to overcome some of the problems mentioned above is proposed. The input noise as a function of the frequency, of the JFET bias condition and parameters, as well, of the source resistance is obtained. Several PSPICE/MATLAB simulations of the models are completed and the results are presented.

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II. LOW – FREQUENCY JFET NOISE MODELS

In this section, low - frequency noise models for JFETs are proposed. The models are synthesized on the base of the JFET T - small - signal equivalent circuit [4], which is simplified so to be suitable for noise analysis and simulation.

A. Noise Model with Internal Noise Sources

In the first model the noise sources are included in the small signal equivalent circuit as shown in Fig. 1.

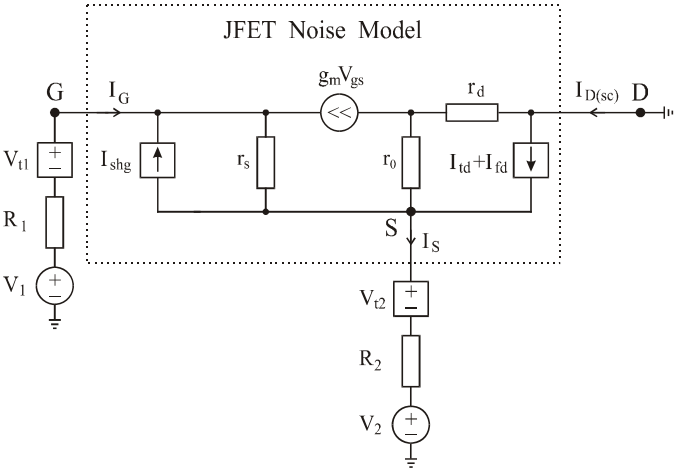

Fig. 1. JFET small-signal low-frequency noise model with Thévenin sources connected to the gate and the source

The source I_{shg} models the shot noise in the gate bias current I_G. The thermal noise and the flicker noise in the drain bias current I_D are modeled by $I_{td} + I_{fd}$. In the band Δf, these have the mean-square values

$$i_{shg}^2 = 2qI_G\Delta f \tag{1}$$

$$i_{td}^2 = 2kT\left(\frac{2g_m}{3}\right)\Delta f \tag{2}$$

$$i_{fd}^2 = \frac{K_f I_D^m}{f}\Delta f \tag{3}$$

where g_m is the small-signal transconductance of the JFET, q is the electron charge, k is the Boltzmann's constant, T is

the temperature in Kelvin, m is usually taken to be unity, and K_f is the flicker noise coefficient.

The external drain and source circuits in Fig. 1 are modeled by Thévenin equivalent circuits. With $V_2 = 0$, is modeled a common-source (CS) stage, and with $V_1 = 0$, is modeled a common-gate (CG) stage. The noise sources V_{t1}, and V_{t2} model the thermal noise in R_1 and R_2, and the mean-square values of V_{t1} and V_{t2} are given by

$$v_{t1}^2 = 4kTR_1\Delta f \tag{4}$$

$$v_{t1}^2 = 4kTR_2\Delta f \ . \tag{5}$$

The short-circuit drain output current can be presented as

$$I_{d(sc)} = G_{mg}V_{tg} - G_{ms}V_{ts} + I_{td} + I_{fd} \tag{6}$$

where

$$G_{mg} = \frac{1}{r_s + R_2 II\, r_o}\frac{r_o}{r_o + R_2} \tag{7}$$

$$G_{ms} = \frac{1}{R_2 + r_s II\, r_o} \tag{8}$$

$$V_{tg} = V_1 + V_{t1} + I_{shg}R_1 \tag{9}$$

$$V_{ts} = V_2 + V_{t2} + \left(I_{td} + I_{fd} - I_{shg}\right)R_2 . \tag{10}$$

The equivalent noise input voltage V_{ni} can be expressed as a voltage in series with V_1 for the CS stage and in series with V_2 for the CG stage, respectively. Substituting Eqs. (7), (8), (9) and (10) into Eq. (6), and applying some mathematical transformations to it, gives the following expression for the equivalent noise voltage in series with V_1

$$V_{ni} = V_{t1} - V_{t2}\left(1+\frac{r_s}{r_o}\right) + I_{shg}\left[R_1 + R_2\left(1+\frac{r_s}{r_o}\right)\right] + \left(I_{td} + I_{fd}\right)r_s . \tag{11}$$

To express V_{ni} as a voltage in series with V_2 Eq. (11) is multiplied by G_{mg} / G_{ms}.

Using $r_s = 1/g_m$, the mean-square value of V_{ni} for the CS stage is found to be

$$v_{ni}^2 = 4kT\left[R_1 + R_2\left(1+\frac{1}{g_m r_o}\right)^2\right]\Delta f + 2qI_G\Delta f\left[R_1 + R_2\left(1+\frac{1}{g_m r_o}\right)\right]^2 + 4kT\left(\frac{2}{3g_m}\right)\Delta f + \frac{K_f I_D \Delta f}{f} . \tag{12}$$

It follows from Eq. (12) that the thermal noise current generated in the channel, when expressed as an equivalent voltage in series with the gate, is the same as the open-circuit thermal noise voltage of a resistor of value $R = 2/3g_m$.

B. Vn – In Noise Model

The second model is obtained by reflecting all internal noise sources to the input. In order for the reflected sources to be independent of the source impedance, two noise sources a required [4] – a series voltage source and a shunt current source. The $V_n - I_n$ noise model of the JFET is shown in Fig. 2. To use this model for analysis, the JFET is considered to be noiseless and it must be replaced by T-equivalent circuit, shown in Fig. 1, without the noise sources.

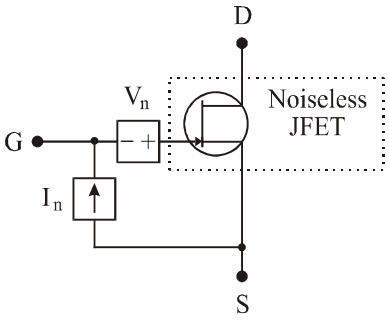

Fig. 2. Vn – In JFET noise model

To solve for the values of V_n and I_n in the model in Fig.2, Eq. (11) is used. Because the equivalent noise input voltage V_{ni} given by this equation is the voltage in series with the gate, R_1 must be considered to be the resistance of the signal source. In the $V_n - I_n$ model, the I_n current noise source connects between the gate and source. For this reason, R_2 must be set to zero in the circuit to solve for I_n. Otherwise, the noise contributed by R_2 would appear in the model and I_n would connect from the gate to the lower node of R_2. With $R_2 = 0$, Eq. (11) becomes

$$V_{ni} = V_{t1} + I_{shg}R_1 + \left(I_{td} + I_{fd}\right)r_s . \tag{13}$$

This equation is in the form $V_{ni} = V_{ts} + V_n + I_n R_s$, where $V_{ts} = V_{t1}$ and $R_s = R_1$. It follows that V_n and I_n are given by

$$V_n = \left(I_{td} + I_{fd}\right)r_s \tag{14}$$

$$I_n = I_{shg} \tag{15}$$

and there mean-square values, respectively

$$v_n^2 = \frac{i_{td}^2 + i_{fd}^2}{g_m^2} = 4kT\left(\frac{2}{3g_m}\right)\Delta f + \frac{K_f I_D \Delta f}{g_m^2 f}$$

$$= \frac{4kT\Delta f}{3\sqrt{\beta I_D}} + \frac{K_f \Delta F}{4\beta f} \quad (16)$$

$$i_n^2 = i_{shg}^2 = 2qI_G \Delta f \quad (17)$$

where $g_m = 2\sqrt{\beta I_D}$ is used, and β is the transconductance coefficient.

The gate bias current I_G is commonly assumed to be zero when the gate-channel junction is reverse biased, but for a high source impedance, the effect of the gate current on the noise might not be negligible.

III. Simulation Results

Based on the two models presented and analyzed above, the noise characteristics for JFET CS stage are simulated using PSpice/MATLAB medium [5]. The simulations are performed with JFET biased at $I_D = 1mA$ and having $\beta = 5.10^{-4} A/V^2$.

Fig. 3 shows the simulated equivalent input noise voltage and the flicker noise over the frequency range from $100\,Hz$ to $100\,kHz$ for two values of the signal source resistance R_s.

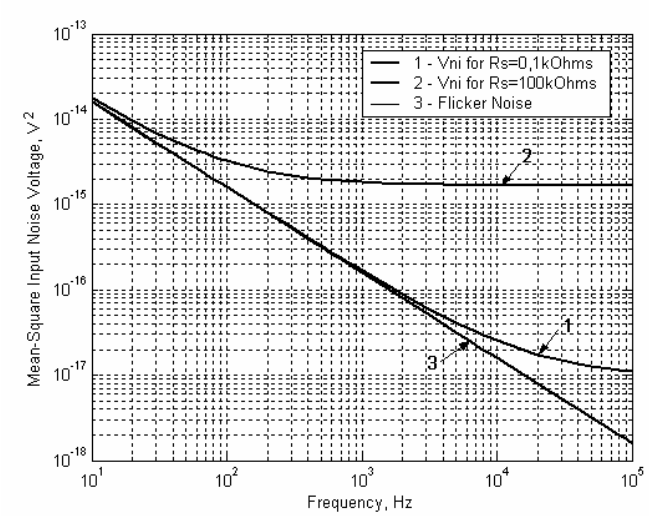

Fig. 3. Equivalent input noise voltage versus frequency.

By comparing a curve 1, which corresponds to $R_s = 0{,}1\,k\Omega$, with a curve 2, corresponding to $R_s = 100\,k\Omega$, respectively, it may be concluded that as the frequency increases, the equivalent input noise voltage decreases more rapidly for small than for large source resistances. For example, for $f = 100\,Hz$, the ratio $\frac{v_{ni}^2(R_s = 100k\Omega)}{v_{ni}^2(R_s = 1k\Omega)}$ is only $2{,}028$, while for $f = 100\,kHz$ the same ratio is $150{,}524$, i.e. the difference between the mean-square noise voltage values for the two cases, due mainly to the effect of the source resistance thermal noise and of the gate shot noise, increases. The contribution of the flicker noise is significant for small R_s. As it is seen in Fig. 3, the curve 3 simulating the flicker noise, completely coincides with a curve 1 up to $f = 300\,Hz$. For frequency in the $300\,Hz$ to $3\,kHz$ range, the flicker noise is slightly lower than the equivalent input noise, and above this frequency range the difference between the two curves increases, that means the effect of the flicker noise on the total noise decreases.

In Fig. 4 the equivalent input noise voltage, as well, two its components, depending on the transistor transconductance are compared. Fig. 4 clearly shows that with the transconductance increase the equivalent input noise components decrease. For example, at $g_m = 5\,mS$ the mean - square value of the total input equivalent noise voltage decreases 8,689 times, of the flicker noise 25 times, and of the channel thermal noise 5 times, as compared with the same values at $g_m = 1\,mS$. The flicker noise dominates for small transconductance values. For g_m in the $2{,}5$ to $3{,}5\,mS$ range, the channel thermal noise is approximately equal to the flicker noise. Above this range, the two noise components differ insignificantly, the flicker noise is slightly lower than the channel thermal noise. At the same time, the source resistance thermal noise and the gate shot noise are independent on the transconductance value and their mean-square values are $1{,}656.10^{-18} V^2$ and $3{,}2.10^{-26} V^2$, respectively, so they can be neglected.

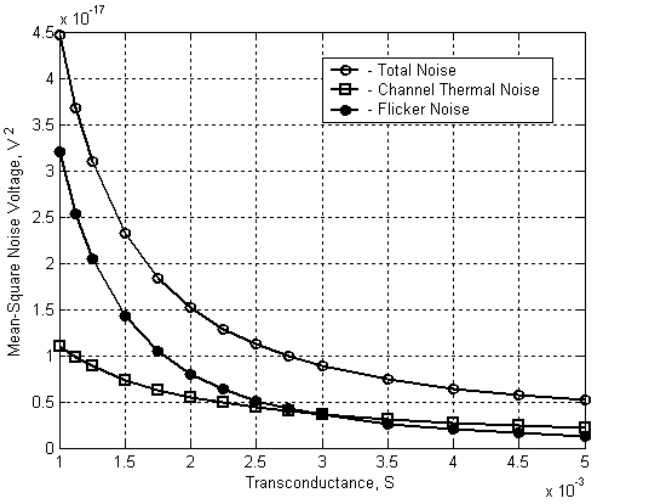

Fig. 4. Influence of the JFET transconductance value on the equivalent input noise voltage components.

Fig. 5 demonstrates how the drain bias current influences on the v_n noise and on its components for working frequency of $20\,kHz$. It is observed from the curves that the flicker noise exceeds the thermal noise, generated in the channel, if the bias current is grater than $1mA$. In Table I the simulated results for different working frequencies are summarized. It is clear from the results that the flicker noise contribution to the v_n noise increases with the drain bias current increase at one and the same frequency. This increase is more significant above the

TABLE I
FLICKER NOISE CONTRIBUTION

f, kHz	v_{nf}^2 / v_n^2, %			
	$I_D = 1mA$	$I_D = 2mA$	$I_D = 3mA$	$I_D = 4mA$
0,1	99,515	99,657	99,720	99,757
0,5	97,618	98,304	98,610	98,796
1,0	95,346	96,665	97,259	97,620
20	50,614	59,172	63,964	67,210
40	33,882	42,017	47,019	50,612
50	29,075	36,697	41,520	45,051

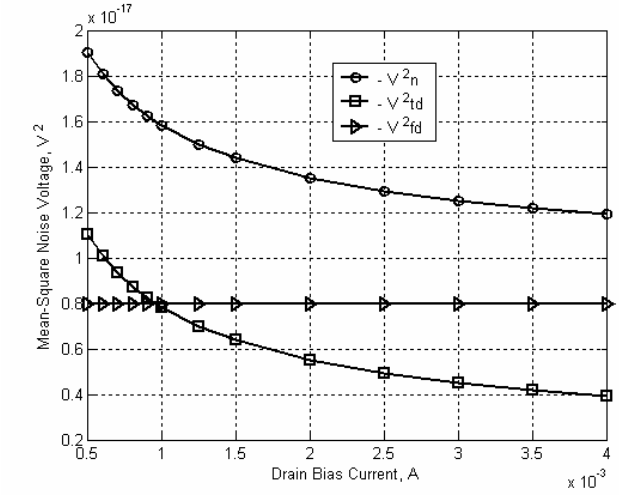

Fig. 5. Influence of the drain bias current on the Vn noise.

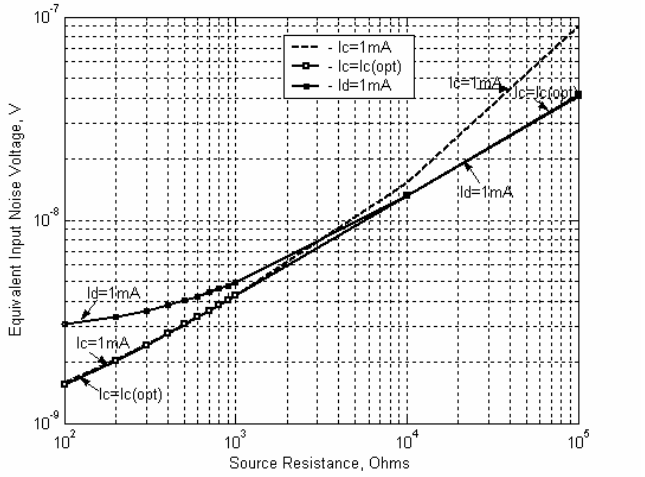

Fig. 6. JFET and BJT equivalent input noise versus source resistance.

frequencies of $20kHz$. On the other hand, the frequency value increase causes significantly decrease of the flicker noise. The simulated results coincide with the theoretical ones, given in [4]. If the gate shot noise can be neglected, the dominant noise above the flicker noise range is the thermal noise generated by the channel. It follows from the simulated results that this noise decreases by $1,505\ dB$ each time the drain bias current is doubled. Thus, there is no optimum bias current which minimizes the thermal noise.

In order to compare the noise performance of the JFET and BJT, the input noise voltage versus R_s is simulated and the results are shown in Fig. 6. For the BJT the noise model given in [6] is used and the noise for a constant and for the optimum bias collector current is simulated. For the JFET the noise simulation for a constant drain bias current is only realized. It is clear that for R_s small, the two BJT cases give the lowest noise. Although the results almost coincide, the noise is slightly lower for the BJT biased at $I_{C(opt)}$. For R_s large, the JFET and the BJT biased at $I_{c(opt)}$ give the lowest noise, but the JFET noise is slightly lower than the BJT noise. For R_s in the 3 to $4k\Omega$ range, the JFET and the BJT biased at $1mA$ give approximately the same noise, while the BJT biased at $I_{C(opt)}$ gives slightly lower noise.

IV. CONCLUSION

An approach for JFET noise modeling and analysis at low frequencies is developed. PSpice/MATLAB simulation results validate the models proposed. The results allow a wide range of designers to analyze and to predict the effect of the JFET bias conditions, of the source resistance and frequency on the input equivalent noise, as well, on the designing systems noise behavior.

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