Digital Frequency Sensitive Phase Detector with Controllable Phase-to-Voltage Response

Aleksandar Yordanov[1], Georgy Mihov[2]

Abstract – **In this paper a digital frequency sensitive Phase Detector (PD) with controlled phase-to-voltage response is presented. The scheme is based on classic type flip-flop phase detectors and enhanced PD working on both fronts of input sequences. The control of phase-to-voltage response characteristic is obtained by additional feedback from output voltage from low-pass filter to reset input of driving flip-flop.**

Keywords – **Digital phase detector, Simulation of phase-to-voltage response**

I. Introduction

In practice several types of digital phase detectors are used. All of them have different features and characteristics and that's why there is no universal phase detector which gives best performance for all kinds of Phase Locked Loops (PLL) circuits. When choosing phase detectors, the following parameters have to be considered: shape, frequency and magnitude of input signals, linearity of phase-to-voltage response, range of operation of phase or frequency difference and etc.

A well known digital Frequency Sensitive Phase Detector is shown in fig. 1 (called in this paper – FSPD type 1). This PD is analyzed in [1], [3], [4] and its main advantages are:

- If input frequency f_1 is different from input frequency f_2 there is DC component in output of PD. The polarity of this component depends on the difference between input frequencies. This feature of phase detector makes it frequency sensitive.

- If $f_1 = f_2$ the scheme works only as phase detector and its phase-to-voltage response is linear in range $(-2\pi \div +2\pi)$.

At present, this PD is most often encountered in practice. One reason is acceleration of the phase lock by combination of the frequency detector properties (for larger detuning) with final phase detection. Another appreciated property is its IC production by many companies, generally under the type number 4046. Further more this phase detector has the maximum possible working range from -2π to $+2\pi$. The phase-to-voltage response of the scheme from Fig.1 is shown in fig. 2. On Fig 3 is the same characteristic but obtained by simulation analysis described in [2].

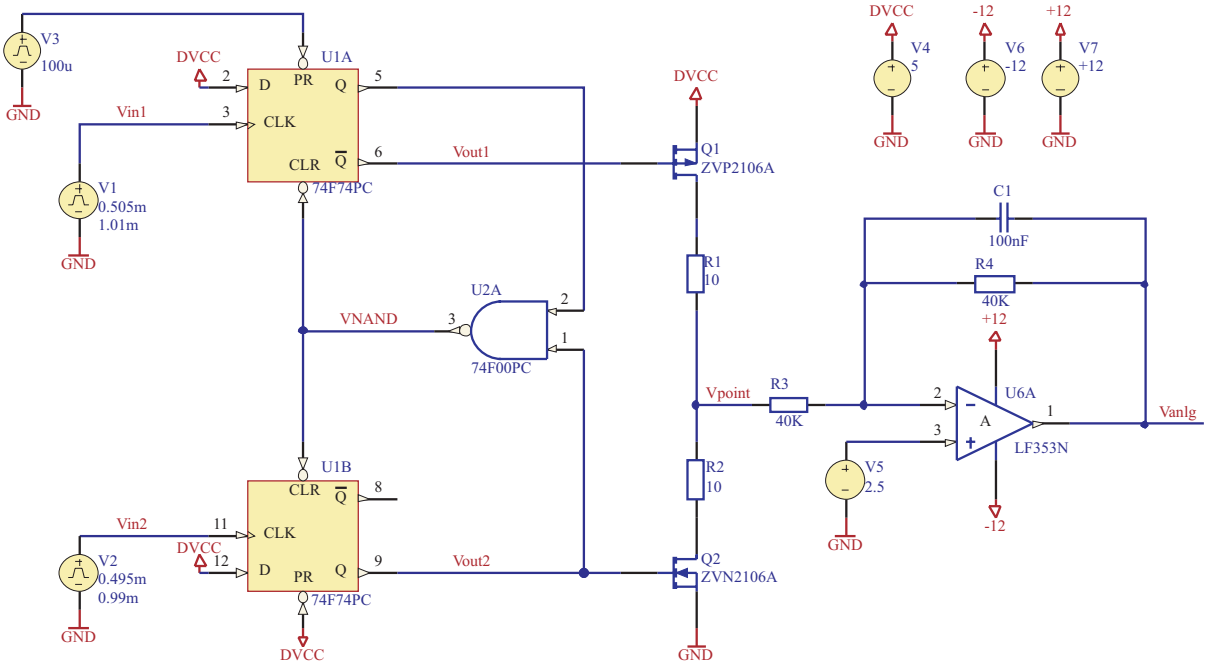

Fig. 1 Scheme of FSDP type 1

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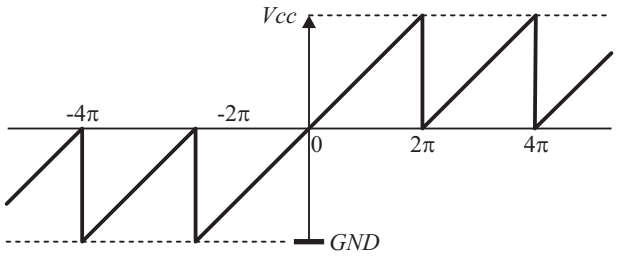

Fig. 2 Phase-to-voltage response of FSDP type 1

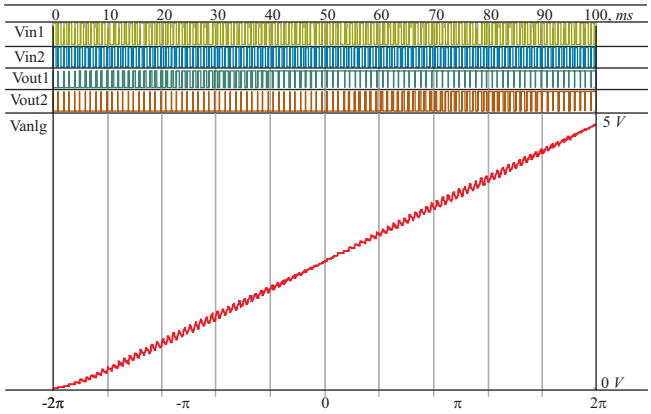

Fig. 3 Phase-to-voltage response of FSDP type 1

Another type of digital Frequency Sensitive Phase Detector is shown in fig 4 (called in this paper – FSPD type 2), it is based on FSPD type 1 and described in [1]. The difference between these two PD's is that the FSPD type 2 works on both fronts of input signals – rising and falling, while FSPD type 1 works only on rising front. The main advantage of this is: doubled frequency in output of phase detector, which means simpler low-pass filter and less pulses in output voltage. A phase-to-voltage response of PD scheme from Fig. 4, is shown in fig. 5 for the general case. On Fig 6 is the same characteristic but obtained by simulation analysis of 0,5 duty cycle of input signals– described in [2].

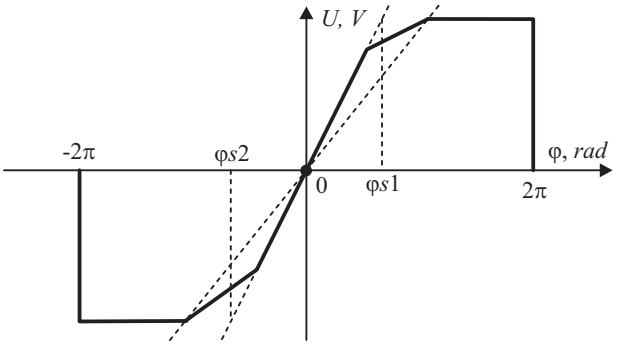

Fig. 5 Phase-to-voltage response of FSDP type 2: theoretical analysis

However this PD have considerable disadvantage which makes its use limited. The working range is only from -π to +π. Furthermore this PD has non-sensitive areas from -2π to -π and from +π to +2π.

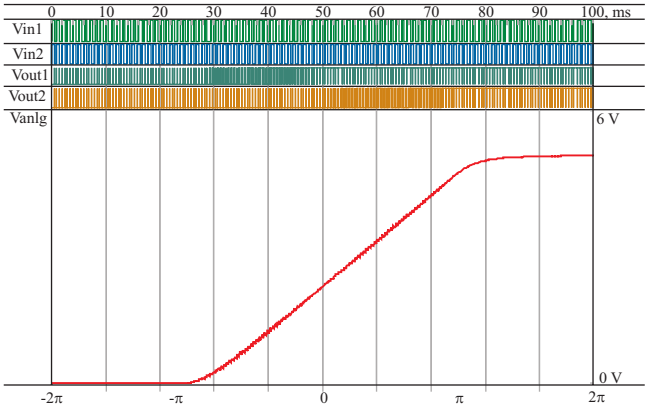

Fig. 6 Phase-to-voltage response of FSDP type 2: simulation analysis

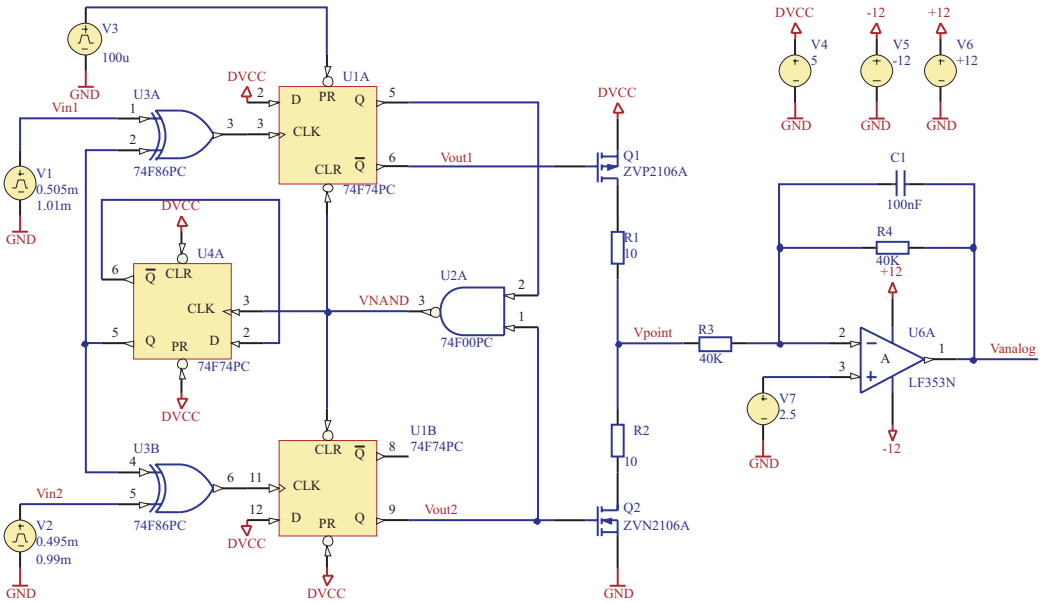

Fig. 4 Scheme of FSDP type 2

II. Digital Frequency Sensitive Phase Detector with Controllable Phase-To-Voltage Response

In present paper a scheme of digital frequency sensitive phase detector is proposed which combines the advantages of both PDs. The scheme of this FSPD is shown in fig 7.

The scheme from Fig. 7 contains the FSPD type 2, but there is included control of Reset input of the 3-th "setting" D flip-flop U4A. So if there is low logical level on this input, there will be low level on the Q output of U4A and XOR logical gates wouldn't change the input signals. So this means that the circuit will work the same way as the one on fig. 1 does. On the other hand if there is high logical level on Reset input of U4A, the PD will work as FSPD type 2. This switching gives the possibility of setting the best type of PD dynamically.

To find the best switching moment, analysis of the specific phase or frequency locked loop solution has to be done. From [1] and [2] can be concluded that in case of high deviations of phase (frequency), the circuit signal needs less amplifying. This is because the scheme feedback has a potential risk of over adjustment and getting out of working range. On the other hand, when the phase locked loop is in locked state the PD should have highest sheer on phase-to-voltage response. By this, the PLL circuit will react more quickly on noise related changes in output phase (frequency) and make easier filtration of PD output voltage.

In fig. 7 is shown the scheme of digital Frequency Sensitive Phase Detector with controllable phase-to-voltage response. The switching point is set by comparators U5A and U5B. In fig. 8 is shown idealized phase-to-voltage response.

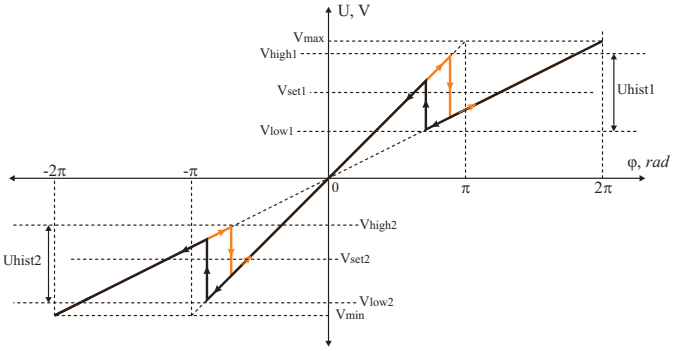

Fig. 8 Phase-to-voltage response of Digital Frequency Sensitive Phase Detector with Controllable Phase-to-Voltage Response

To increase the reliability of the circuit, both comparators should have two levels of switching i.e. the comparators work as Schmitt triggers. The scheme in fig. 7 combines all the requirements mentioned above. Thresholds Vset1 and Vset2 are set by reference voltages V9 and V8. The hysteresis - U_{hist1} and U_{hist2} are determined by the par of resistors R6, R7 and R9, R10 respectively and they are calculate according to middle points V_{set1} and V_{set2}. Maximal high threshold V_{high1} =

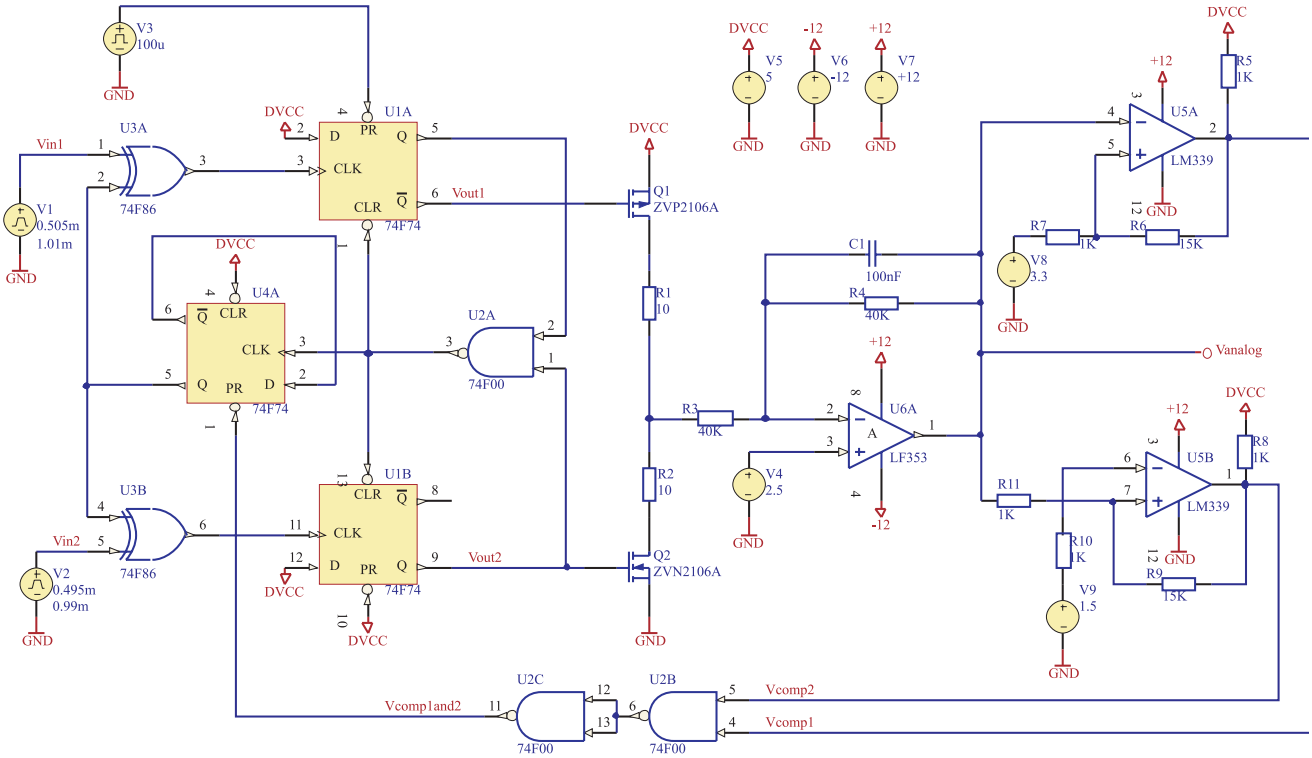

Fig. 7 Digital Frequency Sensitive Phase Detector with Controllable Phase-To-Voltage Response

V_{max}, so middle points are $|V_{set1,2.max}| = \frac{3U_{max}}{4}$ and histeresis is $U_{hist1,2.max} = \frac{U_{max}}{2}$. However this conditions are critical and not recommended to use.

Simulation analysis of the circuit from Fig. 7 is done, by the method described in [3]. The results are shown in fig. 9. This simulation has the same initial conditions and parameters as the simulation shown in fig. 3 and Fig. 6.

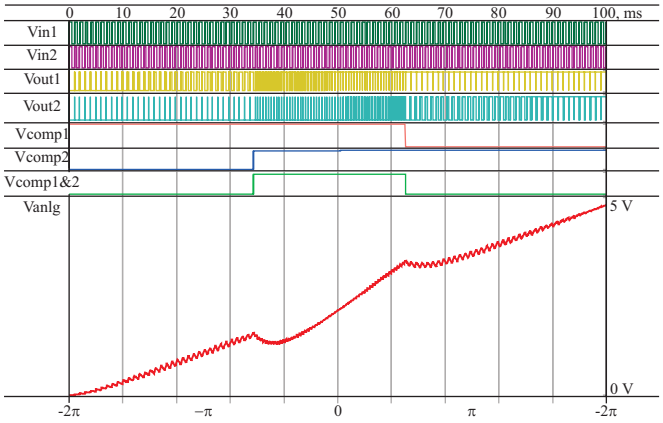

Fig. 9 Phase-to-voltage response of Digital Frequency Sensitive Phase Detector with Controllable Phase-to-Voltage Response: sweep from -2π to +2π and $f_{in2} > f_{in1}$

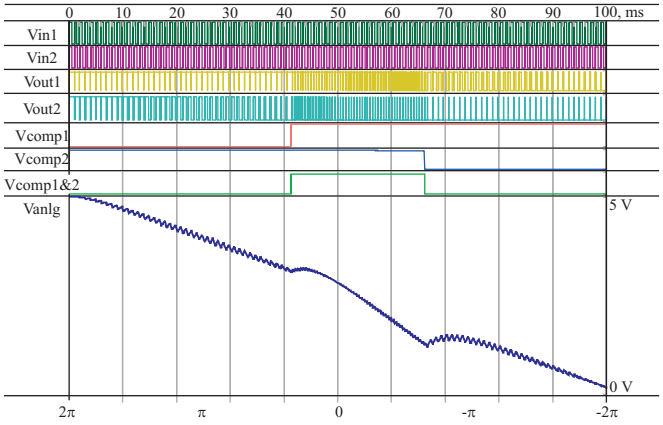

Fig. 10 Phase-to-voltage response of Digital Frequency Sensitive Phase Detector with Controllable Phase-to-Voltage Response: sweep from +2π to -2π and $f_{in1} > f_{in2}$

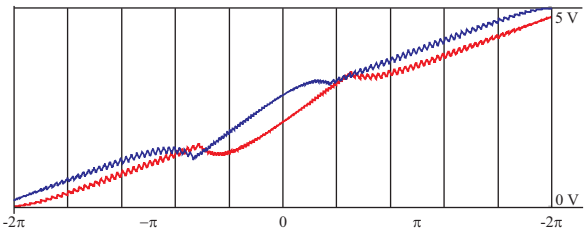

Fig. 11 Histeresis of the phase-to-voltage response, sweeping the phase from -2π to +2π (red trace) and back from +2π to -2π (blue trace)

Fig. 11 shows the histeresis of the phase to voltage response sweeping the in the range of 4π in two directions: up and back. One can see that in the different directions the zero point of the response is moved. This is due to the non-ideality of the integrator U5A (the resistor R4 is connected parallel to the capacitor C1, providing the stability of the integrator).

III. Conclusions and Discussion

Investigated is the most used in practice digital Frequency Sensitive Phase Detector working only on rising edge of input signals – FSPD type 1. Based on this it is developed PD working on both edges of input signal – FSPD type 2. The main advantage of FSPD type 1 is wide working range from -2π to +2π, which makes it very useful in a lot of applications. FSPD type 2 has the advantage of doubled output frequency which makes filtration easier and the PLL circuit more sensitive to phase or frequency deviations.

The issue with using that PD is its limited working range from –π to +π and existence of areas of non-sensitivity from -2π to -π and from + π to +2 π. The solution which can combine the advantages of both schemes is shown in fig. 7 and it is based on using the Reset input of "control" D flip-flop. This gives ability to switch the FSPD operation between type 1 and type 2. The criteria of switching can be analog threshold detected by comparators as shown in fig. 7 or can be digital control after digital processing of output signals of PD. This control is highly dependent on the specific realization of PLL circuit.

Acknowledgement

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