Development and Study of Two-channel Programmable Pulse Synthesizer

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Abstract – **Two-channel programmable pulse synthesizer is presented in the paper. It is intended to generate two-phase control signals to form a pause for commutation of the switch transistors in resonant inverters. The implementation is based on Direct Digital Synthesis and Field-Programmable Gate Arrays.**

Keywords – **resonant inverter, direct digital synthesis, field-programmable gate arrays, pause between commutations of the switch transistors, power regulation factor.**

I. INTRODUCTION

The quasi-resonant and resonant inverters (RI) are widely applied in induction heating of various materials for surface hardening, surface melting, casting etc. The optimal operation of the system inductor-detail depends on the parameters and the operation modes of the active and passive components of the RI and the equivalent parameters of the whole circuit. During the technological process these parameters vary in some limits because of the temperature changes. It is necessary to know how they change in order to measure the values of the important mode parameters. The aim is to control and/ or regulate the operation of the RI to achieve optimal regimes [4].

Aim of the paper: Development and study of two-channel programmable pulse synthesizer for monitoring and control of a class of resonant inverters allowing regulating in real time the power of the inverter in a wide range.

Main problems:

§ Defining the features of the synthesizer: two channels for generating two-phase square waves allowing to control (regulate) the frequency and the duration of the pause and hence to regulate the output power in a wide range.

§ Implementation of the synthesizer using Direct Digital Synthesis (DDS) and Field-programmable gate arrays (FPGA);

§ Design and simulations of the synthesizer.

II. ANALYSIS OF THE OBJECT BEHAVIOR AND DEFINING THE LIMITS OF THE OUTPUT POWER

A circuit of a transistor full bridge RI is shown in [4] and also analyses of some aspects of the induction heating technological process in relation to its control is presented. Some important conclusions, necessary for the development, will be reminded bellow.

During the technological process, while the temperature T of the heated material increases, its features and hence its active and reactive resistance change [7]:

$$Z_T = R_T + j\varpi L_T = f(\Delta T) \quad (1)$$

These changes determine variations of the output power. In order to achieve optimal operation regime of the RI it is necessary to regulate in some limits either the frequency of the control pulses or their duration.

The suggested circuit allows regulation of both the frequency and the pause between the two channels in real time.

The full-bridge RI is controlled by pulse signals with equal parameters (in our case *ChA* and *ChB*), transferred to the switching components in the two parts of the inverter, and with phase angle 2π between them.

Fig. 1 shows the relation between the two control signals, where: T_C is the control signals period; τ_I - the duration of the pulses; τ_P the duration of the pause in one period of the control signal, defined by Eq. (2):

$$\tau_P = 2\tau_r + \tau_I \quad (2)$$

τ_r - the duration of the pause between two consecutive pulses in the both control signals.

The value of τ_r can be defined, taking into account two

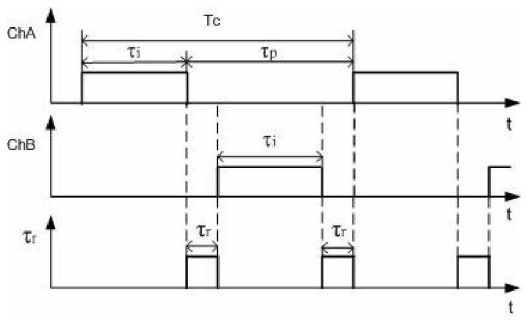

Fig. 1. Waveforms of the control signals for the switch transistors in the RI

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considerations - the first one is that two serially connected transistors must not be turned on at one the same time, and the second is that with increasing the pause the power in the inductor of the RI decreases. The power regulation factor k_r can be determined by Eq. (3) [4]:

$$k_r = 2\tau_I / T_C = 1 - 2\tau_r / T_C \quad (3)$$

The limits of k_r depend on the time intervals for switching on and off the transistors and on the necessary output power of the inverter [4]:

$$0 \le k_r \le 1 - 4k(t_{off} - t_{on}) / T_C, \quad (4)$$

where t_{on} is the turn-on time of the transistor, t_{off} – the turn-off time and k is a safety coefficient, which can vary in the following range $1{,}1 \le k_1 \le 1{,}5$.

III. Architecture of Two-channel Programmable Pulse Synthesizer

The power regulation factor in the presented circuit can vary from 51% to 99%. Fig. 2 shows the architecture of the Two-channel programmable pulse synthesizer [3].

The design is based on Altera's FPGA Cyclone EP1C6Q240C8 [2]. The free version of the development software Quartus II 8.1 Web Edition [5] has been used. The design is created using the Quartus II Block Editor and library functions. The synthesizer includes the following building blocks:

- **Input data block [6]**, consisting mainly of the shift registers *lpm_shiftregx*. It interfaces the control unit, implemented for instance by microcontroller, and the rest blocks of the synthesizer. It transfers serially the frequency control words for *NCO1* and *NCO2* and the control signals *mngx*.

The purpose of the inputs is as follows: *data_clk2* – clock input from the control unit; *reg_cnt* – determines input of either shift register address, or data into the selected shift register; *data_in* – address or data input.

- **Numerically controlled oscillator 1 (NCO1) block** – consists of the adder *lpm_add_sub0 (inst)* and the register *lpm_dff0 (inst12)*. Its principle of operation is expressed in many references, for example [1], [8], etc. The input *clk* is the clock source of the blocks NCO1 and NCO2. The purpose of NCO1 is to setup the PWM resolution of the output signals *ChA* and *ChB*. The output of NCO1 (f_{NCO1}) is a clock signal for the counters 74193 and the logic in the last block, synthesizing the output signals. The frequency of NCO1 is determined by Eq. (5):

$$f_{NCO1} = \frac{k_2 \cdot f_{clk}}{2^n}, \quad (5)$$

where: k_2 is the frequency control word, f_{clk} – clock frequency from the input *clk* for the both NCO blocks, n – the width of the phase accumulators of the NCO blocks.

The PWM resolution is expressed by Eq. (6):

$$\Delta f_{NCO1} = \frac{f_{clk}}{2^n}, \quad (6)$$

The output *q1_out* is intended for test purposes.

- **Block NCO2** is build up of the adder *lpm_add_sub0 (inst14)* and the register *lpm_dff0 (inst13)*. The frequency f_{NCO2} of the signal *q2_out (q2[31])* is determined using the Eq. (5), but with the constant k_3 – the frequency control word for NCO2, instead of k_2. The output *q2_out* is intended for test purposes too.
- **Block forming the pause** – consists of the counters 74193, which are cascaded into one 12-bits subtracting counter. They are initialized with the constant k_0 and determine the pause duration in the output signals. The greatest value of the pause is determined by Eq.(7):

$$\tau_P^{max} \le 2^{12} / f_{NCO1} = 2^{12} \frac{2^n}{k_2 f_{clk}} \quad (7)$$

- **Block synthesizing the output signals –** it is built up of the triggers *DFF* and the gates with three inputs. Its purpose is to synthesize the control signals for channel A and channel B (outputs *ChA* and *ChB*) of the inverter. Their frequency/ period are equal and they depend on the frequency/period of NCO2 output (Eqs. (8) and (9)).

$$f_C = f_{NCO2} / 2 \quad (8)$$

$$T_C = \frac{2^{n+1}}{k_3 \cdot f_{clk}}, \quad (9)$$

Table I shows the initializing constants for the proper operation of the synthesizer.

TABLE I
CONSTANTS AND CORRESPONDING BLOCKS USED IN THE SIMULATION AND PROGRAMMING OF THE DESIGN

constant	*Block used at simulation*	*Block used at programming*	*Purpose*
k_0	*lpm_constant0*	*lpm_shiftreg2 (inst10)*	Defines the pause duration for the two channels
k_2	*lpm_constant2*	*lpm_mux0 (inst18)*	Defines the NCO1 output frequency f_{NCO1}
k_3	*lpm_constant3*	*lpm_mux0 (inst20)*	Defines the NCO2 output frequency f_{NCO2}

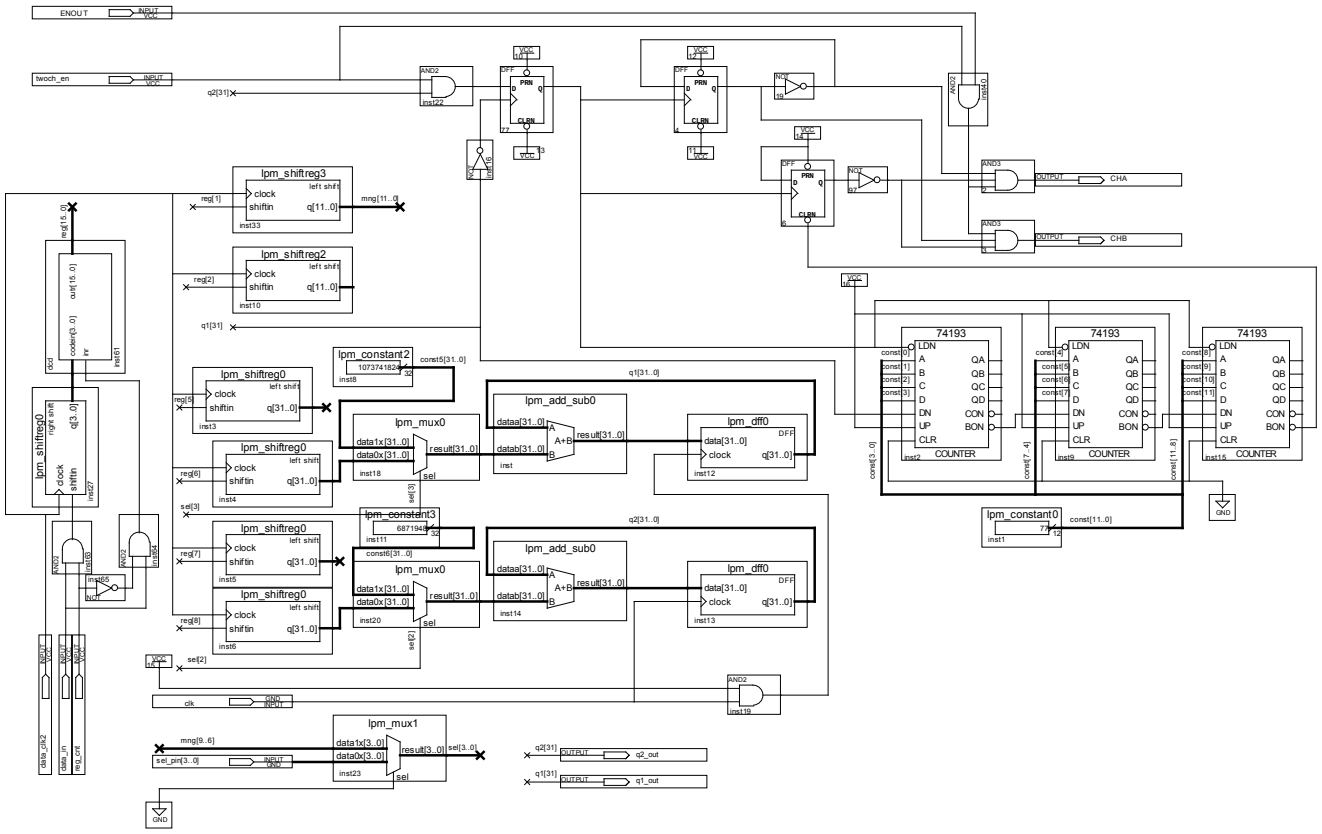

Fig.2. Architecture of two-channel programmable pulse synthesizer

IV. Simulation results of the Two-channel Programmable Pulse Synthesizer operation

To simulate the design it is necessary first to make a *.wvf* file with the input and output signals and the type of the input stimuli. It is created as a table in Quartus II and includes the outputs *ChA, ChB, q1_out* and *q2_out* and the following control signals: *sel_pin2* – controls the multiplexer *lpm_mux0 (inst20); sel_pin3* - controls the multiplexer *lpm_mux0 (inst18); ENOUT* and *twoch_en* – enable/ disable *Ch* and *ChB* output.

The value of the constant k_2 at f_{clk}*=50 MHz, n=32,* $f_{NCO1} = 12{,}5 MHz$, using Eq. (5), is $(1073741824)_{10}$. The PWM resolution is 80 ns.

Table II includes the input data for the simulations for two different resonant frequencies of the RI and the results are shown in Tables III and IV. Waveforms of the output and control signals of the two-channel synthesizer at different values of k_0 are shown in Figs. (3), (4) and (5).

164 logic elements from about total amount of 6000 and 14 I/O pins of FPGA have been used.

The power regulation factor k_P achieved has limits from 51% to 99%. The design can be modified in order to increase these limits.

TABLE II
CALCULATING THE CONSTANTS K_3 AND $k_0^{\max}$, OUTPUT FREQUENCY AND PAUSE OF THE TWO CHANNELS AT F_{CLK}*=50 MHz, N=32,* F_{NCO1} *=12,5 MHz/*T_{NCO1}*=80NS,* K_2*=*$(1073741824)_{10}$ FOR TWO DIFFERENT FREQUENCIES

$f_A=f_B=40$ kHz $T_A=T_B=25\,\mu s$		$f_A=f_B=3$ kHz $T_A=T_B=333\,\mu s$	
$f_{NCO2}=80kHz$ $T_{NCO2}=12{,}5\mu s$	k_3=6871948	$f_{NCO2}=6kHz$ $T_{NCO2}=166{,}7\mu s$	k_3=515396
$\tau_{II}^{\max}=6{,}25\mu s$	$k_0^{\max}=78$	$\tau_{II}^{\max}=83{,}375\mu s$	$k_0^{\max}=1037$

TABLE III
OUTPUT SIGNAL PARAMETERS AT F_{OUT}*=40 KHZ*

k_0	τ_i, μs	τ_P, μs	τ_r, μs	dc_{sim}, %	k_r, %
10	11,683	13.227	0.772	46.81	93.61
40	9,282	15.678	3.198	37.19	74.38
50	8,482	16.478	3.998	33.98	67.96
60	7,682	17.278	4.789	30.78	61.55
70	6,883	18.077	5.597	27.58	55.15
72	6,721	18.239	5.759	26.93	53.85

dc_{sim} is duty cycle at simulations

TABLE IV
OUTPUT SIGNAL PARAMETERS AT $F_{OUT}=3$ KHZ

k_0	τ_i, μs	τ_p, μs	τ_r, μs	dc_{sim}, %	k_r, %
10	165,922	167,438	0,758	49,77	99,55
50	162,721	170,639	3,959	48,81	97,62
70	161,123	172,237	5,557	48,33	96,66
100	158,722	174,638	7,958	47,61	95,23
300	142,720	190,64	23,96	42,81	85,63
500	126,723	206,637	39,957	38,01	76,03
700	110,724	222,636	55,956	33,21	66,43
1000	86,723	246,637	79,957	26,01	52,03
1030	84,323	249,037	82,357	25,29	50,59

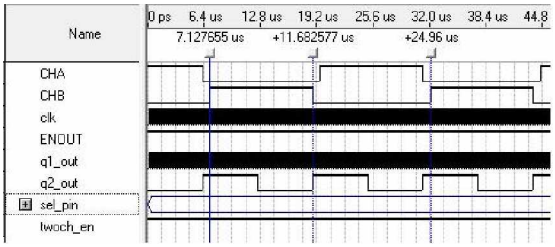

Fig.3. Waveforms of the output and control signals of the two-channel synthesizer at $k_0=10$ and $f_{out}=40kHz$

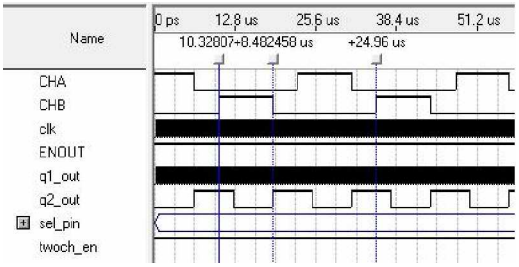

Fig.4.Waveforms of the output and control signals of the two-channel synthesizer at $k_0=50$ and $f_{out}=40kHz$

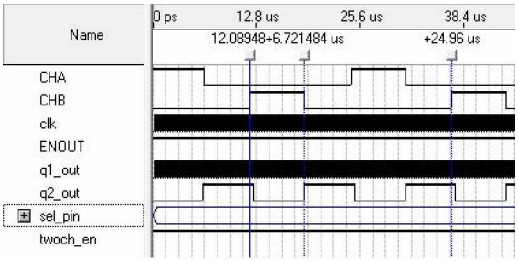

Fig.5. Waveforms of the output and control signals of the two-channel synthesizer at $k_0=72$ and $f_{out}=40kHz$

V. CONCLUSION

Two-channel programmable square-wave pulse synthesizer with opposite phases has been designed and simulated. Its purpose is to control a class of resonant inverters in real time. It is possible to regulate the frequency and the pause duration of the synthesized control signals and hence to regulate the output power of the RI in wide range. The suggested structure allows variations of the regulation factor from 51% to 99%. It is possible to modify it to reach a regulation range 1 - 99%.

The innovative method for direct digital synthesis determines very high PWM resolution. The design is based on cheap FPGA circuit with general purpose from which insignificant part of resources has been used. So the synthesizer can be used in more complex devices and systems, implemented in one FPGA.

REFERENCES

[1] A Technical Tutorial on Digital Signal Synthesis, Analog Devices, Inc., 1999.
[2] Cyclone Device Handbook, vol. 1, Altera Corp., 2005.
[3] Karailiev, H., V. Rankovska, "DDS Method for Generating a Frequency Grid at Systems for Test Control and Automated Regulation", ICEST 2006, Conference Proceedings, pp. 300-303, Sofia, Bulgaria, 2006.
[4] Karailiev, H., V. Rankovska, V. Karailiev. Embedded Microprocessor System for Monitoring and Control of Resonant Inverters. ICEST 2006 Conference Proceedings, Sofia, 2006, pp. 304-307
[5] Quartus II Version 5.0 Handbook. Vol. 1: Design & Synthesis, Altera Corp., 2005.
[6] Rankovska, V., H. Karailiev. Development and Study of One-channel Programmable Pulse Synthesizer. ICEST 2009 Conference Proceedings, Veliko Tarnovo, 2009, (forthcoming)
[7] Sluhockii, A. E., S. E. Riskin. Inductors for Induction Heating. Energy, Leningrad, 1974г. (in Russian)
[8] Tierney, Joseph, Charles M. Rader, Bernard Gold. A digital Frequency Synthesizer. IEEE Transactions on Audio and Electroacoustics, Vol. au-19, No. 1, March 1971, pp. 48-57