Design and Analysis of Ultra-Wideband Low Noise Amplifier in 0.13μm CMOS Technology

Alena Djugova[1], Jelena Radic[2] and Mirjana Videnovic-Misic[3]

***Abstract* – In this paper design of ultra-wideband (UWB) low noise amplifier (LNA) in 0.13 μm CMOS technology is presented. As a first block in a receiver chain LNA needs to provide adequate gain, low noise figure, input and output matching, low power consumption, small chip area and very wide bandwidth. For proposed LNA topology simulation results for basic figures of merit are given. Optimized LNA has maximum gain (S_{21}) of 15.77 dB with the 3-dB band from 2.5 to 5.4 GHz and return losses (S_{11} and S_{22}) of less than –8.4 dB and –18.9 dB, respectively. In addition, average noise figure of 1.5 dB is achieved, with power consumption of only 3.2 mA at 1.2 V.**

***Keywords* – Ultra-wideband (UWB), Low noise amplifier (LNA), Inductive degeneration, Quality factor, Resistive shunt-feedback, Inductive shunt peaking.**

I. INTRODUCTION

Ultra-wideband (UWB) system presents an emerging, low power, wireless technology offering a high data rates at small distances. UWB allocated band (IEEE 802.15.3a) is between 3.1–10 GHz (low-frequency band from 3.1–5 GHz and high-frequency band from 6–10.6 GHz) [1]. Two major solutions, Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) based on frequency hopping and Direct Sequence UWB (DS-UWB) are proposed to transmit the data rate up to 480 Mbps by using only the low frequency band. This low frequency band has been allocated for development of the first generation of UWB systems.

Design of low noise amplifier (LNA) maintains to be one of the challenging tasks in up-to-date receiver design. Being the first circuit in the receiver's chain it must meet several stringent requirements. It needs to provide sufficient gain to amplify received weak signal and to overcome the noise of the subsequent stages, low noise figure (NF) to improve sensitivity and adequate input and output matching to improve reflection coefficients. All this requirements have to be fulfilled within defined (wide) bandwidth and with low power consumption. In Section II several circuit techniques, proposed in literature to target these goals, are described.

In this paper broadband LNA topology, which merge narrowband LNA architecture with inductive source degeneration and resistive shunt-feedback technique, is proposed. Analysis of chosen topology is given in Section III. Simulated figures of merit (FOMs) are given in Section IV followed by discussion of achieved trade-offs and advantages of presented topology. The Section V concludes the paper.

[1]Alena M. Djugova is with the Faculty of Technical Sciences, Trg D. Obradovica 6, 21000 Novi Sad, Serbia, E-mail: alenad@uns.ac.rs

[2]Jelena B. Radic is with the Faculty of Technical Sciences, Trg D. Obradovica 6, 21000 Novi Sad, Serbia, E-mail: jelenar_@uns.ac.rs

[3]Mirjana S. Videnovic-Misic is with the Faculty of Technical Sciences, Trg D. Obradovica 6, 21000 Novi Sad, Serbia, E-mail: mirjam@uns.ac.rs

II. WIDEBAND AMPLIFIERS TOPOLOGIES

Two major UWB LNA design goals are wide band and low NF. There are four basic techniques used to obtain wide frequency band: distributed amplifier, common gate circuit, inductively degenerated common source amplifier incorporated with additional input band-pass LC-filter and common source amplifier with resistive shunt-feedback.

Distributed amplifiers can provide flat gain over the wide frequency band. To achieve necessary gain several amplifying stages are needed. Consequently, this approach is power hungry and area consuming. Moreover, difficult NF optimization for this technique is still an issue [2].

Second approach utilizes common gate circuit that provides wideband input matching. Main disadvantage of common gate amplifiers is their relatively low transconductance value that can not provide low noise and high gain in a whole frequency range. This type of amplifier is usually used as the first stage of multi cascade amplifiers where the next stages enhance the amplification bandwidth [3].

The inductively degenerated common source amplifier incorporated with additional input band-pass LC-filter represents another technique for achieving broadband input matching. In addition gain flatness and low power consumption are achieved. However, large number of on-chip reactive elements demand high chip area and degrade NF at higher frequencies [4].

Common source amplifier with resistive shunt-feedback provides wideband input matching and flat gain [5, 6]. Input resistance is determined by the feedback resistance divided by the voltage gain of the common source amplifier [7]. To obtain 50Ω input match few hundred Ohms for feedback resistance is needed, which results in NF degradation. Moreover, due to strong dependence of voltage gain on the amplifying transistor transconductance, the amplifier requires a large amount of current to achieve high gain.

III. CIRCUIT DESIGN

In this paper, an inductive degenerated amplifier circuit is modified with resistive feedback. This method is selected to achieve high gain, low noise and low power consumption LNA for the low-frequency band from 3.1–5 GHz. Proposed method is based on extending the operational bandwidth of

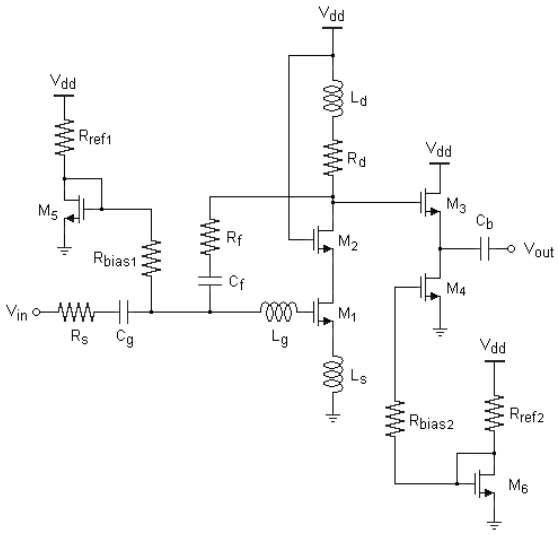

Fig. 1. Cascode feedback LNA topology

existing narrowband systems in order to cover UWB frequency band.

Schematic of a one stage LNA is shown in Fig.1. Transistors M_1 and M_2 are connected in cascode to improve the reverse isolation of the circuit. Additionally, cascode topology reduces effective M_1 input capacitance and helps to obtain higher gain and broader bandwidth. The source follower composed of transistors M_3 and M_4 form the output buffer and provides output wideband matching. Bias circuit is composed of resistors R_{ref1}, R_{bias1} and transistor M_5, where transistor M_5 forms current mirror with M_1. To decrease the overall power consumption (P_D), transistor M_5 width, W_5, should be small fraction of transistor M_1 width, W_1. The value of R_{bias1} is chosen large enough to provide high impedance path to RF signal while giving at the same time small contribution to the circuit noise. For biasing of output matching circuit the same bias circuit topology is used, composed of transistor M_6 and resistors R_{ref2} and R_{bias2}.

LNA architecture is input matched using inductive source degeneration (L_s in the schematics). As this method do not use additional noisy components (resistors) lower noise figure (*NF*) is expected. The source degenerated LNA first order input impedance Z_{in} (assuming feedback effect negligible and ignoring C_{gd}) is equal to:

$$Z_{in} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} \cdot L_s, \qquad (1)$$

where C_{gs} is total gate-source capacitance and g_m is transconductance of the input RF transistor M_1. At resonant frequency ω_0, where imaginary parts cancel, input impedance becomes:

$$imag(Z_{in}) \mid \omega_0 = 0 \rightarrow Z_{in} = \frac{g_m}{C_{gs}} \cdot L_s = \omega_T \cdot L_s \ . \qquad (2)$$

In case of the perfect input LNA match with source degeneration inductor L_s, input impedance $Z_{in} = \omega_T \cdot L_s$ is equal to source resistance $R_s = 50\Omega$.

An additional degree of freedom is provided by the gate inductance L_g that is used to set the resonance frequency ω_0 given by:

$$\omega_0 = \left[(L_g + L_s) \cdot \frac{C_{gs} \cdot C_g}{C_{gs} + C_g} \right]^{-\frac{1}{2}}. \qquad (3)$$

Quality factor of the series resonating input circuit is:

$$Q_{nb} = \frac{1}{(R_s + \omega_T \cdot L_s) \cdot \omega_0 \cdot C_{gs}}. \qquad (4)$$

The (–3-dB) bandwidth of RLC resonant circuit is inversely proportional to its Q-factor ($BW_{-3dB} = \omega_0/Q_{nb}$) [8], therefore high Q value is not desirable in the wideband design. To achieve broad band, resistor R_f is added as a shunt-feedback element to reduce Q-factor of the resonating narrowband LNA circuit. Resistance R_f can be much larger that in the conventional resistive shunt-feedback circuits where the size of the R_f is limited as it determines low input impedance. Miller equivalent input resistance of R_f is given by [7]:

$$R_{feq} = \frac{R_f}{(1 - A_v)}, \qquad (5)$$

where A_v is the open-loop voltage gain of an LNA. With this transformation Q-factor of the input circuit shown in Fig. 1 is given by:

$$Q_{wb} = \frac{1}{(R_s \,||\, R_{feq} + \omega_T \cdot L_s) \cdot \omega_0 \cdot C_{gs}}. \qquad (6)$$

It can be seen from (6) that by proper R_{feq} selection narrowband LNA can be transformed into wideband LNA.

In Fig. 1 resistive and capacitive shunt-feedback (R_f and C_f) are employed to produce better stability, gain flatness and bandwidth. Capacitor C_f is used for the ac coupling purpose while large values of feedback resistor also improve input impedance matching without affecting the noise figure significantly [9]. Additionally, technique called inductive shunt-peaking, applied by series connection of L_d and load resistance R_d, is used to increase bandwidth and improve gain flatness [8].

Capacitors C_g and C_b are input and output DC blocking capacitors. Their values are chosen large so they do not influence the resonant frequency of the input and output circuit, respectively.

IV. Simulation Results

The designed circuit has been simulated using Spectre Simulator from Cadence Design System. To achieve wideband LNA that covers frequency band from 3.1–5 GHz narrowband amplifier (without feedback) was optimized at 4GHz central frequency. To obtain initial device dimensions and component values in UMC 0.13µm CMOS eight-metal

technology the optimization technique with constant power consumption is used [10]. After shunt-feedback resistor introduction frequency band is extended to desired boundaries. In order to get simulation results as close as possible to measurement results, BSIM3V3 models for all circuit components were introduced. Due to increased complexity of the circuit it was necessary to carefully examine dependence of the LNA FOMs on circuit parameters. This has been carried out by changing values of one by one circuit parameter analyzing at the same time the LNA performance behavior.

LNA topology was optimized with the main aim to minimize *NF* and P_D, improve voltage gain while still keeping acceptable values for remaining FOMs. Simulation results for the cascode LNA topology are given in Figs. 2–4 (S_{11} and S_{22}, S_{12} and S_{21}, *NF* and NF_{min}).

Parameter S_{11} is below –8 dB in the band of interest (–8.812 dB at 3.1 GHz and –8.336 dB at 5 GHz) and is less than –7 dB from 3–5.4 GHz. This demonstrates the effectiveness of wideband matching realized by matching network (L_s and L_g), shunt-feedback and shunt-peaking load. The lowest S_{11} value can be seen at 4 GHz. This result is in accordance with expectations as initial LNA topology is optimized at this frequency. Increase in R_f value results in flatter characteristics, with S_{11} minimum shifted to the higher frequencies and higher maximum S_{11} value (S_{11} closer to zero). The same effect can be seen with increase in L_d inductor value. The first block of the proposed LNA topology can be roughly seen as basic common source amplifier with resistive R_f shunt-feedback and $Z_D = R_d + j\omega L_d$ drain impedance. Though there are some difference, such as source degeneration and cascode part of topology, some R_{in} and A_v properties can be more easily seen in simplified structure. In the basic common source amplifier with resistive R_f shunt-feedback and Z_D drain resistance input resistance and voltage gain at lower frequencies are:

$$R_{feq} = \frac{R_f + Z_D}{1 + g_m \cdot Z_D}, \tag{7a}$$

$$A_v \approx -\frac{g_m \cdot R_f \cdot Z_D}{R_f + g_m \cdot R_s \cdot Z_D} = -\frac{1}{\frac{1}{g_m \cdot Z_D} + \frac{R_s}{R_f}}. \tag{7b}$$

From (7a) can be seen that R_f increase results in R_{feq} increase. According to (6) Q_{wb} is lower and BW wider, which is in accordance with simulation results. To shift the position of the flat and minimum part of the S_{11} spectrum larger inductor L_g values need to be used. As L_g increase narrow the S_{11} characteristic trade-off between its value and wanted bandwidth has to be achieved.

Parameter S_{22} is less than –18.9 dB for the frequency band of interest and below –16.45 dB for the whole simulated range. The excellent reverse isolation (S_{12}) below –43 dB is also obtained.

Regarding the gain, maximum S_{21} parameter value of 15.77dB is achieved with 3-dB band from 2.48GHz to 5.4GHz. Size of the amplifying transistor M_1 is chosen to be 230.4 μm for optimum S_{21} and noise performance. Width of M_1 determines the gain at the lower frequencies while width

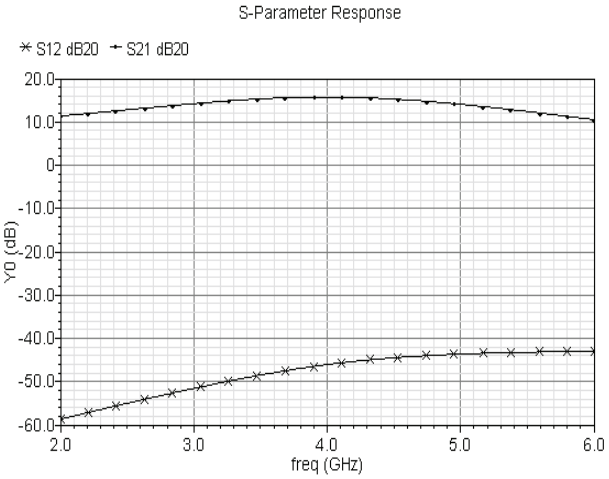

Fig. 3. LNA input-output isolation (S_{12}) and voltage gain (S_{21})

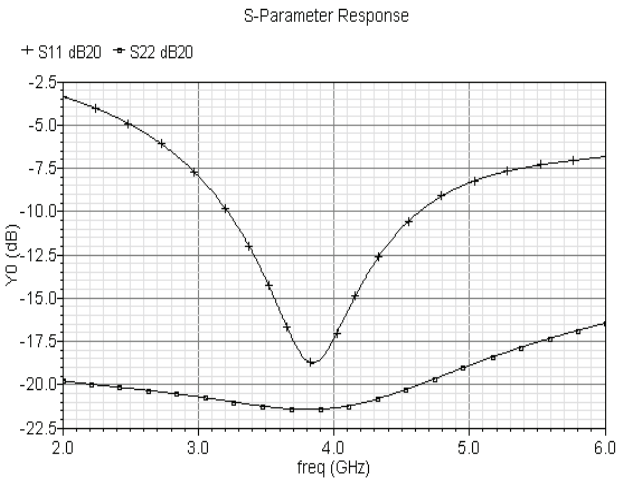

Fig. 2. LNA input (S_{11}) and output (S_{22}) return loss

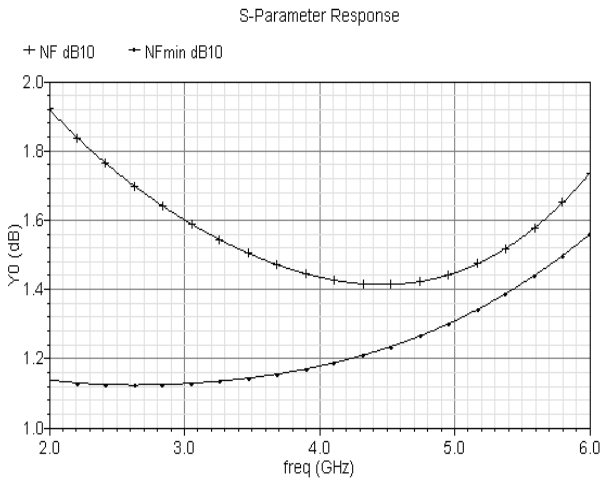

Fig. 4. LNA noise figure (*NF*) and minimum noise figure (NF_{min})

of M_2 (57.6 μm) represents the trade-off between gain and –3dB bandwidth. These values satisfy the gain requirement, while keeping at the same time P_D at reasonable level. Parameter R_f increase results in S_{21} increase, that can also be seen from (7b). For voltage supply V_{DD}=1.2V, a total current including the biasing circuits and output buffer is 3.2mA. The core consumes 1.9mA, while the rest is consumed by the buffer (1mA) and biasing circuits (0.260mA).

NF is flat over the simulated range with the average value of 1.5 dB. Minimum NF value of 1.414 dB is obtained at 4.47GHz. This value is close to NF_{min}, the minimum possible NF value.

Stability parameters simulations were performed from 2GHz to 6GHz. Unconditional stability requirements for the whole simulated range is satisfied. Minimum values for stability factors K_f (Rollet stability factor) and B_{1f} (alternate stability factor) are equal to 12 and 1, respectively, which are values much higher than 1 and 0 [11, 12].

The optimized FOMs of designed LNA and FOMs values of similar LNA topologies in the frequency band of interest [13, 14, 15] are summarized in Table I. In comparison with LNAs FOMs found in literature, design presented in this paper shows higher S_{21}, lower power consumption and *NF*. This result is achieved for simple cascode topology, without additional improvement techniques such as current reuse and cascade. While comparing amplifier design in this work and [13], simulated in the same technology, it can be seen that proposed design have better values for almost all FOMs. The cascade source degenerated LNA design, presented in [14], achieves the best S_{11} value using band-pass filter at a price of large number of reactive elements that causes higher *NF*, power consumption and larger chip area. The same gain value is obtained in [15] where current reuse topology is used. The design [15] drawback is high power consumption and higher *NF* since more circuit elements are needed.

TABLE I
PERFORMANCE COMPARISON

	This work	[13]	[14]	[15]
BW [GHz]	3–5	3–5	3–5	3–5
S_{11} [dB]	<–8.4	<–10	<–10	<–9
S_{22} [dB]	<–18.9	N/A	<–10	<–8.5
S_{21} [dB]	15.77	11	14	14
NF [dB]	1.41	1.8	2	2.4
Power [mW]	3.8	5.2	9	12
Technology	0.13μm	0.13μm	0.18μm	0.18μm

V. CONCLUSION

In this paper low-power approach for ultra-wideband low noise amplifier design in the 3.1–5 GHz band is demonstrated. Using single stage cascode amplifier topology, high gain and low noise can be achieved in the desired frequency range consuming only 3.8mW. Due to the LNA architecture simplicity, input and output is strongly coupled which makes impedance input/output matching more difficult. To obtain required S_{11} parameter value typical source degenerated amplifier is expanded using shunt-feedback resistor. This technique gives adequate input match without introducing large number of additionally components (inductors and capacitors). Obtained simulation results prove that matching method used in this paper together with shunt-load peaking is good solution for UWB LNA design.

ACKNOWLEDGEMENT

This research was supported by the Serbian Ministry of Science and Technological Development (contract TR-11023 and TR-11006) and FP6-INCO project (contract number 043669).

REFERENCES

[1] G. R. Aiello, G. D. Rogerson, “Ultra-Wideband Wireless Systems”, IEEE Microwave Magazine, vol. 4, pp. 36–47, 2003.

[2] P. Heydari, D. Lin, "A Performance Optimized CMOS Distributed LNA for UWB Receivers", CICC'05, Proceedings of the IEEE 2005, pp. 337-340, San Jose, California, USA, 2005.

[3] K. Chen, J. Lu, B. Chen, S. Liu, “An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-μm CMOS”, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 3, pp. 217-221, 2007.

[4] A. Bevilacqua, A. M. Niknejad, “An Ultrawideband CMOS Low Noise Amplifier for 3.1–10.6-GHz Wireless Receivers”, IEEE Journal of Solid-State Circuits, vol. 39, pp. 2259-2268, 2004.

[5] F. Bruccoleri, E. A. M. Klumperink, B. Nauta, "Noise Canceling in Wideband CMOS LNA’s", ISSCC'02, Digest of Technical Papers, pp. 406–407, San Fransisco CA, USA, 2002.

[6] S. Andersson, C. Svensson, O. Drugge, "Wideband LNA for a Multistandard Wireless Receiver in 0.18 μm CMOS", ESSCIRC'03, Conference Proceedings, pp. 655–658, Estoril, Portugal, 2003.

[7] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York, McGraw-Hill, 2001.

[8] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

[9] F. Ali, C. Hutchinson, A. Podell, “A Novel Cascode Feedback GaAs MMIC LNA with Transformer-Coupled Output using Multiple Fabrication Process”, IEEE Microwave and Guided Wave Letters, vol. 2, pp. 70–72, 1992.

[10] D. K. Shaeffer, T. H. Lee, “A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier”, IEEE Journal of Solid-State Circuits, vol. 32, no. 5, pp.745-759, 2005.

[11] SpectreRF simulator, Cadence Design System, www.cadence.com

[12] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Prentice Hall, 1984.

[13] A. Mirvakili, M Yavari, "A Linear Wideband CMOS LNA for 3–5 GHz UWB systems", ISOCC'08, Conference Proceedings, pp. 150–153, Busan, Korea, Portugal, 2008.

[14] H.-Jin Lee, Dong Sam Ha, S.S. Choi, "A Systematic Approach to CMOS Low Noise Amplifier Design for Ultrawideband Applications", ISCAS'05, Conference Proceedings, pp. 3962–3965, Kobe, Japan, 2005.

[15] B. Ansari, H. Shamsi, A. Shahhoseini, "Analysis of a 3–5 GHz UWB CMOS Low-Noise Amplifier for Wireless Applications", MWSCAS'09, Conference Proceedings, pp. 979–982, Cancun, Mexico, 2009.