Realization of Direct Digital Synthesis Generators Based on FPGA and PSoC Integrated Circuits

Eltimir Ch. Stoimenov[1] , Georgi S. Mihov[2] and Ivailo M. Pandiev[3]

***Abstract* – This paper presents an implementation of a Direct Digital Synthesis (DDS) generator incorporating FPGA and "System on Chip" (PSoC) technologies. The DDS is a digitally-controlled method of generating multiple frequencies from a reference frequency source. An evaluation board equipped with a FPGA Spartan-3A and a PSoC (from Cypress Inc.) integrated circuits were used for development. PSoC is a programmable integrated circuit obtaining certain analog and digital recourses with general purpose. In the current research the FPGA is synthesize sinusoidal, or other, signal in digital form. The synthesis itself is achieved by a Look-Up Table (LUT) containing 256 samples. An UART interface is used to transfer the information from the FPGA to a PSoC where an 8 bit digital-to-analog conversion (DAC) took place. Moreover, a two pole low pass filter (LPF) and a programmable gain amplifier (PGA) is incorporated in the PSoC. In addition the parameters of the created DDS generators can be controlled by a personal computer through a USB interface.**

***Keywords* – Mixed-signal systems, Function generators, Direct Digital Synthesis, FPGA, PSoC.**

I. INTRODUCTION

The function generators have been found useful in many applications, such as analogue and mixed-signal processing, telecommunications, and measurement systems. Additionally, the principals of oscillation can be extended to construct other types of generators, such as voltage-controlled oscillators (VCOs), quartz crystal resonator sensors, voltage-to-frequency converters, etc. [1-4]. The traditional hardware realization of function generators uses closed-loop analog circuits with active and passive elements or digitally-controlled method of generating multiple frequencies from a reference frequency source called Direct Digital Synthesis (DDS) [1]. The main advantage of the DDS generators is that the typical amplitude stabilization is not higher than 0,01% and the typical THD is 0,1% [5]. Generally, the DDS generators are a type of frequency synthesizer used for creating arbitrary waveforms. In them stable clock oscillator drives a Programmable-Read-Only-Memory (PROM) which stores one or more integral number of cycles of a sine waveform (or other arbitrary wave-form, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a Digital-to-Analog Converter (DAC) which in turn generates the analog output signal. Nowadays, one of the most effective techniques for realization of DDS generators is by using Application Specific Integrated Circuits (ASICs) with fixed electrical parameters (such as the DDS function generators from Analog Devices) or by developing electronic circuit based on FPGA (Field Programmable Gate Array) and PSoC (Programmable-System-On-a-Chip). The FPGA ICs are becoming more popular and are used in many mixed-signal applications [6-8]. To the authors' knowledge, DDS function generators based on FPGA and PSoC ICs have not yet been reported in the literature. It is, therefore, the purpose of this paper to present a programmable DDS function generator employing FPGA and PSoC ICs.

II. DIRECT DIGITAL SYNTHESIS (DDS) : GENERAL OVERVIEW

A frequency synthesizer, including DDS, generates multiple frequencies from one or more frequency references**.**

The block diagram of a classical DDS system is shown in Fig.1.

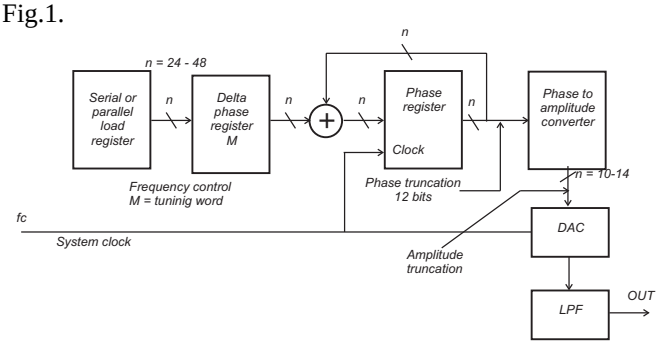

Fig. 1. Block diagram of DDS system.

The heart of the system is the *phase accumulator* whose content is updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M stored in the *delta phase register* is added to the number in the phase accumulator register.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) look up table. Each address in the look up table corresponds to a phase point on the sine wave from 0° to 360°. The LUT contains the corresponding digital amplitude information for one complete cycle of a sinewave. The LUT therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turns drive the DAC. Because of the symmetry of the sine wave, only data for 90° could be use for reconstruction.

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For an n-bit phase accumulator (n generally ranges from 44 to 32 in most DDS systems), there are 2^n possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If f_c is the clock frequency, then the frequency of the output sinewave is equal to

$$f_0 = \frac{M \times f_c}{2^n}. \quad (1)$$

This equation is known as the DDS "*tuning equation*". The frequency resolution of the system is equal to $f_c / 2^n$. For n = 32, the resolution is greater than one part in four billion [1].

III. DDS Function Generator Development Based on FPGA and PSoC

The current paragraph discusses the particular hardware and software realization of DDS function generator. Also the objectives and the approach are presented.

A. Objectives

Design a function generator with the following parameters:

- Output signal forms : *sine, triangular, square;*
- Frequency band : *0 – 2 MHz;*
- Frequency tuning method : *digitally - minimum 8bits resolution;*
- Amplitude tuning method : *digitally;*
- Output signal amplitude : *±10V*;
- THD: 0.1%
- PC connectivity: *via standard USB ports*.

B. Approach

In order the above objectives to be achieved a DDS function generator is designed with the block schematic shown in Fig. 2.

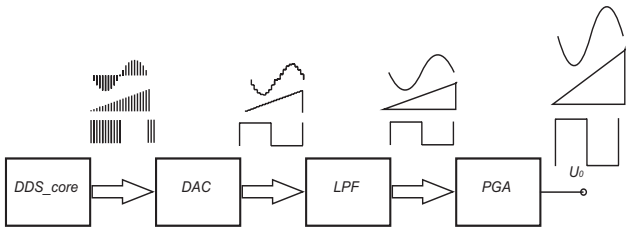

Fig. 2. DDS development block diagram.

The DDS core, shown on Fig. 2, generates a digital signal with a sine, triangle or square shape and passes it to a DAC. After the conversion the analog signal is filtered by an anti-imaging second-order Low-Pass Filter (LPF) and amplified by a Programmable Gain Amplifier (PGA).

In our development the DDS generating core is implemented on a FPGA, which allows best versatility and makes the design open for constant improvement. VHDL is used for programming FPGA IC. On the other hand the DAC function is accomplished by a PSoC from Cypress Inc. Using the PSoC technology also allows implementation of the LPF and PGA on the same integrated circuit. The above functions of DAC, LPF and PGA are realized by the graphical editor of PSoC Designer IDE from Cypress Inc.

Xilinx® Spartan®-3A Evaluation Kit from Avnet is used as a development platform for realization the circuits. It poses the following key features related to the current design [9]:

-Xilinx XC3S400A-4FTG256C Spartan-3A FPGA;
-Cypress 8C24894 PSoC;
-USB connectivity.

The block diagram of the Evaluation Kit is shown in Fig. 3. The blocks of interest are patterned.

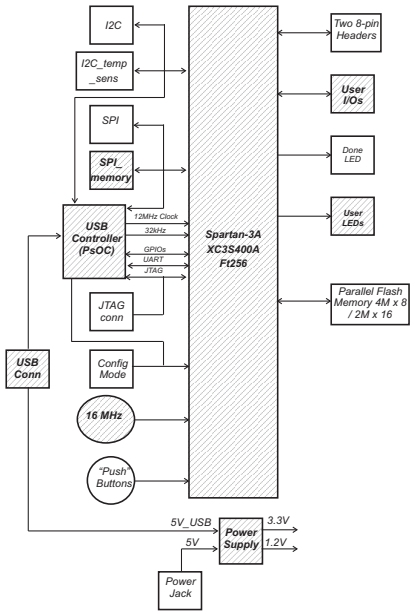

Fig. 3. Spartan 3A Evaluation board.

The block diagram of our DDS function generator development is presented on Fig. 4.

As it shown the FPGA contains the DDS core which generates different waveform signals, according to our objectives. The generated signal is transmitted through UART interface to the PSoC for further processing.

The PSoC itself contains all the necessary blocks for digital to analog conversion, filtering and amplifying the output signal. Moreover the embedded USB interface is used for communication with a PC. The control unit block decodes the commands sand by a PC. Than it adjust the gain of the PGA or transmit a command to the FPGA for frequency tuning or signal form. The programming of the PSoC is done on C programming language. The algorithm flowchart of the control unit is shown in Fig. 5.

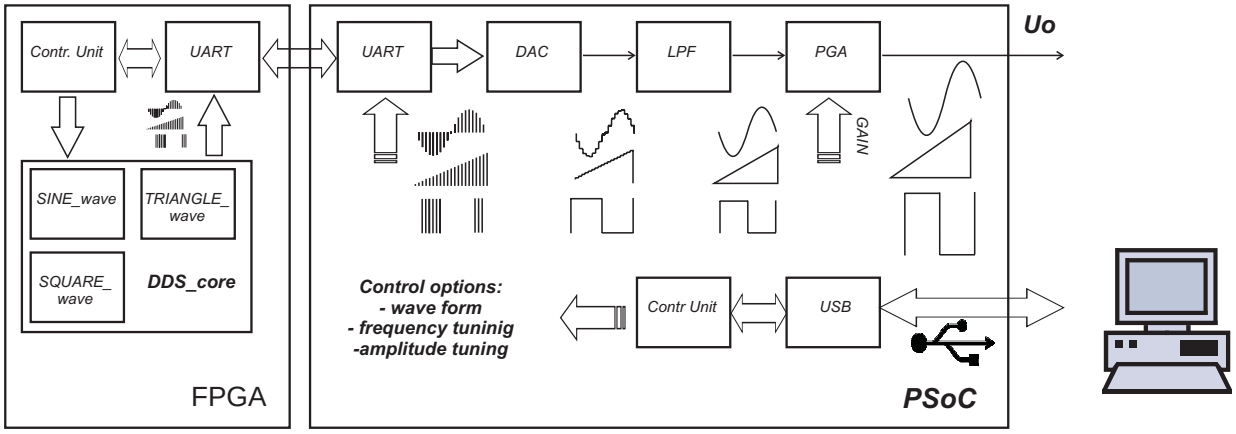

Fig. 4. Block diagram of DDS function generator.

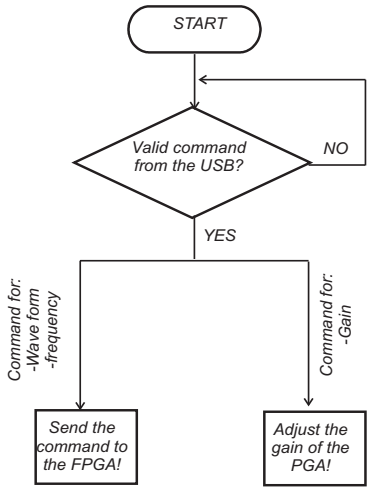

Fig. 5. Control unit flowchart.

The DDS core block from Fig. 4 incorporates three sub blocks. Each of these blocks produces one of the three output shapes – sine, triangle or square. The sine wave sub block has the block scheme represented in Fig. 6.

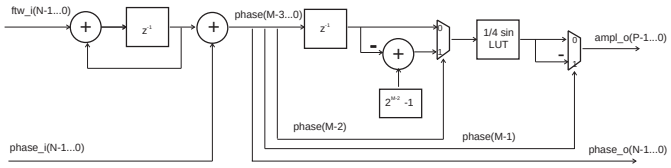

Fig. 6. Sine wave sub block.

As it can be seen from the figure only one quarter of the sine-wave is stored in the LUT, the rest is computed by simple operations (negating, subtraction), resulting in a reduced memory requirement. The resolution of the frequency tuning word (FTW), the phase and the amplitude can be defined separately [10].

A screen shot taken from PSoC Designer IDE (Cypress inc.) is presented in Fig. 7. As is shown in the "Analog Configuration Blocks" section the 8-bits DAC is connected with a second-order anti-imaging LPF. The filtered out signal is passed to a PGA for an output signal amplitude adjustment.

On the other hand the digital section contains an UART interface for communication with the FPGA. Also a 16-bits Timer for FPGA reset impulse production is implemented. The reset impulse duration is about 1*s* .

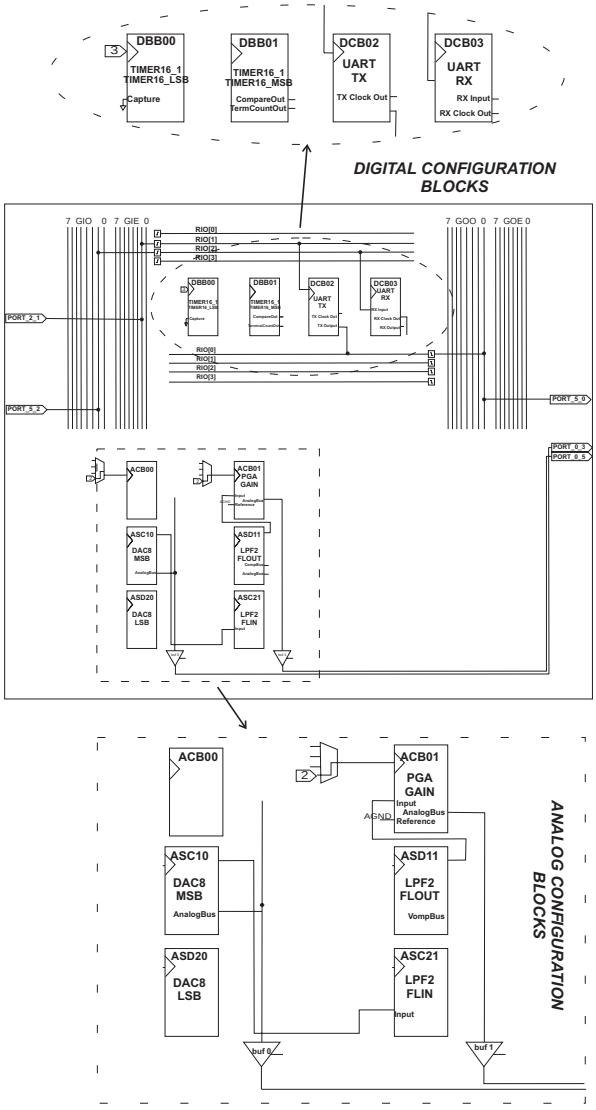

Fig. 7. PSoC Designer IDE – DDS project screen shot.

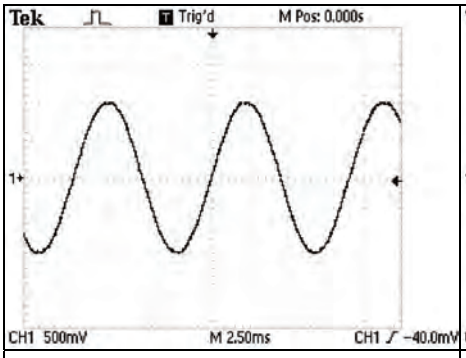

Fig. 8. Sinusoidal output signal.

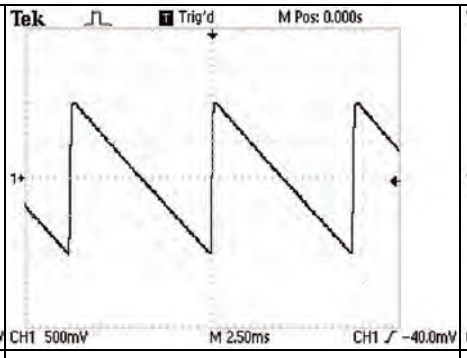

Fig. 9. Triangle output signal.

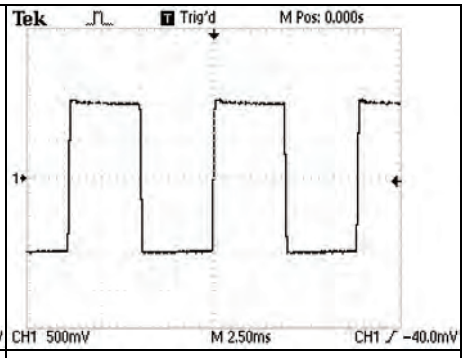

Fig. 10. Square output signal.

IV. Experimental Results and Discussions

This chapter presents some oscillograms from the experimental studies. The following technical equipment was used: Xilinx Spartan – 3A Evaluation Kit; Tektronix 1002B Oscilloscope (oscilloscope setup: AC mode and 10X probe attenuation); Personal computer.

Fig. 8 through Fig. 10 shows the sinusoidal, triangle and square output signals respectively. The signals amplitude and frequency are $1V$ and $114Hz$, respectively.

After analyzing the results a comparative table between the desired and achieved results could be make (Table 1).

TABLE I
COMPARISON BETWEEN DESIRED VALUES AND ACHIEVED EXPERIMENTAL RESULTS

Parameter	Desired	Achieved
Output signal shapes	*sine, triangular, square*	*DONE*
Frequency band	*0 – 2 MHz*	*0 – 200 Hz*
Frequency tuning method	*digitally / minimum 8bits resolution*	*DONE*
Amplitude tuning method	*digitally*	*DONE – 16 levels*
Output signal amplitude	±10V	0 - 3.3V
THD:	0.1%	*Future study*
PC connectivity	*via standard USB ports*	*DONE*

The table reveals the main problems of the development:

Problem 1 - Frequency bandwidth:

The achieved frequency bandwidth is in orders lower than the desired. Our study and analysis shows that the root cause is the low data transfer rate between the FPGA and PSoC. The UART, connecting the two ICs, appears to be constrained to about 37,5 kbps. Higher transfer rates lead to data errors.

Solution: Using another connecting protocol and finding better communication lines between the FPGA and PSoC may improve the results.

Problem 2 - Output signal amplitude:

The achieved output signal is unipolar and with small amplitude. The explanation is clear – the output of the PSoC is directly connected to the output of the system.

Solution: Buffering and amplifying the signal from the PSoC will resolve the problem.

IV. Conclusion

In conclusion we can restate that DDS is very modern and pliable technology. It allows flexible control of all the parameters of interest. Moreover the technology is not resource demanding and is convenient for implementation in microprocessor and mixed signal systems. Also using a FPGA and PSoC ICs greatly reduces the design workload and makes the system even more flexible.

By our personal opinion the objectives stated in chapter III are fulfilled sufficiently. Of course, the main problems, described in chapter IV, should be addressed in future developments.

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