Behavioural VHDL-AMS Model for the Current-Feedback Operational Amplifier

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***Abstract* – In this paper linear, frequency-dependent VHDL-AMS model for the Current-Feedback Operational Amplifier (CFOA) is introduced. The model simulates the actual performance of typical CFOAs for a wide range of frequencies. For creating the model, simplification and build-up techniques known from macromodelling operational amplifiers have been adapted. Model parameters are extracted for the CFOA AD8001 from Analog Devices as an example. To confirm the validity, the simulation results are compared with the manufacturer's data and with the results obtained by simulation of the PSpice macromodel supplied from Analog Devices.**

***Keywords* – Analog circuits, Current-feedback operational amplifier, Analog simulation, VHDL-AMS.**

I. INTRODUCTION

The CFOAs, as a variety of operational amplifiers (op amps) family, have been realized to overcome the finite gain-bandwidth product of VFOAs. The CFOAs can be represented as a cascade structure of positive second-generation current conveyor (CCII+) and an additional voltage buffer. Nowadays the CFOAs have emerged as one of the most important active building block in developing many analog and mixed-signal circuits and systems [1-3]. Testing the workability of the developed electronic circuits is usually done using SPICE (Simulation Program with Integrated Circuit Emphasis) with a company specifying macromodel for the CFOA. A variety of SPICE macromodels for the CFOAs, are available in the literature [4-10]. The majority of published SPICE based macromodels are presented as *device-* (*transistor-*) *level models*, called micromodels. Typically the input stage of the micromodels is a *device-level model* and other stages consist of an extensive number of passive elements, ideal controlled sources and ideal diodes.

Testing a complete analog system via transistor-level simulation is an extremely difficult process and can often become infeasible due to the limitation of simulation capacity. A similar difficulty is encountered when high-level design is performed for the whole system. For these reasons, compact models of analog blocks, and in particular, op amps are desired which can be substituted in place of the actual transistor-level netlist to speed up the simulation without sacrificing any of the required accuracy.

One method to decrease simulation time and improve the convergence, without a significant loose of information, is by using behavioural modelling technique. Behavioural modelling is a way of providing macroscopic models of the corresponding microscopic (microelectronic) circuits. The use of behavioural modelling for op amps has been well known for a few years. Behavioural models are realized by using structural macromodelling, the C code modelling, Analog Behavioural Modelling (ABM) available in PSpice A/D simulators and finally the behavioural modelling with VHDL-AMS.

Nowadays one of the most effective techniques for behavioural modelling of analog and mixed electronic circuits is by using VHDL-AMS. The conveyed literature survey reveals that behavioural models for the CFOAs have not been available yet. Without any doubt behavioural models for basic types of CFOAs, are necessary for simulating complex circuits. The goal of this paper therefore is to develop a simple behavioural VHDL-AMS model that accurately simulates the frequency performance of most common CFOAs.

II. CFOAS

The most common CFOA is equivalent to a CCII+ plus an output voltage buffer. These op amps have a high impedance non-inverting input y, a low-impedance inverting input x, a current output z and the voltage output o. In some of the CFOAs the port z, between the first stage (CCII+) and the second stage (voltage buffer), is defined as an external pin. This allows the usage of CFOAs in some specific selective amplifier circuits, sinusoidal oscillators and multivibrators. The port o is the output of the voltage buffer, where the resistance is very low (magnitude of several ohms). The simplified model of the CFOA is presented in Fig. 1. This model contains three parameters to be determined by measurements, i.e. α_{yx}, the y to x voltage gain, α_{xz}, the x to z voltage gain and α_{zo}, the z to o voltage gain. All these parameters are ideally equal to 1. For this model the general relation between input and output voltages and currents can be given as $i_y = 0$, $v_x = \alpha_{yx} v_y$, $i_z = \alpha_{xz} i_x$ and $v_z = \alpha_{zo} v_o$. If pin z is defined as an external port α_{yx} is measured by app-

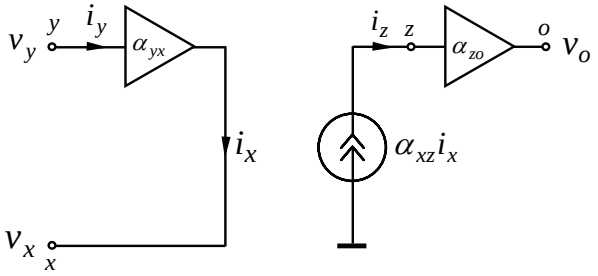

Fig. 1. A simple model of the real CFOA.

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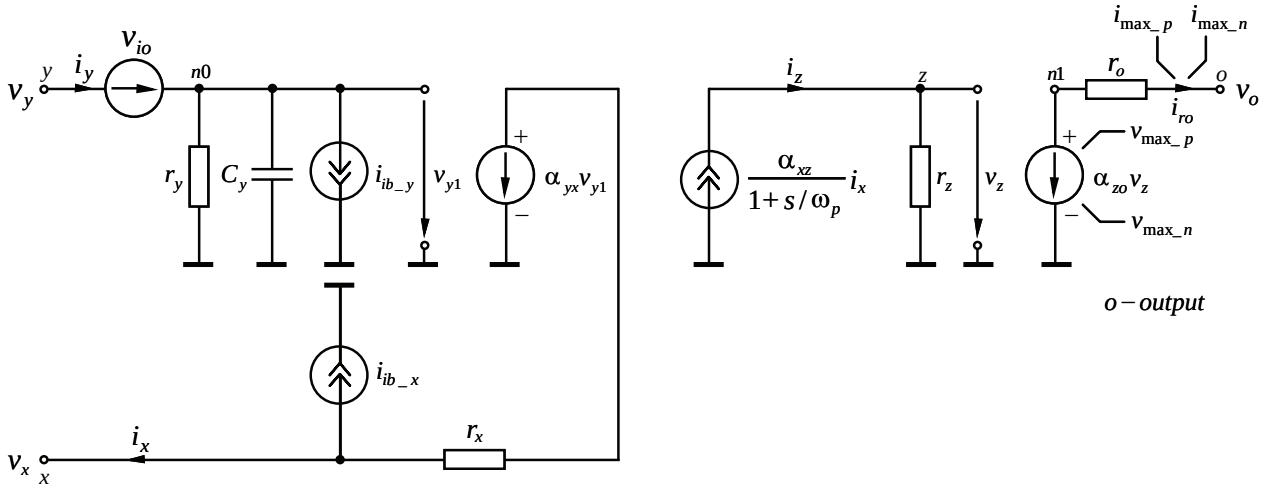


Fig. 2. Circuit diagram of the Current-Feedback Operational Amplifier (CFOA) behavioural model.

lying a voltage signal at port y and measuring the resulting voltage at port x. α_{xz} is measured by injecting a current signal at port x and measuring the output current at port z. Whereas α_{zo} is measured the same way as α_{yx}.

III. Behavioural Modelling with VHDL-AMS

The technical requirement for effective models is generally agreed when the simplest model possible is developed. Simple models have a number of advantages. They can be developed faster, are more flexible, require less data, run faster and it is easier to interpret the results since the structure of the model is better understood. As the complexity increases, these advantages are lost [11]. The proposed behavioural model of the CFOA is developed following the design method based on a Top-Down analysis approach and applying simplification and build-up technique. The process of model building and testing can be broken down into three basic steps: *structure the model*, *build the model* and *validate the model* [12].

A. A behavioural language: VHDL-AMS

VHDL-AMS is a comparatively new standard 1076.1 of VHDL that support hierarchical description and simulation of analog, digital and mixed-signal applications with conservative and non-conservative equations [13, 14]. On the analog side, a variety of abstraction levels is supported. The VHDL-AMS modelling is not restricted to electronic circuits, but also supports thermal, mechatronic, optical and other systems.

B. A CFOA behavioural VHDL-AMS model

The behavioural model of CFOA is built using the electrical characteristic curves obtained by analyses of the PSpice macromodel for AD8001AN [15]. In fact, the monolithic op amp AD8001AN is a typical representative of the commercially available CFOAs. The circuit diagram of the new CFOA model is shown in Fig. 2, where the different stages are presented with controlled sources and passive components.

The proposed model including effects such as (1) accurate inverting and non-inverting input impedance, (2) offset voltage and input bias currents, (3) dc transfer characteristic, (4) ac small-signal frequency response, (5) transient response under a wide range of conditions, (6) input and output voltage and current limitation and (7) output resistance.

The mathematical equations that describe the model can be given as

$$i_y = \left(v_y - v_{io}\right)\left(\frac{1}{r_y} + sC_y\right) \tag{1}$$

$$i_{ib\_y} = i_{ib} + i_{io}/2 \tag{2}$$

$$v_x = \alpha_{yx}v_{y1} - r_x i_x \tag{3}$$

$$i_{ib\_x} = i_{ib} - i_{io}/2 \tag{4}$$

$$i_z = \frac{\alpha_{xz}}{1+s/\omega_p}i_x \tag{5}$$

$$v_z = i_z r_z \tag{6}$$

$$v_o = \begin{cases} v_{max\_p} - r_o i_{ro}, & v_z \geq v_{max\_p} \\ \alpha_{zo}v_z - r_o i_{ro}, & v_{max\_n} < v_z < v_{max\_p} \\ v_{max\_n} - r_o i_{ro}, & v_z \leq v_{max\_n} \end{cases} \tag{7}$$

where $v_{y1} = v_y + v_{io}$ and ω_p is the $-3dB$ radian frequency for the dominant pole of a typical CFOA.

Short-circuit current limiting is simulated with model parameters i_{max_p} and i_{max_n}. In short-circuit mode the output current i_{ro} is limited to one of the values i_{max_p} or i_{max_n}.

Fig. 3 shows the behavioural VHDL-AMS model of CFOA. The library clause and the use clause make all declarations in the packages `electrical_systems` and `math_real` visible in the model. This is necessary, because the model uses nature `electrical` from package `electrical_system`

```
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;
entity      CFOA is
generic (
  iib   : CURRENT := -2.0e-6;       --input bias current
  iio   : CURRENT := 4.0e-6;        --input offset current
  vio   : VOLTAGE := 2.0e-3;        --input offset voltage
  ry    : RESISTANCE := 10.0e6;     --positive input resistance
  cy    : CAPACITANCE := 1.5e-12;   --positive input capacitance
  rx    : RESISTANCE := 50.0;       --negative input resistance
  rz    : RESISTANCE := 900.0e3;    --transresistance
  ro    : RESISTANCE := 50.0;       --output resistance
  ayx   : REAL := 1.0;              --the Y to X voltage gain
  axz   : REAL:= 1.0;               --the X to Z current gain
  fp    : REAL:= 700.0e3;           --fp of gain
  azo   : REAL:= 1.0;               --the Z to O voltage gain
  v_max_p : VOLTAGE := 5.0;         --max pos. output voltage
  v_max_n : VOLTAGE := -5.0;        --max neg. output voltage
  i_max_p : CURRENT := 110.0e-3;    --max pos. output current
  i_max_n : CURRENT := -110.0e-3); --max neg. output current
  port (terminal y, x, output : electrical);
end entity CFOA;
architecture arch_CFOA of CFOA is
-- inner terminals
  terminal n0, n1, z: electrical;
-- inner branch quantities and free quantities
  quantity vy across          y to electrical_ref;
  quantity v_io across i2 through y to n0;
  quantity vy1 across iy, icy, iib_y through n0 to electrical_ref;
  quantity vx across ix, iib_x through x to electrical_ref;
  quantity iz through electrical_ref to z;
  quantity irz through z to electrical_ref;
  quantity vz across          z to electrical_ref;
  quantity vo1 across io1 through n1 to electrical_ref;
  quantity vro across iro through n1 to output;
  quantity voutput across output to electrical_ref;
  quantity iro_h : current;
-- constants
  constant wp: REAL := fp * math_2_pi; -- -3db frequency in radians
  constant num: REAL_VECTOR := (0 => axz);
  constant den: REAL_VECTOR := (1.0, 1.0/wp);
begin
--***input stage***--
  v_io == vio;
  iy  == vy1/ry;
  icy == cy * vy1'dot;
  iib_y == iib + iio/2.0;
  vx == ayx * vy1 + ix * rx;
  iib_x == iib - iio/2.0;
--***transfer stage***--
  iz == ix'ltf(num, den);
  irz == vz/rz;
--***output stage***--
  iro_h == vro/ro;
--limitation of the output voltage
  if vz'above(v_max_p) use vo1 == v_max_p;
      elsif not vz'above(v_max_n) use vo1 == v_max_n;
    else vo1 == azo * vz;
end use;
--limitation of the output current
if iro_h'above(i_max_p) use iro == i_max_p;
      elsif not iro_h'above(i_max_n) use iro == i_max_n;
    else iro == iro_h;
 end use;
end architecture arch_CFOA;
```

Fig. 3. A CFOA behavioural VHDL-AMS model.

and constant `math_2_pi` for the value of π from package `math_real`. The proposed CFOA model is composed by an *entity* and an *architecture*, where bold text indicates reserved words and upper-case text indicates predefined concepts. The entity declares the generic model parameters and specifies three interface terminals of nature `electrical`. The parameters are given with concrete numerical values for the CFOA AD8001AN. The proposed CFOA model includes the following electrical terminals: non-inverting input – `y`, inverting input – `x` and output – `o` (or `output`). Furthermore, the model has three inner terminals: `n0`, `n1` and `z`. They are used to specify the voltages `vy1`, `vz` and `vo1`, respectively.

The architecture of the model is subdivided into three parts: *input stage*, *transfer stage* and *output stage*. It contains the implementation of the model. The architecture is coded by using a style combining structural and behavioural elements. The structural description is the netlist of the model and the behavioural description consists of simultaneous statements to describe continuous behaviour.

IV. MODEL PERFORMANCE

The verification of the proposed behavioural model, shown Fig. 3, is performed by comparing simulation results with the manufacturer's data and with the results obtained by simulation of the PSpice macromodel supplied from Analog Devices. The test circuits for simulation modelling are created following the test conditions given in the semiconductor data books of the corresponding CFOA. The power supply voltages of the circuits are chosen to be ±5V. The model parameters α_{yx}, α_{xz} and α_{zo} are approximately equal to 1.

The simulation modelling of the proposed behavioural model of the CFOA was implemented within simulation program System Vision 5.5 (from Mentor Graphics) and simulation modelling of the macromodel AD8001AN/AD was performed with OrCAD PSpice.

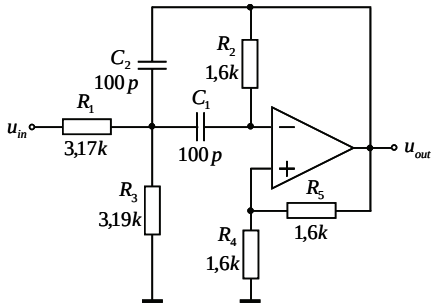
In Table 1 are presented the simulation results and the data sheet parameters for the CFOA AD8001AN. As a result, the proposed behavioural CFOA model corresponds with the parameters of the AD8001AN and it is more accurate at DC and low frequencies than the AD8001AN/AD.

TABLE I
COMPARISON BETWEEN SIMULATION RESULTS AND DATA SHEET

Parameter	AD8001AN Data sheet	AD8001AN/AD macromodel	The proposed CFOA model
DC parameters			
Input offset voltage v_{io}	$2mV$	$5mV$	$2mV$
– Input bias current – i_{ib_x}	$5\mu A$	$6\mu A$	$5{,}01\mu A$
+ Input bias current – i_{ib_y}	$3\mu A$	$25\mu A$	$3\mu A$
AC parameters			
Transresistance – r_z	$900k\Omega$	$316k\Omega$	$900k\Omega$
Input resistance:			
+Input – r_y	$10M\Omega$	$3{,}3M\Omega$	$10M\Omega$
–Input – r_x	50Ω	51Ω	50Ω
+ Input capacitance – C_y	$1{,}5\,pF$	$1{,}5\,pF$	$1{,}5\,pF$
–3 dB Small Signal Bandwidth	$880MHz$ (1) $260MHz$ (2)	$370MHz$ (1) $427MHz$ (2)	$870MHz$ (1) $270MHz$ (2)
Dominant pole frequency– f_p	$700kHz$	$896kHz$	$700{,}01kHz$
Slope (open loop)	$-20dB/dec$	$-20dB/dec$	$-20dB/dec$
Output voltage swing – V_{max}	$\pm 3{,}1V$ (3)	$\pm 2{,}68V$ (3)	$\pm 3{,}09V$ (3)
Short circuit current – I_{max}	$100mA$	$85{,}64mA$	$100{,}01mA$
Output resistance – r_o	50Ω	51Ω	50Ω

Notes: (1) $A_U = +1$ ($R_F = 649\Omega$ [15]); (2) $A_U = +10$ ($R_F = 470\Omega$ and $R_N = 51\Omega$ [15]); (3) $R_L = 100\Omega$.

To validate the proposed CFOA model, simulation of Deliyannis-Frend biquad bandpass filter shown in Fig. 3 was carried out for both the aforementioned model and the macromodel given by Analog Devices in the PSpice library. The results are shown in Fig. 4a and Fig. 4b.



Bandpass filter with parameters:

$f_o = 1MHz$

$Q = 1$

$H_{oBP} = 1$

$n = 2$

Fig. 3. The Deliyannis-Frend biquad filter used in testing the different CFOA models.

The result of the simulations performed shows that the presented model corresponds to the AD8001AN/AD for frequencies from 0 up to $100MHz$. At higher frequencies the macromodel supplied from Analog Devices is superior to the behavioural one, with the expense of a much more complicated set of mathematical equations that describe the proposed model.

The purpose of developing that CFOA model was to introduce a behavioural model that is suitable for analyses of the mixed-signal applications with VHDL-AMS simulators yet quite accurate to a wide frequency range.

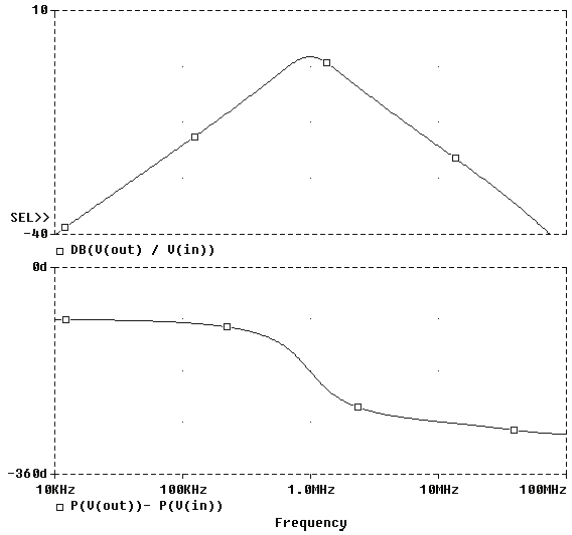


Fig. 4a. The simulated response of the bandpass filter shown in Fig. 3 for the AD8001AN/AD.

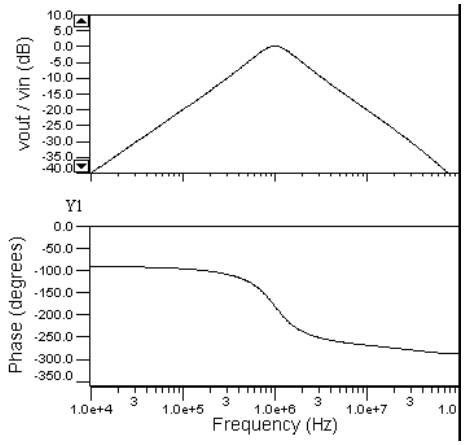


Fig. 4b. The simulated response of the bandpass filter shown in Fig. 3 for the proposed CFOA model.

V. Conclusion

In this paper behavioural VHDL-AMS model of CFOA has been presented. The proposed model accurately describes the behaviour of a typical CFOA over a wide frequency range, including electrical parameters such as inverting and non-inverting input impedance, open-loop transresistance, bandwidth, voltage and current limitations, output resistance, etc. To achieve simplicity of the mathematical equations describing the model, it neglects several second-order effects found in the CFOAs (such as the frequency dependence of the output impedance of the voltage followers, the CMRR and the temperature effects). One of the aims of the further work is to explore the possibility of modelling second-order effects of the typical CFOA, which are taken into consideration for designing high-frequency mixed-signal applications.

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