Investigations of Power Losses in Off-Chip and On-Chip Inductors

Tihomir S. Brusev[1] and Boyanka M. Nikolova[2]

Abstract – **This paper includes investigations of power losses in off-chip and on-chip filter inductors in monolithic dc-dc converter designed on CMOS 0.35 μm technology. Chip coils of the company Murata are used for off-chip inductors. For the extraction of the model's parameters of integrated inductors of CMOS 0.35 μm process is used one of the Cadence tools named "Virtuoso Passive Component Designer". Comparison between power losses in off-chip and on-chip inductors is made.**

Keywords – **power losses, off-chip and on-chip inductors, dc-dc converters.**

I. INTRODUCTION

The fully monolithic dc-dc converters can reduce the cost and size of the battery powered portable electronic devices. One of the most important parameters in the dc-converters is efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} , \qquad (1)$$

where P_{OUT} is the average output power, P_{IN} is the average input power of the converter. The losses in power stage of buck converter are much higher compare to the energy dissipation in the feedback control system [1]. They dominate and determine the efficiency of the system. The power losses in the filter inductor can seriously decrease the overall efficiency of the converter's system. It's very important to be investigated and compared power dissipations when off-chip and on-chip filter components are used. Integrated inductors occupied huge silicon area. Therefore is necessary to be estimated which type of inductors is more suitable for the designed dc-dc converter.

This paper presents the investigations results of power losses in filter inductor of monolithic dc-dc converter designed on CMOS 0.35 μm technology in buck converter implemented on standard CMOS 0.35-μm technology. In Section II are presented the received simulations results with Cadence. This section is divided on two parts. In Section II *A* are shown the received results for power dissipations in the off-chip filter inductor. For the investigations are used chip coils of the company Murata. In Section II *B* are presented

[1]Tihomir S. Brusev is with the Faculty of Telecommunications, Technical University of Sofia, Kl. Ohridski 8, 1797 Sofia, Bulgaria, E-mail: brusev@ecad.tu-sofia.bg

[2]Boyanka M. Nikolova is with the Faculty of Telecommunications, Technical University of Sofia, Kl. Ohridski 8, 1797 Sofia, Bulgaria, E-mail: bnikol@tu-sofia.bg

power losses when on-chip filter inductors of CMOS 0.35 μm process are used. Influence of the low Q-factor of integrated filter inductor over the dc-dc converter efficiency is evaluated.

II. POWER LOSSES IN OFF-CHIP AND ON-CHIP INDUCTORS

In Fig. 1 is shown the circuit of a buck converter implemented on standard CMOS 0.35 μm technology. For the power losses investigation of off-chip and on-chip filter inductors an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage V_{out} is regulated to 1.2V, which on the other hand is determined by the standard supply voltages of advanced CMOS processes.
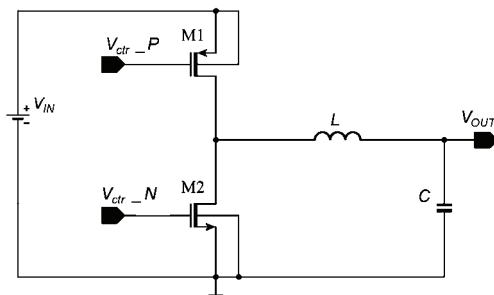

Fig. 1. Synchronous buck converter schematic.

Part of the total power losses in the monolithic switching mode buck dc-dc converter is due to the series resistance and parasitic capacitance of the filter inductor. Integrated inductors have high series resistance, which grows up with increasing of the inductor's value. This lead to the low quality factor Q of these components [2]. Integration of a spiral inductor with sufficient inductance is not feasible, because they occupy huge silicon area and have low Q factor. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance is equal to [3]:

$$P_{ind} = b \left[\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD1}^2}{R_{L0} \Delta i_L} \right] , \qquad (2)$$

where b is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray capacitance and parasitic series resistance per 1 nH inductance, V_{DD1} is power supply.

The influence of switching frequency f_s and inductor current ripple Δi_L over the power losses in the filter inductor are investigated. Integrated passive inductors occupied huge silicon area, which make more expensive the electronic devices. It's necessary to be estimated energy dissipation in off-chip and on-chip filter inductors.

Power losses in the filter inductor of the synchronous buck converter designed on CMOS 0.35 µm technology are analyzed with Cadence, as a function of switching frequency f_s and inductor current ripple Δi_L. Evaluated and compared are power losses in off-chip and on-chip filter inductor of monolithic buck dc-dc converter.

A. Power losses in the off-chip filter inductor

In this section is evaluated power losses in off-chip filter inductors of monolithic dc-dc converter designed on CMOS 0.35-µm technology. The investigated inductors are chip coils for high frequency horizontal wire wound of the company Murata. They have broad range of inductance and high self-resonant frequency. This realizes high Q-factor and stable inductance at high frequency. Their low dc resistance is ideal for low power losses. These off-chip inductors are often used in telecommunication applications.

The received results of power losses in the off-chip filter inductor of buck dc-dc converter are presented below. For the simulations with Cadence on CMOS 0.35-µm technology are used inductor's models of the company Murata [4].

In Table I are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA and Δi_L=0.5x$I_{out\,(av)}$.

TABLE I

POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; Δi_L/0.5x$I_{OUT\,(AV)}$;

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	5000	2000	1500	1000
Δi_L/0.5x$I_{out\,(av)}$	0.5	0.5	0.5	0.5
P_{ind} [mW]	0.0579	0.148	0.316	1.02

In Table II are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA and Δi_L=$I_{out\,(av)}$.

In Table III are presented power losses in the off-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA and Δi_L=2x$I_{out\,(av)}$. Received simulations results for power losses in the off-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\,(av)}$=20 mA given in Table I, Table II and Table III, are graphically

presented in Fig.2. For simulations the inductor's models of the company Murata are used.

TABLE II

POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; Δi_L/$I_{OUT\,(AV)}$;

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	1000	750	500
Δi_L/$I_{out\,(av)}$	1	1	1	1
P_{ind} [mW]	0.056	0.183	0.333	1.02

TABLE III

POWER LOSSES IN THE OFF-CHIP INDUCTORS OF BUCK CONVERTER; Δi_L/2x$I_{OUT\,(AV)}$;

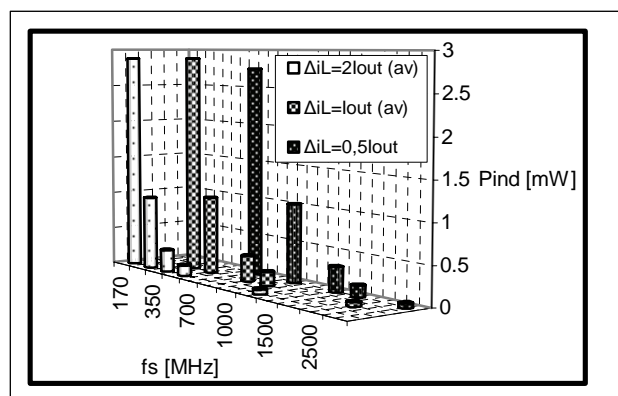|	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	1250	500	350	250
Δi_L/2x$I_{out\,(av)}$	2	2	2	2
P_{ind} [mW]	0.062	0.139	0.291	0.97

Fig. 2. Power losses in the off-chip filter inductor of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\,(av)}$=20 mA.

Power losses in the off-chip filter inductor of buck dc-dc converter decreased with increasing of switching frequency f_s and inductor current ripple Δi_L.

B. Power losses in the on-chip filter inductor

The dependence of the power dissipation in on-chip filter inductors of CMOS 0.35-µm technology are investigated and evaluated. Standard monolithic inductors are not optimized for the specific applications. In the other hand theirs number of values are limited. That's way is necessary to be designed integrated inductors with desired value and geometry. One of the Cadence tools named "Virtuoso Passive Component

Designer" is used for the extraction of inductor's model parameters [5].

Fig. 3. Window from CADENCE tool "Virtuoso Passive Component Designer".

The model of on-chip inductors used in the investigations is shown in Fig. 4. The parameters presented in Fig. 4 are: L_s – series inductance; R_s – series resistance; C_p – parallel capacitance; $C_{OX1/2}$ – oxide capacitance; $C_{s1/2}$ – substrate capacitance; $R_{s1/2}$ – substrate resistance.

The values of the extracted parameters are used for simulations. The received results of power losses in the on-chip filter inductor of buck dc-dc converter are presented below. Investigations are made for average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA.
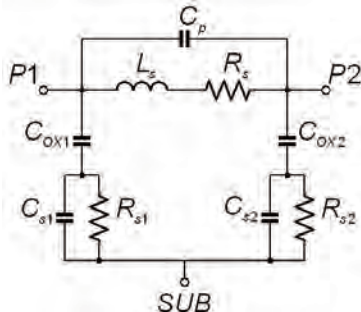

Fig. 4. The model of on-chip inductors.

In Table IV are presented power losses in the on-chip filter inductor P_{ind} as a function of switchnig frequency f_s and inductor current ripple Δi_L, for $\Delta i_L = 0.5 \times I_{out\,(av)}$.

In Table V are presented power losses in the on-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA and $\Delta i_L = I_{out\,(av)}$.

In Table VI are presented power losses in the on-chip filter inductor P_{ind} as a function of switching frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\,(av)}$ equal to 20 mA and $\Delta i_L = 2 \times I_{out\,(av)}$.

Received simulations results for power losses in the on-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\,(av)} = 20$ mA given in Table IV, Table V and Table VI, are graphically presented in Fig. 5.

TABLE IV

POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L / 0.5 \times I_{OUT\,(AV)}$;

	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	5000	4000	3000	2000
$\Delta i_L / 0.5 \times I_{out\,(av)}$	0.5	0.5	0.5	0.5
P_{ind} [mW]	15.37	15.9	16.35	23.59

TABLE V

POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L / I_{OUT\,(AV)}$;

	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	2000	1500	1000
$\Delta i_L / I_{out\,(av)}$	1	1	1	1
P_{ind} [mW]	15.37	15.74	16.37	23.6

TABLE VI

POWER LOSSES IN THE ON-CHIP INDUCTORS OF BUCK CONVERTER; $\Delta I_L / 2 \times I_{OUT\,(AV)}$;

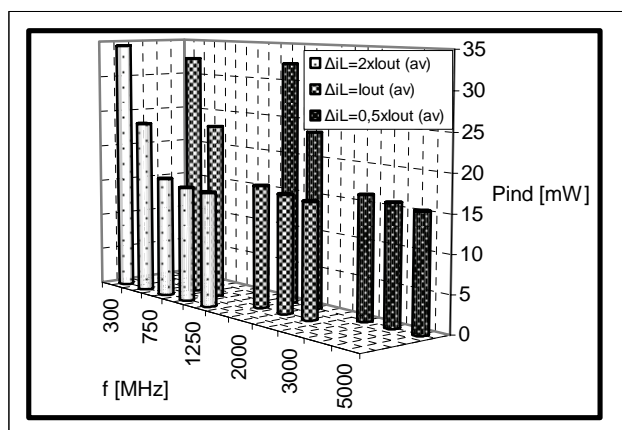|	L=10 nH	L=14.1 nH	L=28.2 nH	L=51 nH
$I_{out\,(av)}$ [mA]	20	20	20	20
f_s [MHz]	1250	1000	750	500
$\Delta i_L / 2 \times I_{out\,(av)}$	2	2	2	2
P_{ind} [mW]	15.37	15.5	16.3	23.59

Fig. 5. Power losses in the on-chip filter inductor of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\,(av)} = 20$ mA.

As can be seen from Fig. 2 and Fig. 5 power losses in the filter inductor of buck dc-dc converter goes down with increasing of switching frequency f_s and inductor current ripple Δi_L. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35 µm process (Fig. 2, Fig. 5). The reason is the high series resistance and low Q-factor of the on-chip inductors.

The efficiency of the designed monolithic dc-dc converter as a function of on-chip filter inductors is evaluated. Investigations are made at different average outputs currents ($I_{out\ (av)}$) of the circuit. In Table VII are shown received results at $I_{out\ (av)} = 5$ mA. In Table VIII are shown received results at $I_{out\ (av)} = 20$ mA. The simulation results shown in Table VII and Table VIII are graphically presented in Fig. 6.

TABLE VII

EFFICIENCY OF THE DC-DC CONVERTER

	L=1.4 nH	L=2.6 nH	L=4.7 nH	L=9 nH
$I_{out\ (av)}$ [mA]	5	5	5	5
η [%]	8.7	13.9	15.4	15.5

TABLE VIII

EFFICIENCY OF THE DC-DC CONVERTER

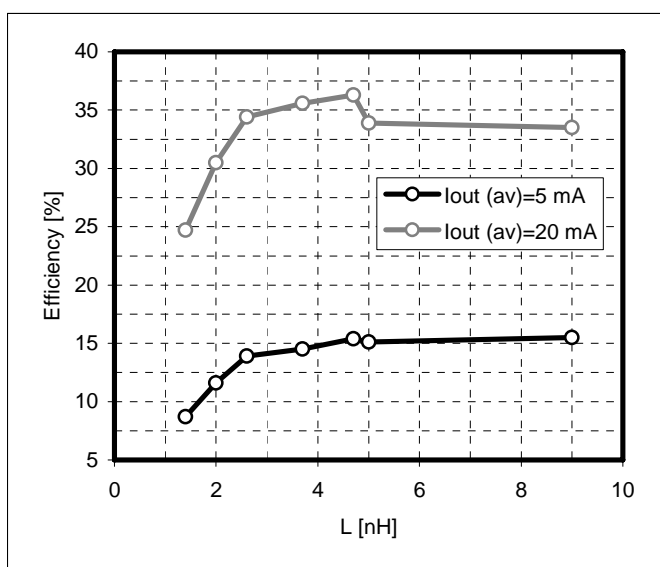|	L=1.4 nH	L=2.6 nH	L=4.7 nH	L=9 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
η [%]	24.7	34.4	36.3	33.5

Fig. 6. Efficiency of the monolithic dc-dc converter designed on CMOS 0.35 µm technology as a function of different on-chip inductors.

The maximum value of the converter's efficiency when on-chip filter inductors are used is 36 %. One of the reasons is low Q-factor of the available integrated inductors.
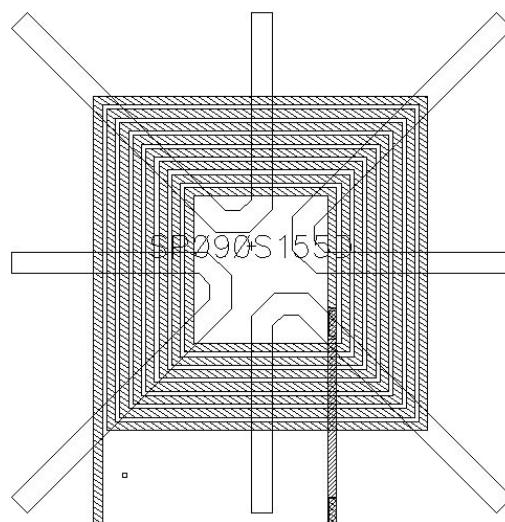

Fig. 7. The layout of on-chip inductors.

III. CONCLUSION

The power losses in the off-chip and on-chip filter inductors of monolithic buck dc-dc converter designed on CMOS 0.35 µm technology has been investigated. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35 µm process (Fig. 2, Fig. 5). The received results show that by increasing of switching frequency f_s of the circuit power dissipations in the filter inductor decreased. By increasing of the Δi_L requirements for the inductor's value decreased for fixed switching frequency f_s. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the Δi_L leads to the increasing of rms current through the inductor, which causes to the bigger conduction losses in the inductor.

ACKNOWLEDGEMENT

REFERENCES

[1] Kurson V., S. G. Narenda, V. K. De, and E. G. Friedman, "Monolithic DC-DC Converter Analysis and MOSFET Gate Voltage Optimization," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 279-284, March 2003.

[2] Gardner D., A. M. Crawford, S. Wang, "High Efficiency (GHz) and Low Resistance Integrated Inductors Using Magnetic Materials," *Proceedings of the IEEE International Interconnect Technology Conference*, pp. 101-103, June 2001.

[3] Kurson V., "Supply and Threshold Voltage Scalind Techniques in CMOS Circuits", 2004.

[4] http://www.murata.com

[5] http://www.cadence.com