Investigation of Power MOSFET and IGBT Gate Drivers using SPICE

Georgi Tzv. Kunov[1] and Elissaveta D. Gadjeva[2]

Abstract **–The driver circuits for control of the power MOSFET and IGBT transistors are of significant importance in the field of converter device design. A number of companies offer specialized integrated circuits for this purpose. They are successfully used in the cases when the transistors operate in the mode of soft switching (ZVS and ZCS). In the present paper, the influence of the shape of control pulses on the commutation processes of MOSFET and IGBT commutation is considered, in the mode of hard switching. A special attention is paid on a driver circuit limiting the speed of variation of the voltage and the current (du/dt and di/dt), which leads to reducing of the overvoltages on the transistors. The influence on the commutation losses is investigated when applying the proposed approach using the PSpice simulator.**

Keywords **– MOSFET/IGBT Gate Driver, Computer simulation, MOSFET/IGBT Gate Driver Spice model**

I. INTRODUCTION

In the field of power converters realized by MOSFET/IGBT transistors, the commutation processes in transistors are significantly influenced on the type of the used Gate Driver circuits [1,2,3]. A number of companies offer specialized integrated Gate Driver circuits. Among the most widespread are the integrated drivers of the I21xx series of the company International Rectifiers and their analogs MPIC21 of the company Motorola, the series TC4xxx of MICROCHIP/TELCOM, IXDDxxx of IXYS, etc. The listed specialized Gate Driver circuits are intended for commutation of power transistors with differing powers. They do not take into account the influence of the parasitic capacitances (the Miller capacitance and the output capacitance) on the commutation processes. The time interval for charge and discharge of the parasitic capacitances significantly influences on the:

- switching speed (*dv/dt* and *di/dt*) and hence on the EMI/RFI emissions [4,5];
- dynamic power losses;
- overvoltages on the transistors;
- reliable turn-on and turn-off of the transistors during the switching.

Based on *dv/dt* and *di/dt* tracking, a reliable (but too complex) driver circuit is proposed in [6] for power IGBT transistors. It satisfies the listed above conditions. A simple and cheap solution to suppress the Miller capacitance current represents the specialized integrated circuit ACDL331J [7]. The function *two-level turn-off* is added in [8] to the abilities of [7], which allows to decrease *dv/dt* and hence the overvoltages on the transistors.

In the present paper, MOSFET/IGBT driver circuits are investigated using *Cadence PSpice*, which realize the functions *one-level turn-on/turn-off* and *two-level turn-on/ one-level turn-off*. The investigated circuit using two drivers IXDD414 corresponds to the circuit proposed in [5].

[1]Georgi Kunov is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, Klimenrt Ohridski Blvd. 8, 1000 Sofia, Bulgaria, E-mail: gkunov@tu-sofia.bg

[2]Elissaveta Gadjeva is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, Klimenrt Ohridski Blvd. 8, 1000 Sofia, Bulgaria, E-mail: egadjeva@tu-sofia.bg

II. INVESTIGATION OF POWER MOSFET AND IGBT GATE DRIVERS

A. One-level Turn-on/Turn-off Gate Drivers

The circuit of one-level turn-on/turn-off Gate Drivers is shown in Fig. 1. The presented connection of the power transistors allows to investigate the influence of the Miller capacitance and the output capacitance on the following characteristics of power transistors: peak current value, Gate-Source voltage and peak value of the commutation power. The simulation results are shown in Fig. 2 for V12= V22=0V, i.e. for the unipolar supply voltage of the integrated drivers IXDD414. The simulation results for V12=V22=5V are shown in Fig. 3. It is seen from the comparison of the results in Fig. 2 and Fig. 3 that for the case of bipolar supply voltage the peak value of the capacitance current through the transistors decreases three times and the peak value of the switching power decreases four times. The additional sources V12 and V22 increase the threshold voltage V_{th} of the transistors, thus avoiding the negative influence of the Miller capacitance current on the gate voltage.

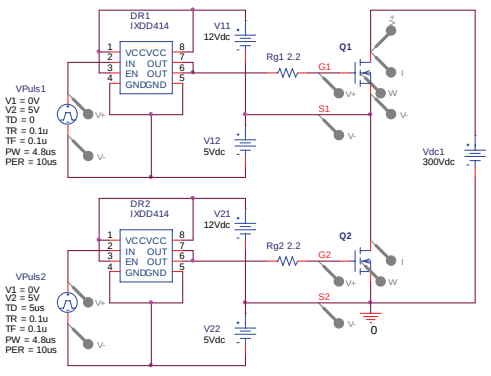

Fig. 1. The circuit of one-level turn-on/turn-off Gate Driver

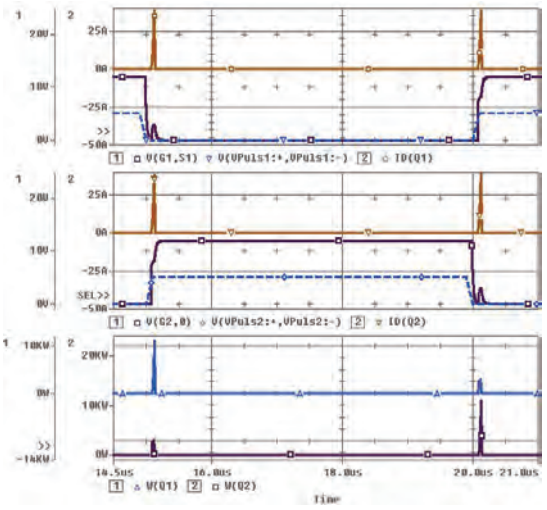

Fig. 2. Simulation results of the circuit in Fig. 1 for V12=V22=0V

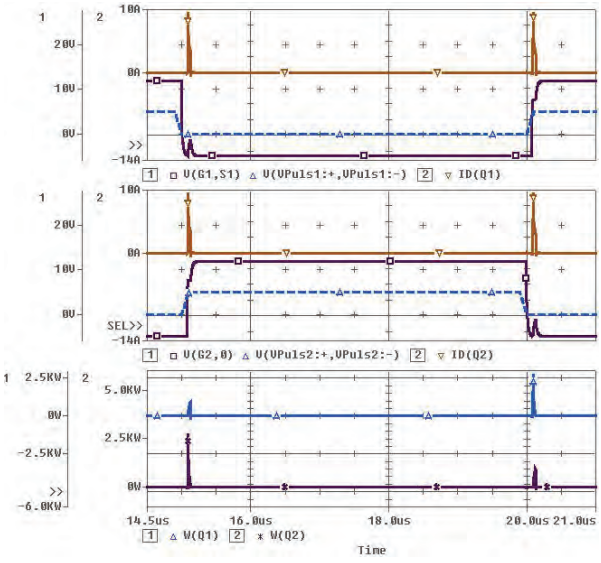

Fig. 3. Simulation results of the circuit in Fig. 1 for V12=V22=5V

B. Two-level Turn-on/One-level Turn-off Gate Driver

The circuit of the two-level turn-on/one-level turn-off Gate Driver is shown in Fig. 4. Each transistor is controlled by two drivers IXDD414.

The switching from "0" in "1" of DR12 and DR22 is delayed with respect to DR11 and DR12. This time delay is defined by the turn-on time t_{don} of the transistors. The moment of turn-on is tracked by the diodes D1, D2 and comparators V1A and V2A. During the time interval t_{don} the resistor dividers R1,R2 and R3,R4 limit the gate voltage at the level below the nominal level. It is seen from the simulation results shown in Fig. 5.

From the comparison of the obtained results in Fig. 5 and the results for one-level turn-on (Fig. 3) it can be seen that the peak value of the current through the transistors and the switching power decrease two times.

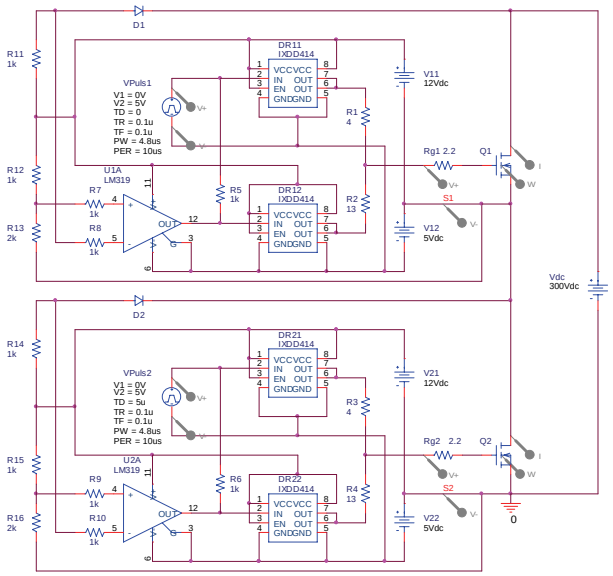

Fig. 4. The circuit of the two-level turn-on/one-level turn-off Gate Driver

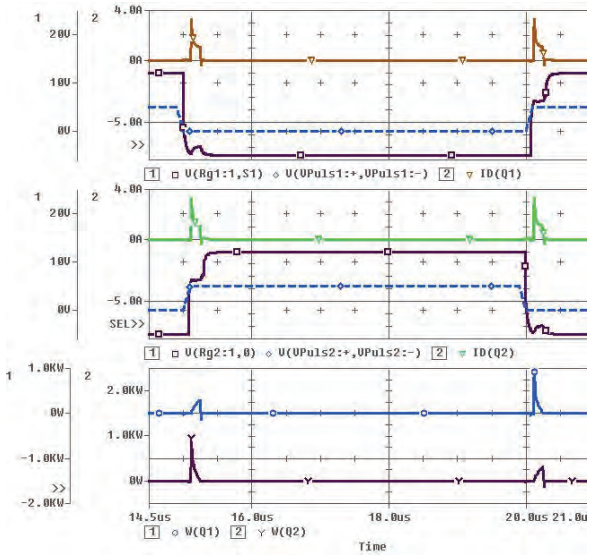

Fig. 5. Simulation results of the circuit in Fig. 4

C. Two-level Turn-on/One-level Turn-off Gate Driver of BUCK Converter

The simulation circuit is shown in Fig. 6. In this case the voltage value of the first turn-on level is defined parametrically. In order to avoid the transients of the load current, the load is represented by a current source I_{load}. The following dependencies are investigated:

- *di/dt* as a function of the threshold voltage V_{th} for a constant current I_{load} (Fig. 7);
- *dv/dt* as a function of the current I_{load} for a constant threshold voltage V_{th} (Fig. 8).

The simulation results for the variation of the collector-emitter voltage are shown in Fig. 9 for different values of the threshold voltage V_{th}.

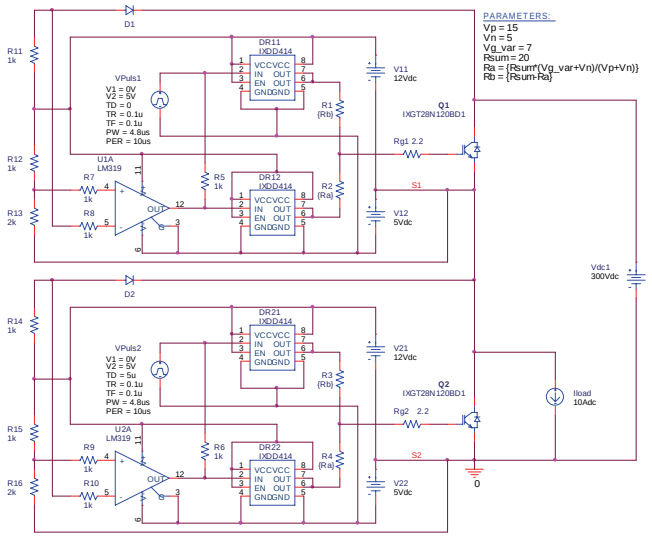

Fig. 6. The circuit of the two-level turn-on/one-level turn-off Gate Driver of BUCK converter

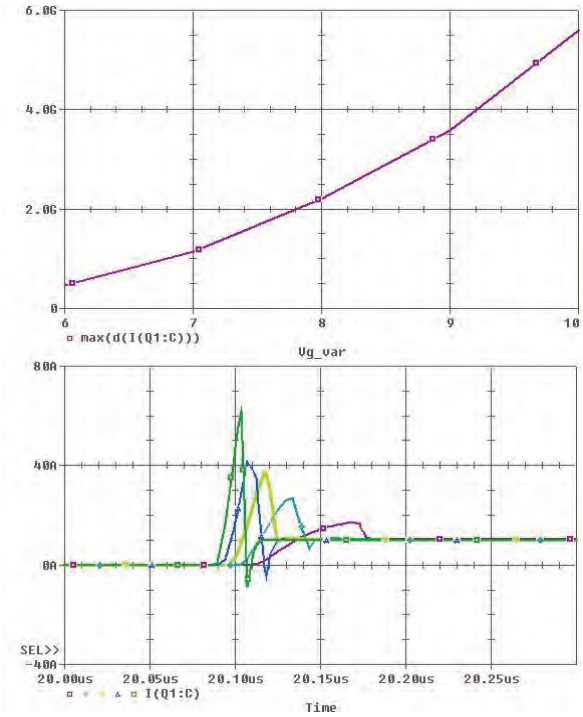

Fig. 7. The dependence of *di/dt* as a function of the threshold voltage for a constant current I_{load}

III. PSPICE MODEL

The *PSpice* model of the MOSFET Gate Driver IXDD414 [9] can be applied in the cases when the ground node DGND is connected to the ground 0 of the circuit. When the node DGND is not connected to the ground 0, this *PSpice* model cannot be used. It is necessary to modify the *PSpice* subcircuit description of the driver IXDD414 in order to avoid this restriction. For this purpose, the node 0, participating in the original model description [9], is replaced by the node GND, corresponding to the pin DGND.

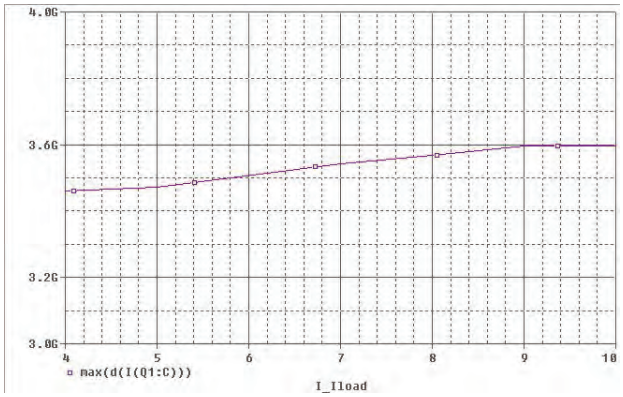

Fig. 8. The dependence of *dv/dt* as a function of the current I_{load} for a constant threshold voltage

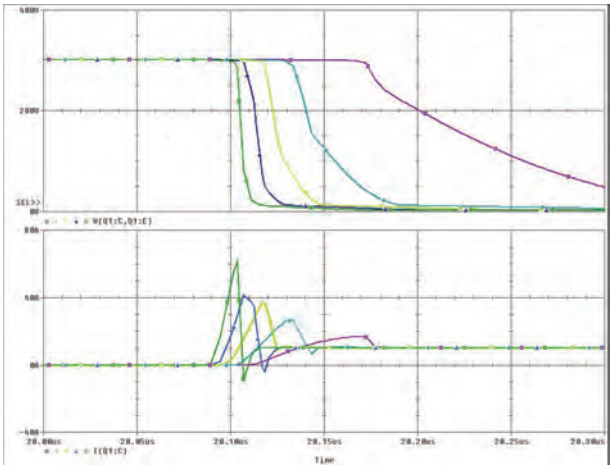

Fig. 9. Simulation results for the variation of the collector-emitter voltage for different values of V_{th}.

In addition, the elements R33 and R34, connecting the node GND to the ground 0 [9], are omitted (represented as comments by the symbol * in first column). The resulting modified *PSpice* model of IXDD414 is represented in Table I. The modified element descriptions are given in italic.

The obtained generalized *PSpice* model in Table I allows to connect the node DGND of the driver IXDD414 to arbitrary circuit node. In this way, circuits with two and more IXDD414 elements can be analyzed, as shown in Fig. 6.

IV. CONCLUSION

MOSFET/IGBT driver circuits have been investigated based on computer simulation. The influence of unipolar and bipolar supply voltage of the Gate Drivers is investigated on the peak value of the capacitance currents through the transistors and the switching power. A driver circuit is simulated that realizes the principle of two-level turn-on/one-level turn-off. The obtained results show the decreasing of the peak values of the current and the power during the commutation. The influence of the turn-on threshold voltage on *di/dt* and *dv/dt*. The PSpice model of IXDD414 is improved, which allows its usage as a high-side driver.

TABLE I: PSPICE MODEL OF IXDD414

```
.SUBCKT IXDD414 VCC IN EN GND  VCC OUT OUT GND
Q_Q5   N209276 N03676 GND BC107A
C_C5   N02728 GND  1uF
R_R9   N02728 GND  10k
C_C3   VEE GND  100uF
R_R24   GND TP  10K
R_R26   GND N242307  724
M_Q2 N04428 N209276 GND GND  MNMOS
R_R18   N01509 GND  10k
X_U4   VCC VEE GND LM7805C
R_R12    OUT GND  10k
R_R17    N82692 GND  10k
*R_R34  GND 0  0.0001
M_Q1  N04213 N209203 GND GND  MNMOS
C_C6   VSS GND  47uf
R_R70   GND TEST  1k
R_R15    N161018 GND  10k
C_C2  GND VCC  0.1uF
D_D6  GND N02728 BZ-056
C_C4   VCC GND  100uF
R_R39  GND N260557  2k
R_R35  GND VT  10k
D_D5  GND VSS BZ-056
R_R19   GND N295262  10k
R_R6   N03676 GND  10k
R_R7  N03600 GND  10k
R_R10  N02728 GND  10k
*R_R33   GND 0  0.0001
R_R27  GND N336660  10k
R_R37   GND TP  10k
Q_Q6  N209203 N03030 GND BC107A
R_R4   N03030 GND  10k
R_R36  GND N259753  10k
D_D2  GND N82834 D1N4376
M_Q4  N104168 N04213 GND GND MNFET
R_R28  GND N295639  10k
D_D4 GND N02182 D1N4376
R_R8   N02959 GND  10k
C_C1  VCC GND  220uF
R_R30   GND N242974  100k
R_R16   IN N82692  100
R_R25   N242307 EN  10K
M_Q3  N104168 N04428 VCC VCC MPFET
R_R1   VCC N04213  10K
R_R38  N260557 VCC  10k
R_R2   VCC N04428  10K
D_D6   GND N02728 BZ-056
R_R3    N02959 N03030  5
C_C7    N02959 N03030  1nf
D_D1    N82834 VCC D1N4376
R_R22   VCC N209276  5.0K
R_R5    N03600 N03676  5
C_C8    N03600 N03676 1nf
R_R13   HENABLE N02728  100
D_D3    N02182 VCC D1N4376
R_R23   VCC N209203  5.0K
R_R21   TEST N01509  0.0001
R_R31   VCC VSS  100
R_R11   N104168 OUT  0.01
R_R29   HENABLE N242974  10
X_U9A  N02728 N01509 N03600 VEE GND 74ACT00  PARAMS:
+  IO_LEVEL=0  MNTYMXDLY=0
X_U2A N260557 N260557 N259753 VSS  GND 74ACT08
+ PARAMS:: IO_LEVEL=0  MNTYMXDLY=0
X_U6A N336660 N336660 N295639 VEE  GND 74ACT08
+ PARAMS:  IO_LEVEL=0  MNTYMXDLY=0
X_U22A N295262 N295262 TEST VEE GND  74ACT00 PARAMS
+  IO_LEVEL=0  MNTYMXDLY=0
X_U10A  N01509 N161018 N02959 VEE  GND 74ACT02
+ PARAMS  IO_LEVEL=0 MNTYMXDLY=0
X_U5A TP N336660 VEE GND 74ACT04  PARAMS:
+IO_LEVEL=0   MNTYMXDLY=0
X_U1A  N242307 VT VSS GND 74ACT14 PARAMS:
+ IO_LEVEL=0    MNTYMXDLY=0
X_U7A N82692 TP VEE GND 74ACT04 PARAMS: IO_LEVEL=0
+  MNTYMXDLY=0
X_U3A VT N259753 HENABLE VSS GND  74ACT08 PARAMS
+   IO_LEVEL=0   MNTYMXDLY=0
X_U8A N02728 N161018 VEE GND 74ACT04  PARAMS:
+ IO_LEVEL=0   MNTYMXDLY=0
X_U23A N295639 N295639 N295262 VEE  GND 74ACT00
+  PARAMS: IO_LEVEL=0  MNTYMXDLY=0
.MODEL MNMOS NMOS LEVEL=3 W=4E-6  L=2E-6
+ NSS = 0.00000E+00 VTO = 6.30E-01 TOX = 1.90000E-08
+  XJ = 1.66632E-07  LD = 0.04E-06 RSH = 6.40359E+02
+  NSUB = 1.82429E+16 NFS = 1.26963E+11
+  UO = 5.95254E+02 VMAX = 1.86907E+05
+  DELTA = 8.22502E-01  THETA = 5.77858E-02
+ ETA = 2.1931E-02  KAPPA = 2.60564E-1  CGSO = 7.263E-11
+ CGDO = 7.263E-11 CGBO = 1.1189E-10  CJ = 2.59E-4
+CJSW= 2E-10 PB = 0.811 MJ = 0.36  MJSW = 0.31 TPG = 1
+ DW =-0.18E-6  DL =-0.72500E-06  XQC = 1
.MODEL MPFET PMOS(LEVEL=3 W=4e-3 L=0.01e-006)
.MODEL MNFET NMOS(LEVEL=3 W=4E-3 L=0.01e-006)
.MODEL BC107A NPN
.MODEL BZ-056 D RS=1.E-3  CJO=1.E-12  M=.3333 VJ=.75
+ ISR=7.539E-6  BV=5.009 IBV=43.11E-3 TT=144.3E-9
.MODEL D1N4376 D
.ENDS
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